

WP 16 Demonstration – MMC CHiL testing

By Yongtao Yang

Agenda for the demo

11:30	Registration
12:00 – 13:00	Lunch & Opportunity to network
13:00 – 13:15	Welcome, <i>Theo Bosma, DNV GL</i>
13:15 – 13:30	Introduction to PROMOTioN, <i>Cornelis Plet, DNV GL</i>
13:30 – 13:50	Introduction to WP16 of PROMOTioN, <i>Philipp Ruffing, RWTH Aachen</i>
13:50 – 14:10	Test set-up, methodology & results of MMC HVDC Controller Hardware-in-the-Loop testing, <i>Yongtao Yang, DNV GL</i>
14:10 – 14:40	MMC HVDC Technology in China, <i>Eric Zhang, NR Electric</i>
14:40 – 15:00	Transport to Flex Power Grid Laboratory (incl. safety briefing)
15:00 – 16:30	Demonstration of MMC HVDC converter harmonic impedance measurement and dynamic performance, <i>FPGL Team, DNV GL</i>
16:30 – 17:00	Transport to building B50 and Arnhem Central station

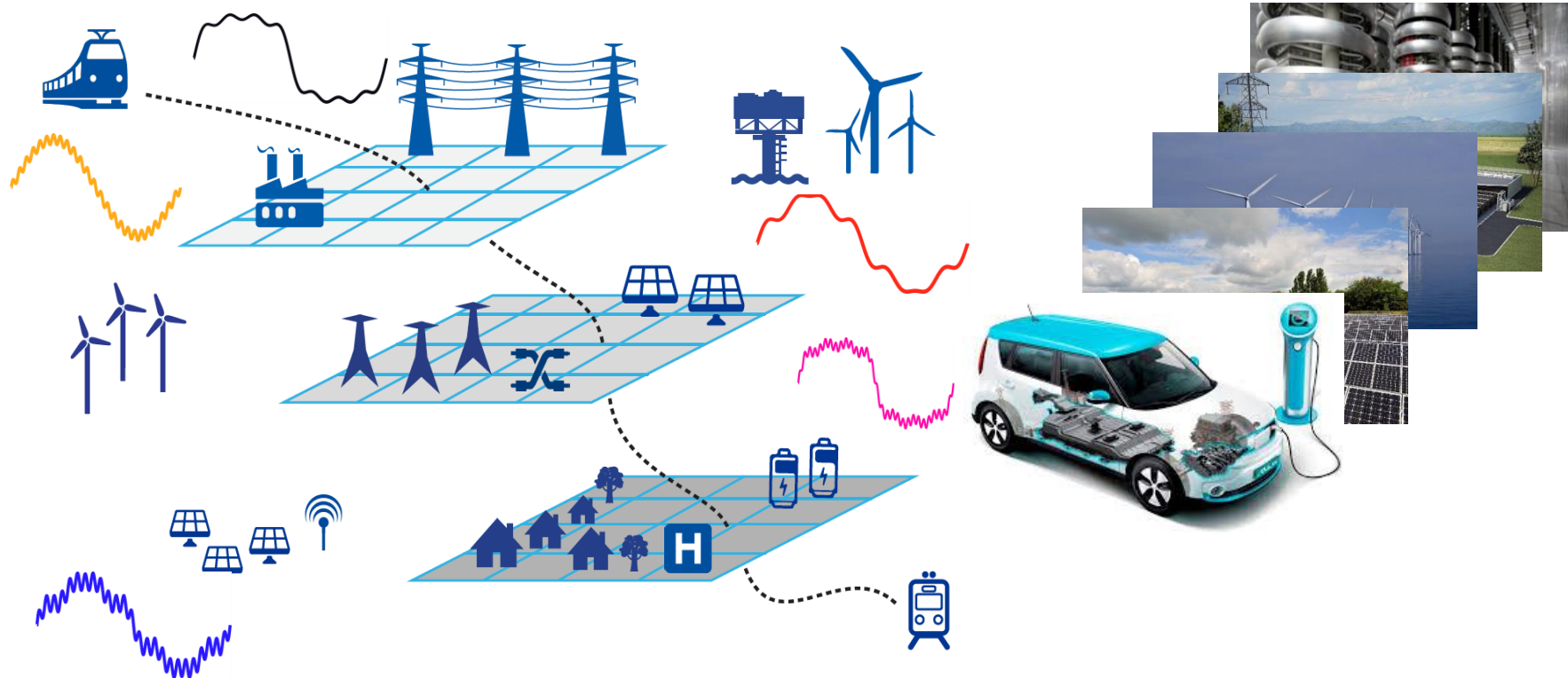


Content

- **Motivation for Control Hardware-in-the-loop testing**
- **Setup of CHIL Testbench for MMC-HVDC/MMC-STATCOM**
- **Update of CHIL Testbench of MMC-HVDC/MMC-STATCOM**

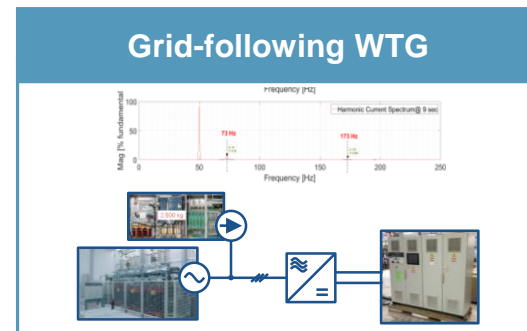
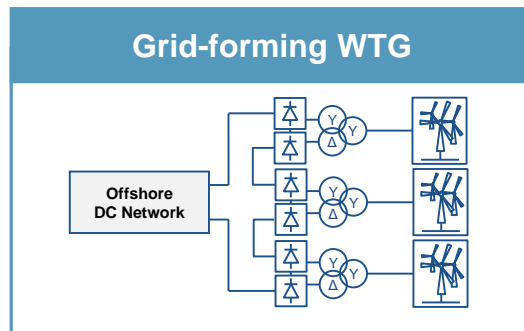
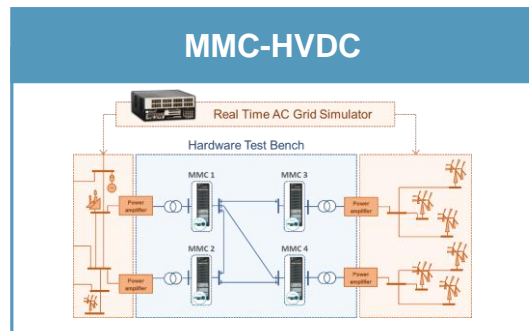


Motivation – Power Electronics Grid



Deliverable D16.5

Implementation of an analytical method for analysis of harmonic resonance phenomena



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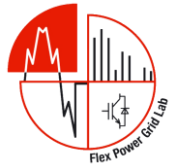


MMC HVDC CHIL Testbench



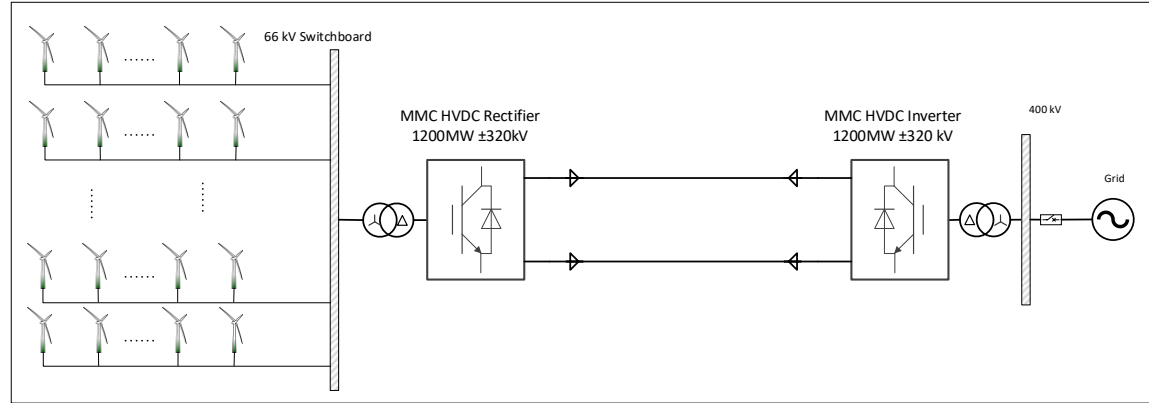
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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

Objectives



Unit MMC resonance performance test

- Small signal perturbation test (injecting harmonic currents)
- Unit MMC converter operated as inverter/rectifier
- Validate the frequency domain performance measurement against theoretical models

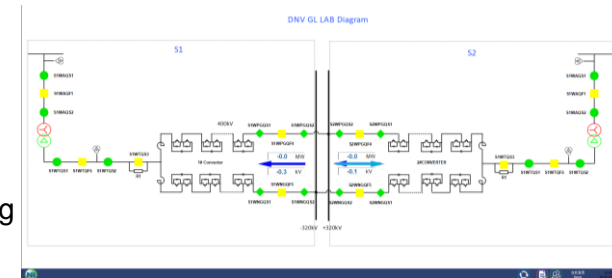


Offshore Wind Park (DC connection) Harmonic Resonance Analysis

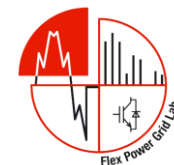
- Using WTG controller scaled up to represent the whole park
- Investigate system level risk of harmonic resonance
- Covering different operation states, e.g. number of connected wind turbines/collector radials, different power levels etc.

AC Grid Support (Optional)

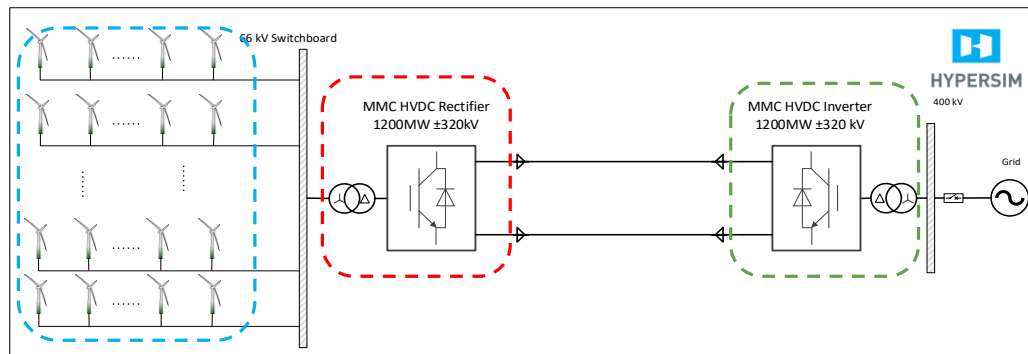
- Fault Ride Through (FRT) testing
- Frequency Support testing
- Power Oscillation Damping (POD) testing



Demo 2.1 MMC HVDC CHiL Test bench



VBC – Valve Base Control
PCP – Pole Control & Protection



↔ **Digital signals**
 ↔ **Analog signals**
 ↔ **Fiber Optics**



WT Converter Controller

Station 1



OP 5700

PCIe



OP 7000



VBC



PCP1






PCP2

Station 2

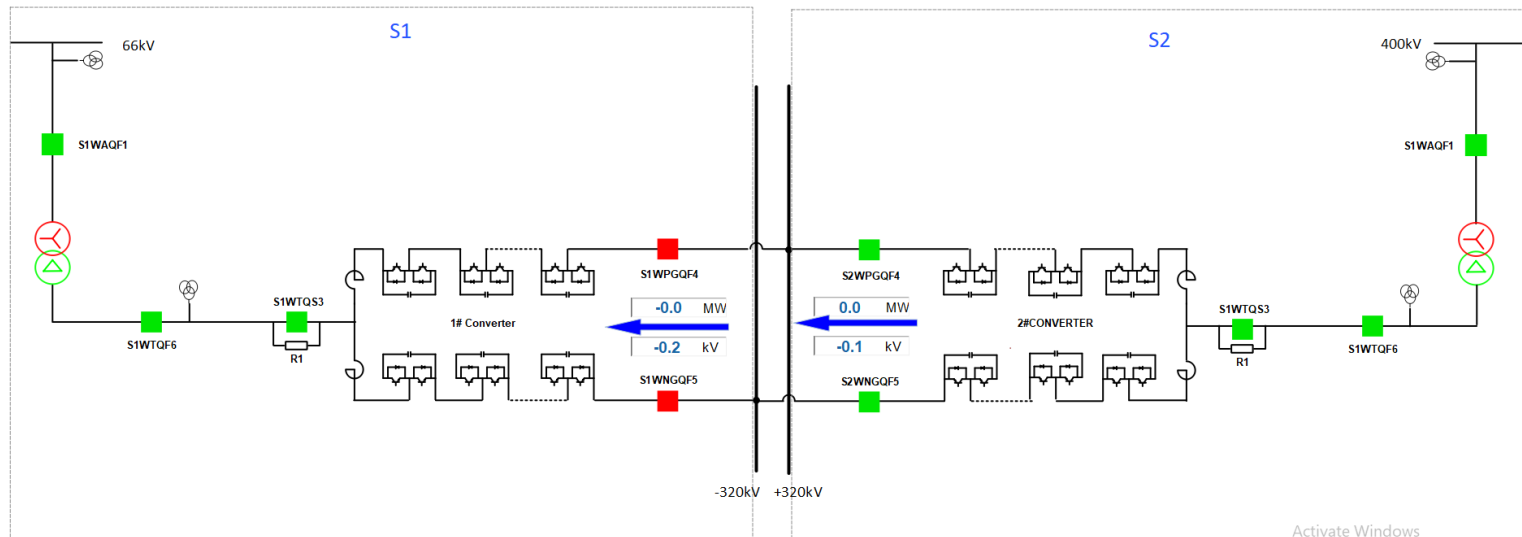


HMI from the NREC SCADA



DNV GL LAB	STATION 1				STATION 2				STATCOM				STATE		STATE				
	P _s	-0.000	MW	Q _s	-0.0	MVar	P _s	-0.000	MW	Q _s	-0.000	MVar	P _s	0.000	MW		Q _s	-0.000	MVar
	I _v	8.174	A	U _v	0.235	kV	I _v	12.343	A	U _v	0.118	kV	I _{sa}	12.956	A		U _{sa}	1.472	kV
	I _s	4.642	A	U _s	0.032	kV	I _s	0.570	A	U _s	0.136	kV	I _{sb}	7.292	A		U _{sb}	1.975	kV
	I _d	1.505	A	U _{dc}	-0.223	kV	I _d	-2.085	A	U _{dc}	-0.101	kV	I _{sc}	9.320	A		U _{sc}	1.564	kV
																STATCOM			

DNV GL LAB Diagram



Activate Windows
Go to Settings to activate Windows.



nit MMC resonance performance test

- ## AC Grid Support

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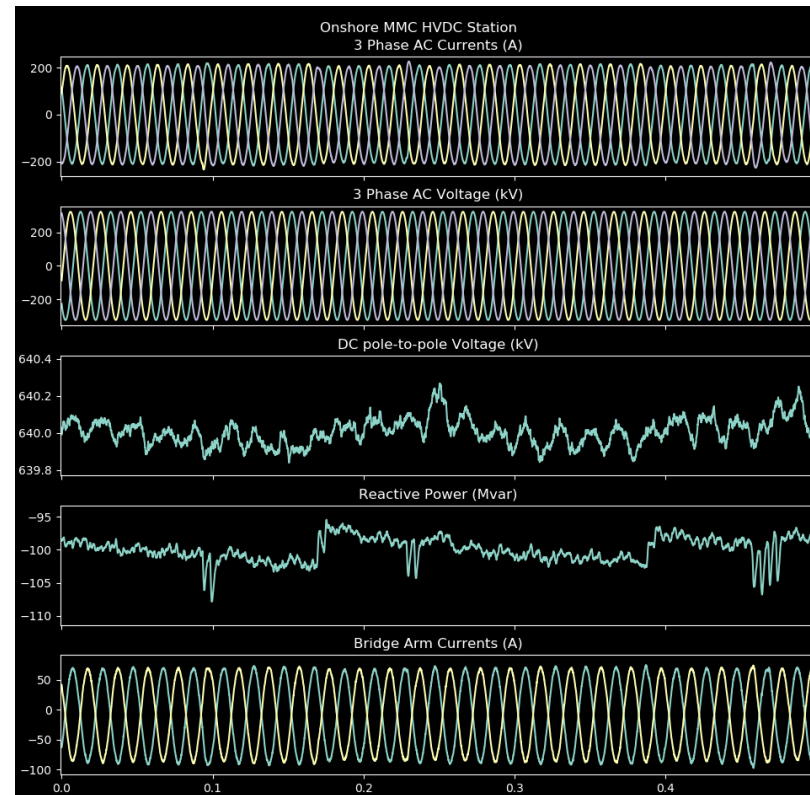
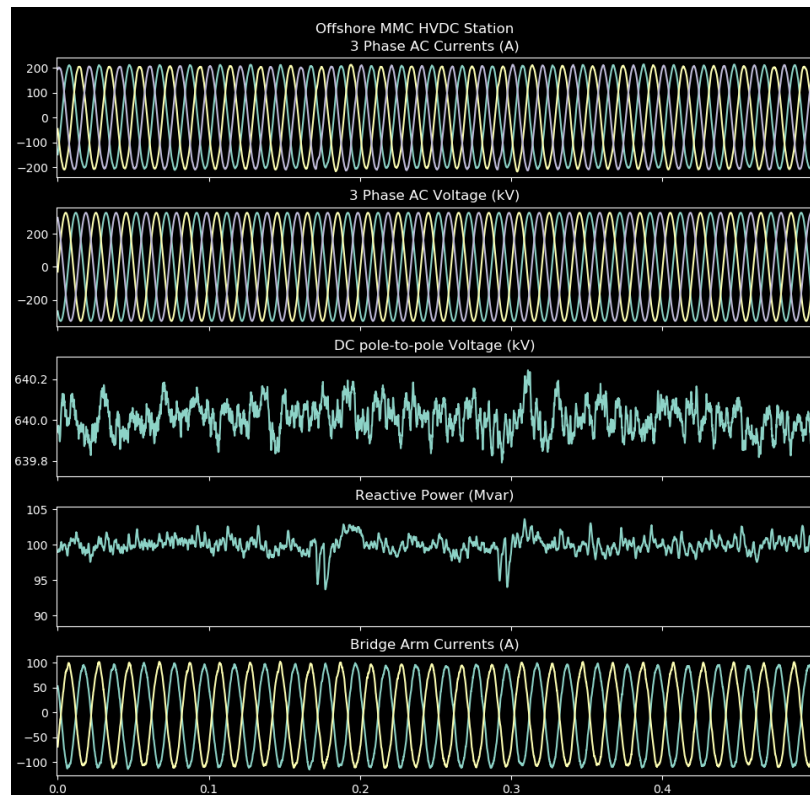


Testcases and results of MMC CHiL

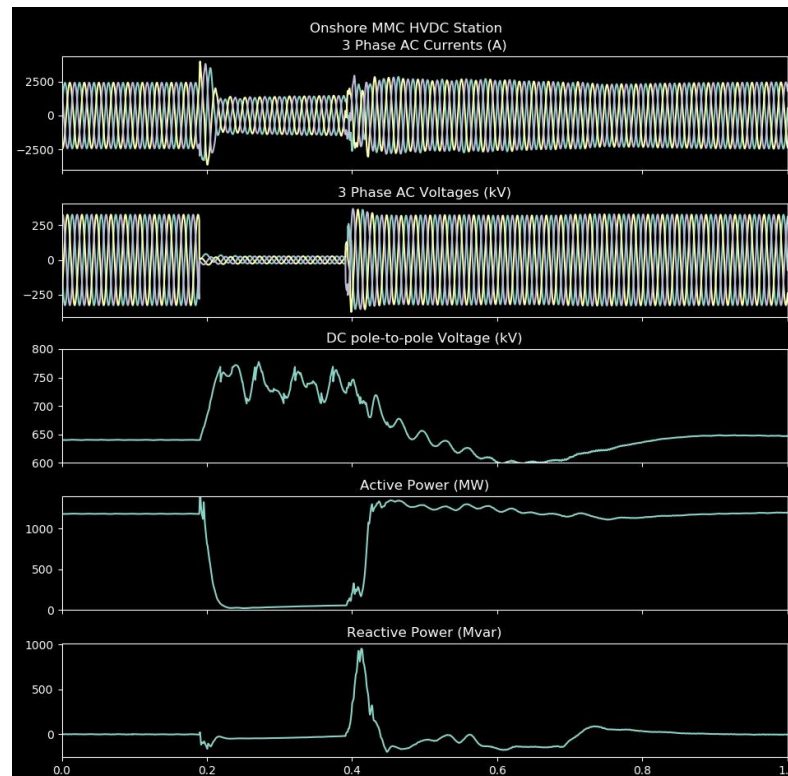
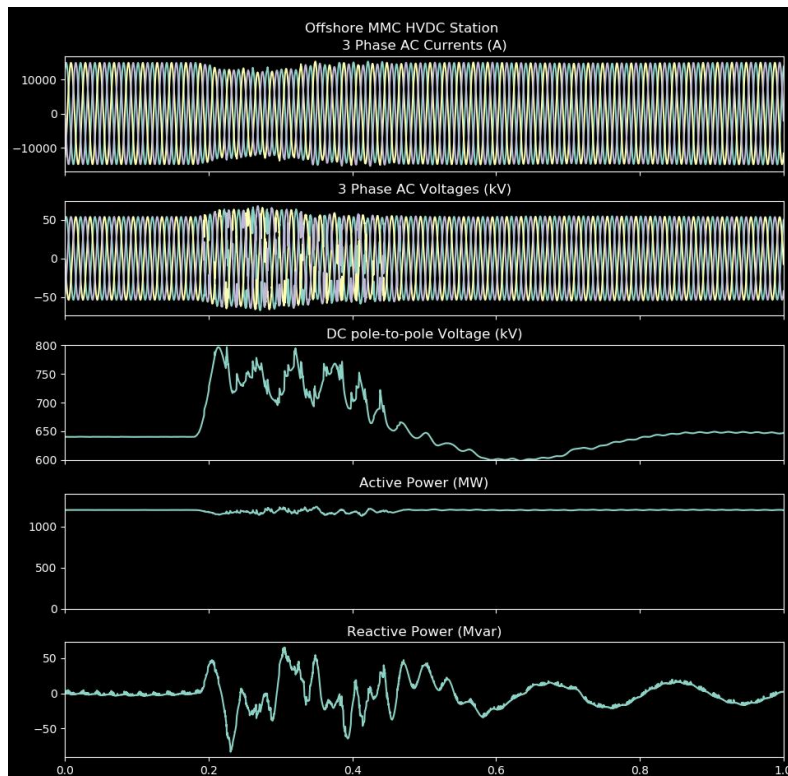


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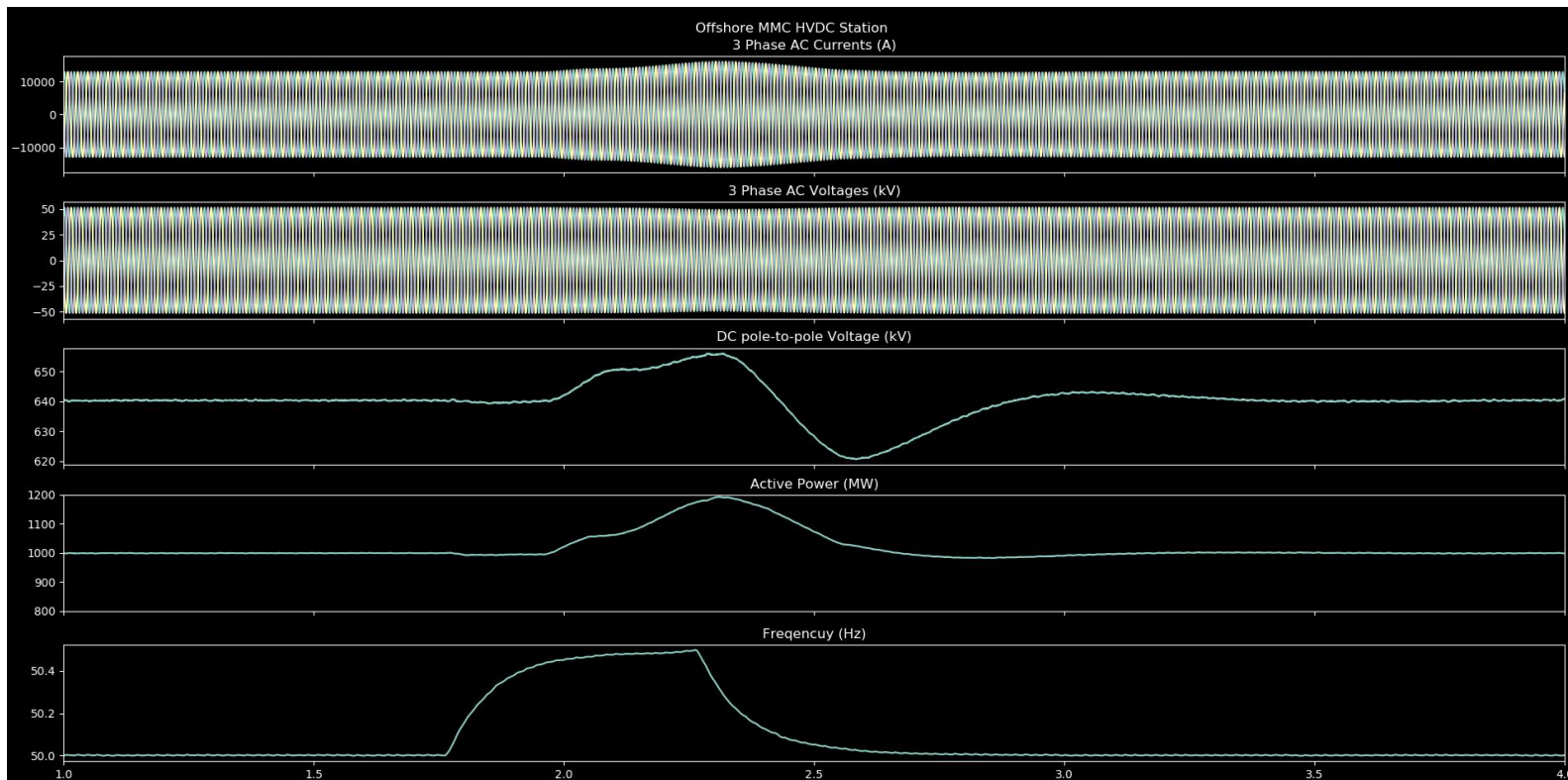
CHIL Measurement Results – Steady state 0MW



CHIL Measurement Results – Fault Ride Through



CHIL Measurement Results – Frequency Response



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