DC Fault Control and High-Speed Switch Design for an HVDC Network Protection Based on Fault-Blocking Converters

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***Abstract*—Future multi-terminal dc networks are envisioned for the large-scale integration of renewable energy sources into today's power systems. An essential aspect for the reliable operation of these systems is the fast and selective dc-side fault handling and separation of faulted lines. The objective of this paper is the development and evaluation of a multi-terminal dc protection strategy based on fault-blocking converters (e.g., full-bridge based modular multi-level converters) and high-speed switches. Both a suitable fault control and a new high-speed switch design for a fast separation of faulted dc lines are elaborated. The novel concept is intended to reduce the requirements on the high-speed switches compared to dc circuit breakers and to ensure a fast restoration of the active power transmission capability, as well as the dc voltage. The fault-clearing strategy is analyzed using electromagnetic transient (EMT) simulations under variation of the fault location, type, and resistance. The investigations are carried out in a cable-based multi-terminal HVdc system with full-bridge modular multi-level converters in symmetrical monopole configuration.**

***Index Terms*—HVdc transmission, fault protection, power system protection, switchgear, PSCAD.**

I. Introduction

WORLDWIDE and in particular in Europe, the progressive integration of renewable energy sources into the production portfolio causes increasing distances between generation and load centers of electric energy. As an example, 50–100 GW of offshore wind power shall be deployed in the North and Baltic Sea until 2030 in order to meet Europe's climate goals [1]. To meet these challenges high voltage direct current (HVDC) systems based on voltage source converters (VSC) are chosen as key components for the reinforcement of today's transmission systems [2]. State-of-the-art VSC-HVDC transmission is based on half-bridge Modular Multilevel Converters (MMC) primarily operated as point-to-point links. However, studies indicate that multi-terminal HVDC (MTDC) systems can increase the system's availability at lower investment and operational costs [3], [4].

Regardless of the technological, operational and economic motivation for future MTDC networks, several fundamental challenges are still under investigation, including the fast and selective separation of faulted DC lines, e.g., after an insulation breakdown of a cable. The conventional method used in today's point-to-point HVDC systems to clear DC faults on the AC side can result in significant system downtimes [3], which might not be acceptable for HVDC systems with several gigawatts of transmission capacity. Thus, a fast and selective separation of faulted lines is required.

The present focus of research and development to fulfill this requirement is on DC circuit breakers [5]. However, HVDC grid protection systems based on FBC fault blocking converters (FBC) are gaining more attention [5]–[8]. A first application of FBCs will be the German point-to-point system Ultranet, which is utilizing full-bridge MMCs. In a second stage it will be extended to a three-terminal DC network [6]. Moreover, several concepts of FBCs with reduced power losses compared to FB-MMCs, e.g., mixed cell MMCs and the alternative arm converter (AAC), are under investigation [9].

Due to the fault blocking and fault current controllability of these converters, DC grid protection systems based on FBCs can utilize DC circuit breakers with significantly reduced requirements and footprints [5], [7] or DC high-speed switches[1] (HSS) [6], [8] as fault separation devices at the line ends. For future HVDC networks, especially offshore networks, the component costs of full-size DC breakers as well as the costs associated with their footprint regarding weight and volume and their high-energy air-cored inductors may be a significant part of the total installation costs. Therefore, FBC based protection systems with low footprint HSS can be an alternative to HVDC circuit breakers [10]. This paper investigates the capability and enhances the performance of FBC based protection systems.

Concepts for the separation of faulted line segments in MTDC systems utilizing FBC based protection systems have already been presented in the recent past [5]–[8], [11]. However, the fault control methods used in these studies are adopted from

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[1]Disconnecting devices with a residual DC current interruption capability.

point-to-point systems [5] or are not discussed in detail [6]–[8], [11]. It has been shown that a selective fault control, specifically designed for FBC based protection systems, can reduce the overall fault separation time [12]. However, this method has not been applied to a complete protection system including fault separation devices and grid recovery yet. This selective control is applied, enhanced and investigated in more detail in this contribution.

Another unresolved issue is the identification and analysis of suitable fault separation devices for FBC based protection systems. Recent studies either use mechanical DC circuit breakers with a reduced energy absorption capability [5], transfer breakers [7] or generic HSSs [8], [11]. While the electrical behavior of mechanical DC circuit breakers is analyzed in [5], most contributions consider idealized switching devices, especially when transfer breakers or HSSs are utilized [7], [8], [11]. In this contribution, a new HSS concept is elaborated, which is particularly designed for FBC based protection systems. Whereas the fault separation devices used in other contributions are designed for current interruption under nominal voltage [5], [7], this work elaborates an HSS concept with significantly reduced requirements regarding the switches' voltage rating. Therefore, the fault control method and the protection sequence are optimized to facilitate the use of HSSs with reduced voltage ratings.

Previous investigations primarily focus on faults in effectively grounded bipolar systems [5], [6], [8] and on pole-to-pole faults in monopole systems [7]. Due to the isolated neutral point of symmetric monopole systems, pole-to-ground faults cause an unbalance in the DC pole voltages, which is considered in the design of a fault clearing strategy of this work [11]. Another important aspect in the analysis of DC protection concepts is the evaluation of the impact of DC contingencies on the resulting power outage in the adjacent AC systems [13]. To perform a comprehensive analysis, the entire fault clearing process including the restoration of the AC-side active power is taken into account.

After an outline of the relevant considerations of MTDC fault handling with FBCs and HSSs the main contributions are as follows:

- Design of a comprehensive fault clearing strategy for MTDC networks based on FBCs in combination with HSSs using selective fault control methods [12] including an enhanced recovery process for FBC based networks in symmetric monopole configuration.
- Elaboration of a novel combination of FBCs and medium voltage solid-state switch based HSSs. This includes an adaptation of the FBC based fault clearing sequence to the HSS concept.
- The description of the specific implementation of the fault clearing strategy in an exemplary MTDC system.
- Comprehensive simulation study and evaluation of the proposed concept based on previously defined key performance indicators (KPIs).

All investigations are based on a minimal meshed MTDC offshore network defined in the European Horizon 2020 project PROMOTioN.

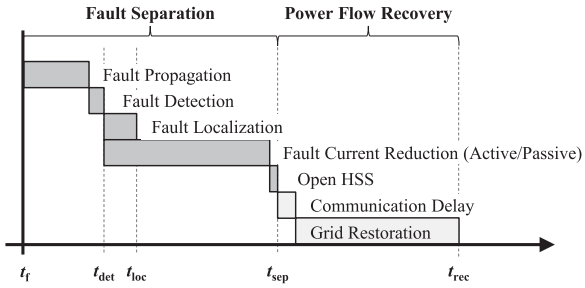

Fig. 1. Fault clearing sequence [12].

II. Fault Clearing in Multi-Terminal HVDC Systems

A. Requirements for MTDC Fault Clearing and KPIs

Future MTDC networks will have several requirements to fulfill under fault conditions. Besides protecting the network's components and ensuring human safety, a main objective of the protection system is to guarantee a stable operation of the AC grids surrounding the DC system [14]. Therefore, HVDC grids necessitate fast, reliable and robust protection systems. Additionally, DC line faults must be cleared selectively to reduce the loss of power transmission capacity. Another criterion for HVDC systems connected to electrically islanded wind parks is the resumption of power transmission after a maximum of 150 ms to prevent the wind turbines from disconnecting from the network [15]. Characteristic values for the evaluation of the overall system behavior in the event of a DC fault are the duration between fault inception and its separation, the duration between fault inception and DC voltage recovery as well as power flow recovery [13]. Consequently, the following KPIs with exemplary values are proposed to assess the protection strategy:

t_{sep}: Fault clearing time until all relevant fault separation devices (here HSSs) are opened.
$t_{\mathrm{P,rec}}$: Active power recovery within a $\pm 10\%$ tolerance band of the post-fault steady-state value.
$t_{\mathrm{V,rec}}$: DC voltage recovery within a $\pm 15\%$ tolerance band of the nominal DC voltage [16].

B. Fault-Clearing Strategy for MTDC Systems Based on Fault-Blocking Converters

Fig. 1 gives an overview of a DC fault clearing sequence with FBCs. After the occurrence of a DC fault at t_{f}, traveling waves propagate through the network. The protection relays, located at each DC busbar, detect the fault at t_{det} and initiate the fault handling process of the converters. The fault current flowing through the relevant HSSs can either decay passively, e.g., in case of FBC blocking, or can be reduced actively by controlling of the DC output current to zero (c.f. Section III-A.) [12], [17]. Simultaneously, the fault localization process commences. Protection relays at each line end select the corresponding HSSs on the faulted line. As soon as their opening condition is fulfilled, the HSSs separate the faulted line from the remaining DC network. A possible opening condition is the decay of the current flowing through a selected HSS below a preset

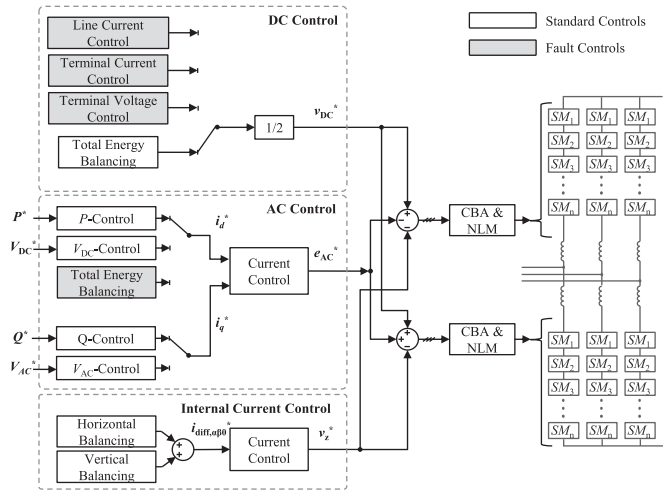

Fig. 2. Control concept for MMCs with fault controlling capability.

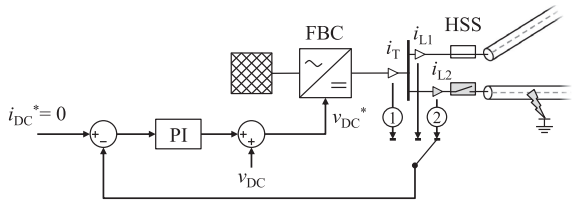

Fig. 3. Illustration of a selective fault current control.

interruption current i_{Int}. After the line separation at t_{sep} and a communication time delay, the recovery process of the DC voltage and the active power transmission starts [12].

C. Fault-Blocking HVDC Converters and Converter Controls

Several concepts of fault blocking VSCs for HVDC applications have been proposed in the past. The most established design is the Modular Multilevel Converter based on full-bridge submodules, which is used for the investigations of this work. However, the proposed protection concept could be applied to other FBCs like the Alternative Arm Converter (AAC) or mixed cell MMCs as well [9].

In contrast to fault feeding converters, which typically comprise half-bridge submodules based on two IGBTs, full-bridge submodules comprise four IGBTs. Therefore, the converter can block during DC faults and interrupt the fault current contribution from the AC to the DC system. Since most FBCs are able to set their DC voltage freely within their limits of $v_{\mathrm{DC}} = [-V_{\max}; V_{\max}]$, even during a DC fault, these converters can actively control their DC output current by adjusting the DC voltage [12], [17], [18].

D. Converter Control

A brief overview of the control concept of an MMC with fault blocking and controlling capability is depicted in Fig. 2. The control used in this paper is divided into an AC, a DC and an internal current control. The AC (grid) control is based on a cascaded vector control proposed by CIGRÉ WG B4.57 [19]. Depending on the reference orders (P, V_{dc}, Q and V_{ac}) the outer loop generates the reference currents of the current control, the inner loop, which generates the reference AC voltage of the converter $e_{\mathrm{AC}}{}^{*}$. The DC control regulates the power transferred through the converter via $v_{\mathrm{DC}}{}^{*}$ and ensures that the total amount of energy stored within the converter remains constant. An even distribution of the stored energy over all arms of the converter is ensured by the internal current control $v_{\mathrm{Z}}{}^{*}$, which comprises an inner current control and a horizontal and vertical energy balancing control as outer loop [20]. These three reference voltages determine the arm reference voltages of the converter. Based on these, firing signals for the IGBTs of the submodules are generated by a nearest level modulation (NLM) algorithm [19]. A capacitor balancing algorithm (CBA) ensures an even capacitor voltage distribution within each arm [19]. The overall control concept is illustrated in Fig. 2.

III. DC Fault Control

In case of a DC fault, the simplest approach to interrupt the fault current contribution from the AC to the DC side is to block the converter by blocking all its power electronic switching devices. Even though this method minimizes the energy input into the DC grid, a major drawback is that reactive power cannot be supplied continuously to surrounding AC systems in STATCOM operation mode [6], [12], resulting in a temporary stop in reactive power transmission [13]. In contrast to converter blocking, most FBC can actively regulate their DC current to zero by adjusting the DC output voltage in case of a fault [6], [12], [17], [18]. Due to the continuous operation, the converters can maintain their STATCOM function during DC-side faults.

A. Active Fault Current Reduction

As depicted in Fig. 2, the DC fault control substitutes the total energy balancing of the DC control in case of a DC fault. Since the DC voltage and active power transfer are now controlled via the DC fault control, the direct component of the AC reference current $i_{\mathrm{d}}{}^{*}$ can be used to control the total energy of the converter. If an HSS is selected to be opened, it is beneficial to selectively control the fault current through this HSS to zero. Thereby, the HSS current is reduced faster and the faulted line can be separated earlier [12].

The principle of the selective fault current control is illustrated in Fig. 3. ① After fault detection, the converter controls its terminal current i_{T} to zero. ② If a fault is localized on a line connected directly to a converter's busbar, this converter changes its fault control mode to line current control (here i_{L2}). The current through the relevant HSS is selected as input of the line current control. Once the opening condition of the HSS is fulfilled, it is triggered to separate the faulted line from the rest of the grid.

B. Recovery Method

In a DC grid in symmetrical monopole configuration, a pole-to-ground (PG) fault can result in a significant overvoltage up

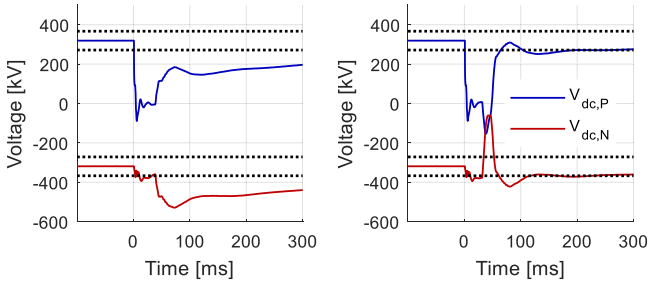

Fig. 4. Comparison of voltage imbalance after an exemplary PG fault without discharge (left) and with discharge (right) of the dc-grid.

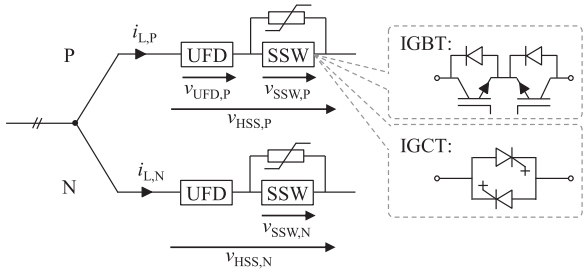

Fig. 5. Example of a solid-state based high-speed switch.

to twice the nominal voltage on the unaffected pole while the potential of the faulted pole is close to zero [11]. Even if the potential of the unaffected pole remains at its nominal level $v_{\mathrm{DC,nom}}$, due to fast protection actions or an overvoltage control, the imbalance between the poles causes an overvoltage at the unaffected pole during DC voltage restoration, as shown in Fig. 4 (left) for a PG fault on the positive pole.

To avoid such overvoltages and accelerate the system's performance regarding the DC voltage KPI (c.f. Section II-A.) an active discharge of the healthy pole is proposed. In contrast to passive discharge methods [11], which do not support a continuous operation of the converters, the DC terminal pole-to-pole voltage $v_{\mathrm{T,PP}}$ is controlled to zero by adjusting $v_{\mathrm{DC}}{}^{*}$ [12]. The total energy balancing is still controlled via the AC reference current $i_{\mathrm{d}}{}^{*}$ during this operation. The effect of discharging the healthy DC pole prior to grid restoration is depicted in Fig. 4 (right). The overvoltage on the healthy pole N as well as the voltage restoration time can be significantly reduced by this method.

IV. Novel DC High-Speed Switch Concept

After limiting the DC fault current on the affected line by controlling the FBCs, the current has to be interrupted by a residual current breaking device. Moreover, the faulted line segment has to be isolated from the rest of the DC network.

A. Requirements

Three main requirements are identified for high-speed switches, which are used as fault separation devices in combination with FBCs:

- A residual current must be interrupted rapidly to accelerate the fault clearing process and to minimize the influence of a DC-side fault on the active power transmission at the AC points of common coupling (PCC). Hence, the switch must provide a counter voltage, which is large enough to force the residual DC current to zero.
- The switch must withstand the transient interruption voltage (TIV) and absorb the stored residual energy of the circuit.
- After interruption, the HSS must build up an insulation capability against the full nominal DC voltage.

B. High-Speed Switch Design

To enable a rapid residual (DC) current interruption, an active switching device is required. The fastest interruption can be achieved by solid-state switches (SSW) such as IGBTs or IGCTs [21], [22]. This HSS design is depicted in Fig. 5. However, fast mechanical DC circuit breakers could be utilized as well. In this paper, the SSWs comprise two antiparallel strings of *n* IGCT modules connected in series, to enable a bidirectional current interruption capability. While power electronic DC circuit breakers must be able to interrupt the full fault current, the SSW in this application only has to conduct the fault currents and interrupt a much lower residual current, since the fault current is actively reduced by the FBCs. As a result, the requirements regarding energy absorption during the switching process and the TIV withstand capability are significantly lower compared to a full-scale DC circuit breaker. To limit the maximum TIV over the SSW a surge arrester is placed in parallel.

To isolate faulted lines the usage of an Ultra-Fast Disconnector (UFD) is proposed [23]. In an UFD a multi-segmented contact system driven by electromagnetic actuators in an SF_6 switching chamber enables a rapid switching process [23], [24]. Prototypes of this switch are able to isolate a DC voltage of $v_{\mathrm{UFD}} = 320$ kV within approximately $t_{\mathrm{open}} = 2$ ms [23]. However, the safe current interruption capability of a UFD is very limited (e.g., $i_{\mathrm{UFD,int}} < 1$ A) [23]. Once the UFD opens, it isolates the full voltage across the HSS. It should be noted that as long as the surge arrester is conducting, current flows through the UFD, which might exceed its current switching capability and thus prevent the UFDs from opening safely. In this case, the opening of the UFD must be delayed until the current through the surge arresters has decayed. Accordingly, when designing the HSS, the relationship between the current-voltage characteristic of the surge arrester and the maximum blocking voltage of the SSW must be considered.

C. Adaption of the Fault-Clearing Sequence to the HSS

The overall fault clearing sequence, which is designed for the HSS concept, is illustrated in Fig. 7. In addition to the sequence described in Section III-A., the HSS opening condition $i_{\mathrm{HSS}} < I_{\mathrm{Thres}}$ is added to the sequence. During the operation of the HSS, the voltage across the SSW should be limited to ensure that no current is flowing through the surge arrester and the UFD can open. The opening condition for the UFD should be smaller

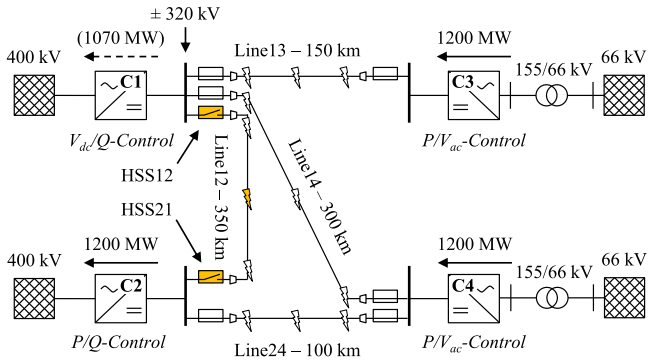

Fig. 6. MTDC network model with an exemplary fault at Line 12%–50%.

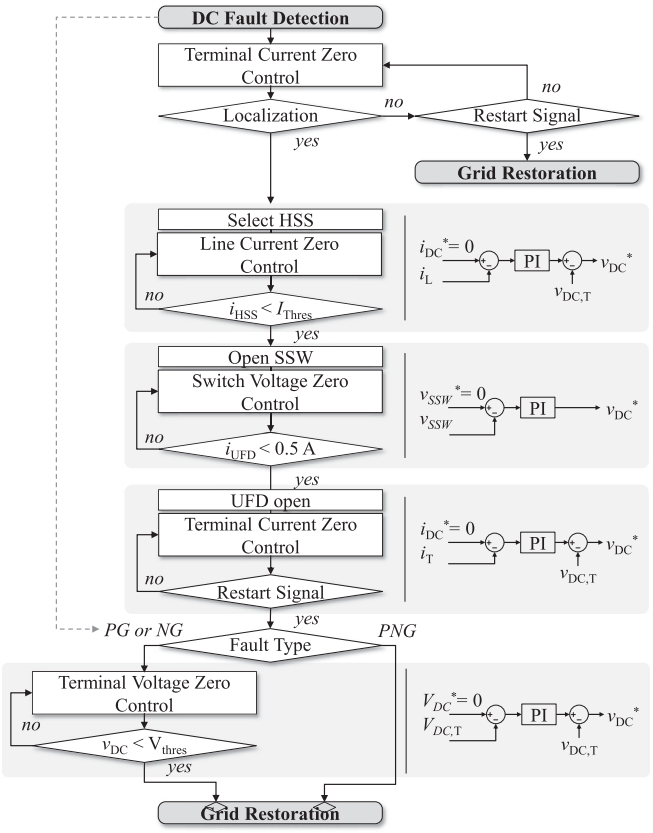

Fig. 7. Flow chart diagram of the fault clearing sequence.

than its safe interruption current (here $i_{\mathrm{UFD}} < 0.5$ A). Therefore, a switch voltage control is proposed, which actively limits the SSW voltage by adjusting the DC reference voltage of the upper and lower arms $v_{\mathrm{DC,P}}{}^{*}$ and $v_{\mathrm{DC,N}}{}^{*}$. This control is realized with a PI controller, as illustrated in Fig. 7. After the UFD is open, the control switches back to terminal current control. If the converter receives a restart signal, the recovery process described in Section III-B. commences. The restart signal could be based on local measurements or provided by a central grid control. Within this paper, a central communication unit, which is described in Section V-E., initiates the restart sequence.

TABLE I
CONVERTER SETTINGS

Converter Station Parameter		Setting
Rated power	S_{r}	1265 MVA
Rated active power	P_{r}	1200 MW
Rated DC pole voltage	$V_{\mathrm{dc,r}}$	± 320 kV
Rated AC voltage converter	$V_{\mathrm{ac,conv}}$	350 kV
Arm inductance	L_{S}	42 mH
Number of submodules per arm	n_{sm}	350
Rated submodule voltage	$V_{\mathrm{sm,r}}$	1.9 kV
Submodule capacitor	C_{sm}	8.8 mF
Output converter inductance	L_{DC}	10 mH

V. INVESTIGATED HVDC SYSTEM AND MODEL DESCRIPTIONS

Fig. 6 gives an overview of the investigated MTDC network, which was designed for DC fault studies in the PROMOTioN project. The model includes four MMCs, cables and switching devices as well as 400 kV AC sources representing a strong transmission grid and 66 kV AC sources representing wind power plants, which are connected to the offshore converters via transformers. All transient simulations are carried out in PSCAD|EMTDC with a time step of $\Delta t = 20\ \mu$s.

The transmission lines are modeled using a *Frequency Dependent Phase Model*. The cables are parametrized according to state-of-the-art 320 kV XLPE submarine cables with metallic screen. Assuming that the sheath and armor are regularly grounded, the concentric conductors of the cable are eliminated mathematically in the model. In contrast to MTDC networks protected by fast DC circuit breakers, no line inductances are needed for fault current limitation and selectivity.

A. Converter Model

All four converters are modeled as full-bridge MMCs in monopolar configuration. They are grounded via a high impedance star point reactor with $L_{\mathrm{Star}} = 5000$ H and $R_{\mathrm{Star}} = 5000\ \Omega$ [19]. The most relevant parameters of the converter stations are summarized in Table I. Each converter is modeled using a *Type 4 Detailed Equivalent Circuit Model* [19], in which all individual submodule switching states and capacitor voltages are represented. Therefore, the model is appropriate for DC fault studies [19].

B. HSS Model and Design

The HSS is modeled according to Fig. 5. The UFD is represented by an ideal switch, which is able to interrupt, if the current flowing through the device is smaller than $i_{\mathrm{UFD,int}} = 1$ A and its contact voltage is smaller than $v_{\mathrm{UFD,int}} = 4.8$ kV [23]. The opening time of the UFD, including a communication delay, is $\Delta t_{\mathrm{UFD}} = 2.5$ ms [23].

The dimensioning of the SSW depends on the required fault separation time. The shorter the permissible separation time, the higher the DC current interruption capability of the SSW must be. Since the amplitude of the interrupted DC current correlates with the TIV and the amount of energy, which needs

to be dissipated in the SSW's surge arrester, the DC current interruption threshold should be limited. This reduces the requirements on the SSW and the surge arresters. Within this work, a residual current interruption threshold of $I_{\mathrm{Thres}} = 100$ A is used as a base case. However, a variation of this threshold is investigated in Section VI-B.

A similar trade-off must be considered regarding the rated voltage of the SSW and its surge arrester. To reduce the number of semiconductors and thereby the switches' losses, the voltage rating should be small. On the contrary, this can increase the amount of dissipated energy in the HSS's surge arresters and thereby the separation time (c.f. Section IV-B.). As a base case, the SSW model comprises two antiparallel series connection of three IGCTs with a rated voltage of 6.5 kV [21]. The rated voltage of the HSS's surge arrester is set to $V_{\mathrm{SA}} = 15$ kV (at $i_{\mathrm{SA}} = 1$ kA). This design results in an on-state resistance of approximately $R_{\mathrm{HSS,on}} = 1.5\ \mathrm{m\Omega}$ and a power loss of 5.3 kW under full load per HSS [21]. Hence, the losses of the proposed HSS concept are lower than the losses of a load commutation switch of a hybrid circuit breaker [25]. Therefore, it is assumed that an air-cooled thermosyphon based cooling system could be sufficient for the proposed switch design [26]. A variation of the HSS's rated voltage is investigated in Section VI-B.

C. Protection Relays

Since all converters are involved in the fault current reduction process, the information, which line is affected, is not required instantaneously. Hence, fault detection and localization can be separated. Even though no line inductors are implemented, single-ended fault detection methods can be used. [12]. As very fast primary protection, a voltage derivative *dv/dt* protection is used. Both overcurrent and undervoltage relays are applied as backup protection. For signal processing and other possible delays, a conservative delay of $\Delta t_{\mathrm{det}} = 0.5$ ms is added to the protection signals. Several methods for fault localization are discussed in the literature. Within this paper, the simple approach of a line current differential protection is used for fault localization. This method is based on the comparison of currents at each line end. Thus, it does not require inductors at the line ends [5], [12]. However, the comparison of the currents requires communication between the relays of each line end.

D. Fault Scenarios

The evaluation of the protection concept is based on a systematic variation of fault scenarios within the DC network. Pole-to-ground[2] (PG) and pole-to-pole-to-ground (PPG) faults are examined at multiple locations, which are shown in Fig. 6, with different fault-to-ground resistances $R_{\mathrm{f}} = [0.1\ \Omega; 5\ \Omega; 10\ \Omega; 50\ \Omega]$[3] . For each line faults in the beginning (0%), middle (50%) and end (100%) are considered.

[2]Due to the symmetrical design, only ground faults of the positive pole are considered regarding pole-to-earth faults.

[3]These values are used for the performance analysis of the fault clearing strategy and do not intend to reflect realistic fault resistances.

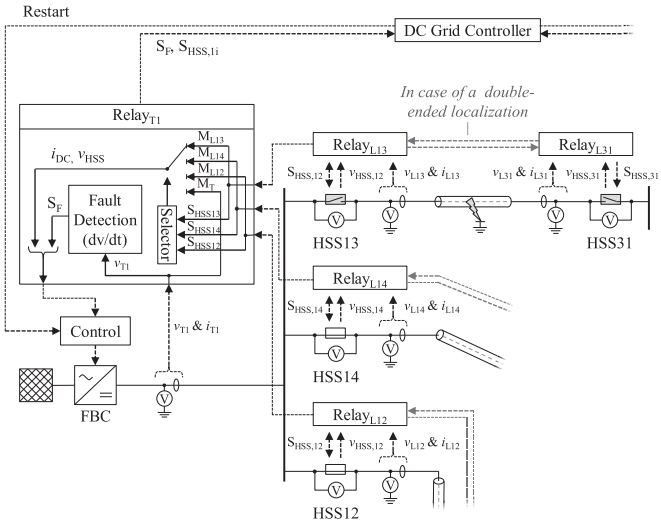

Fig. 8. Illustration of the communication system for terminal C1.

E. Communication System and DC Measurements

The architecture of the DC terminals is described based on an example of the DC terminal T1 of Fig. 6, shown in Fig. 8. The terminal comprises DC current and voltage sensors at every line end and between the converter and the busbar, HSSs at every line end and protection relays. In this work, a distributed relay structure is applied, which includes a terminal relay and line relays at every line end.

The terminal protection relay, which receives the DC terminal measurements, acts as a master protection relay and has two major functions: fault detection based on local measurements ($\mathrm{S_F}$) and handling of the control values of the fault control (i_{DC} & v_{HSS}). The line relays receive the DC measurements at every line end, the HSS voltage and the HSS status. In this work, a double-ended method is used for fault localization. Hence, the two relays of each line communicate with a delay based on a communication velocity of optic glass fiber cables of $v_{\mathrm{com}} = 150$ km/ms [8]. The localization signal $\mathrm{S_{L,ij}}$, the HSS status $\mathrm{S_{HSS,ij}}$, and the relevant measurements (here: i_{Line} & v_{HSS}) are forwarded to the terminal relay.

In this work, the restart of the system is coordinated via a central DC grid controller located at converter C1. The communication between the individual terminals and the master controller is realized via the shortest path along the DC cables with communication delays based on v_{com}. The restart signal is sent to the converters C1–C4 after the grid controller receives the information that all relevant HSSs are open.

To respect the non-ideal measurements of the DC sensors, the DC current, DC voltage and HSS voltage measurements are distorted with a white noise of $\delta_{\mathrm{I,DC}} = 0.1\%$, $\delta_{\mathrm{V,DC}} = 0.4\%$ and $\delta_{\mathrm{V,HSS}} = 0.4\%$ of their rated values. This reflects the typical accuracies of zero flux transducers and DC voltage dividers. To increase the accuracy of the HSS voltage measurement, it is measured across the SSW, as shown Fig. 8. The rated voltage of the sensor is assumed twice the HSS's surge arrester voltage.

VI. Simulation Results

First, an exemplary fault scenario is presented and discussed to demonstrate the fault clearing process. Therefore, a low impedance PG fault in the middle of line 12 is presented. A PG fault is chosen for the demonstration since this type is considered significantly more frequent than PPG faults for cable systems. Moreover, it represents the critical fault scenario for symmetric monopole configurations with regard to DC voltage imbalance and DC overvoltages [11].

A. Exemplary Fault

Fig. 9 shows the DC output voltage and current as well as the AC side active and reactive power flow of all four converters. The PG fault occurs at $t_{\mathrm{F}} = 0$ ms causing a voltage collapse on the positive pole across the entire DC network. Hence, all converters feed into the grid until the fault is detected and the fault clearing strategy commences. First, all converters reduce their DC output current to zero using the terminal current control. As soon as the fault is located, C1 and C2 switch to line current control of L12, which causes the rise in their DC output currents. At $t_{\mathrm{sep,L12}} = 18$ ms the faulted line L12 is separated by all four HSSs.

After fault separation at C2 and a subsequent communication delay of $t_{\mathrm{delay}} = 5$ ms the recovery sequence commences. As part of the recovery sequence, the DC grid is discharged by all converters to $|v_{\mathrm{DC,P}} + v_{\mathrm{DC,N}}| < 0.15\ V_{\mathrm{dc,r}}$ before the voltage and power flow recovery is initiated. During the fault, all converters continue to provide reactive power to the adjacent AC grids. The active power flow is considered to be recovered at all converter stations after $t_{\mathrm{rec,P}} = 100$ ms. Due to the line discharge (c.f. Section III-B.), the voltage recovers to the defined $\pm 15\%$ tolerance band within $\Delta t_{\mathrm{discharge}} = 108$ ms. However, since the remaining balancing takes place via the high impedance grounding of the converters, the DC voltage takes hundreds of milliseconds until the imbalance recedes completely.

Fig. 10 shows the voltages across and currents through $\mathrm{HSS}_{12,\mathrm{P}}$ and $\mathrm{HSS}_{12,\mathrm{N}}$ as well as the control mode changes of converter C_1 during the fault clearing process. First, a significant current increase on the positive pole is observed following the fault inception, caused by the discharge of the cable capacitances. After fault detection, the converter operates in line current zero control with the control value i_{T1} ① Subsequently, the relays of line L12 localize the fault and the fault control mode of C1 changes to line current zero control with the control value $i_{\mathrm{line,12}}$ ② Caused by the line discharge process as well as the line current control of the converter C1 the current through the HSS is reduced below $I_{\mathrm{Thres}} = 100$ A. Once this is detected by the line relay L12, the switches $\mathrm{SSW12}_{\mathrm{P;N}}$ open and the fault control changes to switch voltage control with the control value $v_{\mathrm{HSS,12}}$ ③ Caused by the current interruption, TIVs occur across the SSWs. These are limited by the surge arresters and subsequently suppressed by the switch voltage control. Since the HSS current is very close to zero, the UFDs open. After the UFDs' opening delay of $t_{\mathrm{UFD}} = 2.5$ ms the voltage appears across the UFDs.

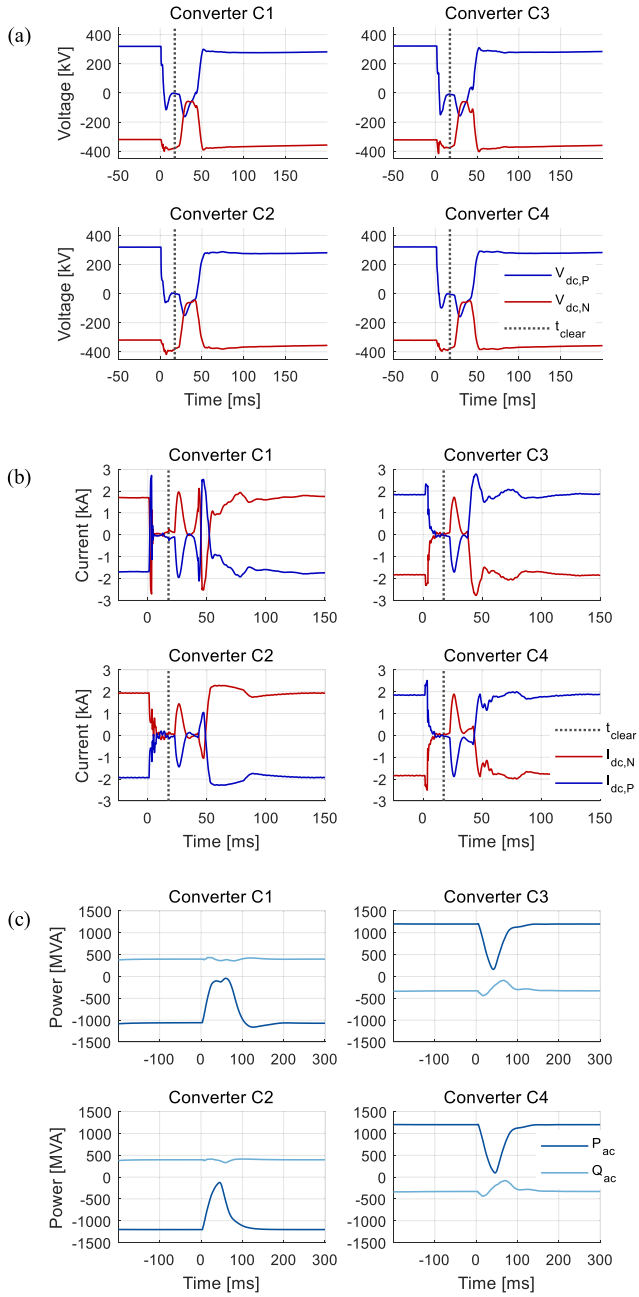

Fig. 9. (a) DC voltage, (b) DC current, and (c) active/reactive power at the AC-PCCs of all four converters for an exemplary PG fault.

After the line relay receives the open-states of the UFDs, the control switches back to terminal current zero control ④ Once the DC grid controller receives the open-status of both HSSs, it sends the restart signal to the converters. Since this is a PG fault, the converter C1 first discharges the grid via the terminal voltage zero control ⑤ until $|v_{\mathrm{DC,P}} + v_{\mathrm{DC,N}}| < 0.15\ V_{\mathrm{dc,r}}$ before the voltage recovery process commences.

B. Overall Simulation Results, KPI Analysis, and Parameter Variation

To evaluate the protection strategy, the defined KPIs are evaluated for all fault scenarios described in Section V-C. Fig. 11

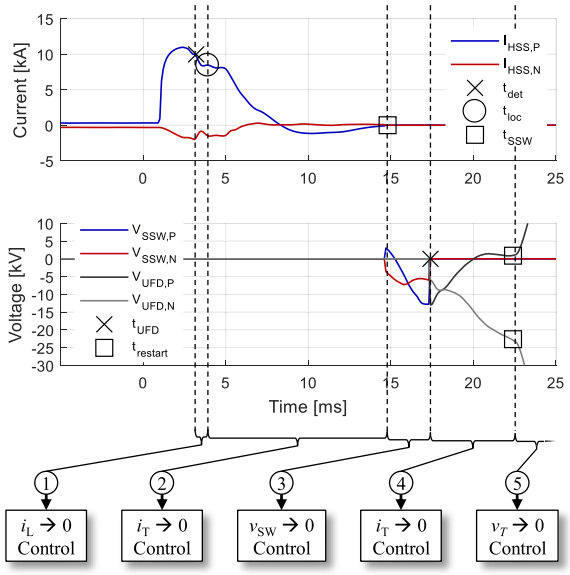

Fig. 10. Current and voltage stress of HSS12 for exemplary PG fault.

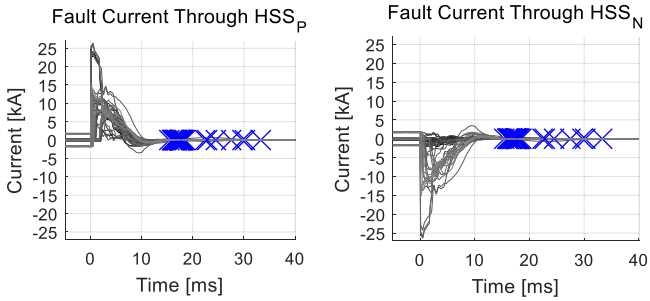

Fig. 11. Current flow through HSSs for all fault locations during all faults with the base case parameters; switching instances indicated by (x).

depicts the fault current through the HSSs of the positive and negative poles as well as the separation times of the respective UFDs for all fault scenarios with $R_F = 0.1\ \Omega$. All switches trip within a time frame of $t_{sep} = 15 \ldots 31$ ms after fault inception. The highest fault currents occur for faults in direct proximity to converter C1 (fault locations: L12-0, L13-0, L14-0), as three cables are connected to this terminal. The maximum current flowing through the HSSs is $I_{HSS,max} = 25.7$ kA. Since these high surge currents only need to be conducted, but not interrupted by the SSWs, the usage of IGCTs, which have very high on-state surge current capabilities, is feasible. Alternatively, a parallel connection of state-of-the-art StakPack[4] IGBTs, similar to the load commutation switch of a hybrid DC breaker [25], can be suitable as well. If a reduction of the HSS surge current is required, fault current limiting reactors can be inserted in series with the HSSs.

An overview of the defined KPIs and the surge arrester energy under variation of the fault resistance is summarized in Fig. 12(a). The maximum values of the KPIs are: Fault separation $t_{sep,max} = 41$ ms, power recovery $t_{P,rec,max} = 129$ ms

[4]Based on a correspondence with ABB Switzerland Ltd. an on-state surge current capability of approximately $I_{ON,Surge} \approx 4 \cdot I_n$ is assumed.

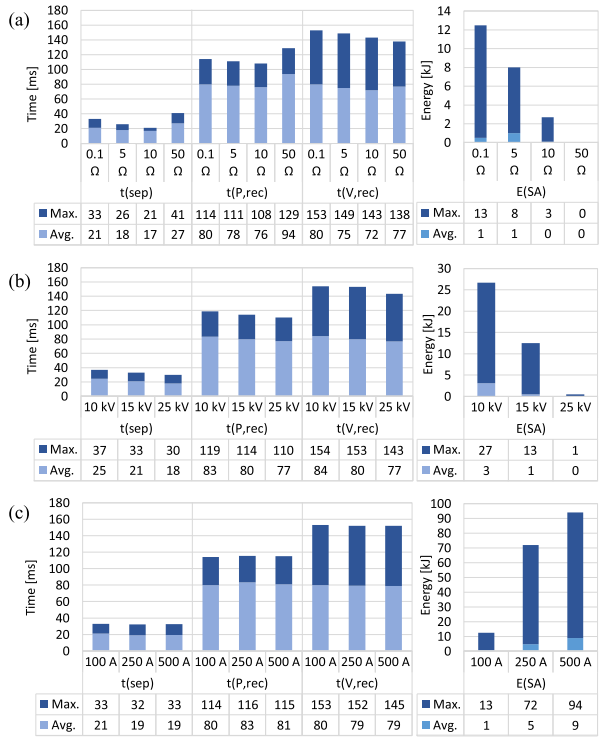

Fig. 12. Maximum and averaged KPIs and surge arrester energy under variation of (a) the fault resistance R_F, (b) the SSW voltage v_{SSW}, and (c) the current interruption threshold I_{Thres} (base case: RF $= 0.1\ \Omega$, $v_{SSW} = 15$ kV and $I_{Thres} = 100$ A).

and voltage recovery $t_{V,rec,max} = 153$ ms. Up to fault resistance of $R_F = 10\ \Omega$, the KPIs improve with an increasing fault resistance, since the increased damping of the fault current loop reduces the overshoot of the HSS current. Hence, the HSSs separate the faulted line earlier. The reduced separation time also causes a small reduction of the recovery times for higher high-impedance faults. The maximum absorbed energy of the HSS surge arrester is $E_{SA,max} = 13$ kJ and occurs during a low-impedance fault, which can be explained by the minimal damping as well.

In case of high-impedance faults (here $R_F = 50\ \Omega$), the fault separation time and consequently the power restoration time increase, due to the delayed fault detection and the reduced discharge of the DC grid through the high-impedance fault location. In this case, the line current and the DC grid voltage is almost completely reduced by the FBCs. To achieve the reduction of the line current, the cable capacitances are discharged by the converters. The converters discharge the positive and negative pole equally. Hence, the need for the active discharge of the healthy pole (c.f. III.B.) and the voltage recovery time is reduced. In case of even higher fault impedances, the separation time and power restoration time do not increase further, since the grid discharge is almost completely realized via the converters.

The influence of the SSW voltage on the KPIs of all fault scenarios is illustrated in Fig. 12(b). An increase in the SSW voltage slightly reduces the KPIs but has a significant influence on the energy dissipated in the HSS's surge arresters. The increase of the HSS voltage enables a fast current interruption. Hence, less energy is dissipated in the switches surge arresters.

Fig. 12(c) depicts the variation of the current interruption threshold I_{Thres}. It is shown that an increase of I_{Thres}, which causes the HSSs to open earlier, does not automatically result in an overall reduction of the KPIs. This is caused by the correlation between the HSS counter voltage and the interrupted current, which is explained in Section IV-B. Consequently, the energy dissipated in the surge arresters increases with the interrupted current. On the contrary, the current interruption threshold should not be too small, since the time to control the HSS current below I_{Thres} would increase significantly [12]. For the HSS base configuration of this work, a threshold of I_{Thres} 100 A provides a relatively low level of dissipated energy and a short overall fault clearing time.

To evaluate the stress imposed on the converters during fault clearing, the maximum arm currents and capacitor voltages are observed during all investigated fault scenarios. The maximum converter arm current is $i_{\mathrm{arm,max}} = 2.7$ kA and the maximum submodule voltage is $v_{\mathrm{c,max}} = 2.47$ kV, which are factor 1.23 and 1.2 of their maximum peak values during normal operation. Thus, it is concluded that the proposed fault clearing strategy does not stress the converters beyond their limits if the fault control is designed well.

VII. Conclusion

Within this paper, a protection concept for the separation of faulted lines in multi-terminal HVDC systems based on fault blocking converters is elaborated and analyzed in a meshed HVDC network in symmetrical monopole configuration. It is shown that an HSS especially designed for the application, which has significantly reduced requirements on its DC current interruption capability and counter voltage compared to full-scale DC breakers, is sufficient for the separation of faulted DC lines. An advantage of the concept is that no additional line reactors are required as part of this fault clearing strategy, since the HSS only have to conduct, but not switch the high fault currents. The simulation results indicate that an HSS based on a combination of a solid-state switch (e.g., a series connection of three IGCTs) and an ultra-fast disconnector is well suited as HSS for the isolation of faulted line segments.

Current regulations and standards do not include specified constraints regarding the power flow recovery time after DC faults, besides that the AC system stability shall not be endangered. For the connection of offshore wind farms a maximum outage of the DC network of 150 ms shall not be exceeded [15]. The investigated protection concept fullfills this requirement. The protection strategy does not cause blocking of the converters, but a temporary stop in active power at the AC-PCCs (in this network $\Delta t_{\mathrm{P,rec}} < 129$ ms), while reactive power can be controlled continuously [13]. The impact on the AC system stability of a temporary stop strongly depends on its strength and the total transmission capacity of the DC system. As long as this temporary stop in active power does not endanger the AC system's stability, it is concluded that the protection strategy presents a viable alternative to protection concepts based on DC circuit breakers.

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