Experimental Investigation of Electrical Stresses on the Main Components of HVDC Circuit Breakers

Nadew A. Belda, *Member, IEEE,* René P. P. Smeets, *Fellow, IEEE,* and Roy M. Nijman

***Abstract*—Recently a number HVdc circuit breakers (CBs) based on various dc current interruption principles have been developed and a few are put in operation. However, due to a lack of practical experience, no clearly defined requirements that the HVdc CBs should satisfy exist. To define and refine justified test requirements, a thorough understanding of the interactions between the internal components of the HVdc CB and the stresses on these components under real dc fault current interruption condition is necessary. In this paper, an experimental dc CB based on the active current injection technique is setup in a high-power laboratory to investigate the performances of the main components; namely, the vacuum interrupter (VI) and the metal oxide surge arrester (MOSA). The performances of three different designs VIs are investigated and it is found out that each of the VIs behave completely different. The key parameters having impact on current interruption performance of the VIs are identified and analyzed in detail.**

Moreover, the performance of a MOSA, designed for HVdc CB application, is also investigated by applying energy per volume ranging between $70 - 220\ J/cm^3$ at temperature as high as $250^{\circ}C$. In order to find out the performance limit of the MOSA for this application, successive high-energy tests are performed until electro-mechanical failures occur in the MO varistors. Various failure modes such as fracturing and puncture are observed. The detailed analysis of these failure mechanisms during destructive tests and the root causes are presented.

***Index Terms*—Active current injection, HVdc circuit breaker, HVdc CB Testing, Metal Oxide Surge Arrester (MOSA), Test Circuits, Test Requirements, Vacuum interrupter**

I. Introduction

HIGH-voltage dc circuit breakers (HVdc CBs) are expected to play an important role in the protection of multi-terminal and meshed HVdc grids [1]. Several concepts of HVdc CBs have been proposed and some are prototype tested [2]–[6]. A few cases have been put in service in radial multi-terminal VSC-HVdc pilot projects in China [7]–[9].

The use of HVdc CBs at the ends of transmission lines enable selective clearing of dc line faults whilst ensuring uninterrupted power flow in the healthy part of the grid. The requirements of the HVdc CBs are, ultimately, determined by the functional specification of the HVdc project in which they are installed. For example, for Zhangbei project (a 4-terminal $\pm$ 500 kV meshed HVdc grid under construction in China), a fault neutralization time of 6 ms, within which the HVdc CBs are expected to clear dc line fault current as high as 20 kA, is defined [10]. The progresses in the developments of the power electronic components have enhanced fault-ride-through capability of HVdc converters. In this regard, the HVdc CBs are expected to clear the dc line fault preferably before any of the converters or at most only one converter close to the fault location blocks [11]. Moreover, when overhead lines are used, the HVdc CBs are required to re-close and re-open after current interruption; thus, putting extra requirement on the energy absorption capability among other stresses. These requirements necessitate adequate testing and verification of the HVdc CBs before installing in the grid.

So far the testing of HVdc CBs focuses on the proof of a concept such as verifying internal current commutation and the transient interruption voltage (TIV) generation. However, in service, the HVdc CBs are subjected to much more stresses than just these. The important stages of the fault current interruption process that the HVdc CBs need to demonstrate are described in [3]. Four critical current interruption stages are identified−Internal current commutation, TIV generation, system energy absorption and dc voltage withstand during and after current suppression. Hitherto the challenge of testing the HVdc CBs has been two-fold. Firstly, no international standards specifying test requirements exist. Secondly, no test circuit capable of supplying adequate and complete stresses to the HVdc CBs is used at this stage of development. In view of this a CIGRE (International Council on Large Electric Systems) joint working group (JWG) A3/B4.80 is established to provide realistic guidelines regarding technical requirements, stresses and testing methods of HVdc CBs based on recent progresses made in the HVdc CB technology, ongoing demonstration projects as well as recent operational experiences.

Nevertheless, a thorough understanding of the interactions of the internal components of HVdc CB and the stresses on these components under realistic current interruption condition is necessary in order to define and refine justified test requirements.

To investigate this, an experimental dc CB based on active current injection technique is set-up in a high-power laboratory. The experimental dc CB utilizes VIs of commercial medium voltage (MV) ac vacuum circuit breakers (VCBs) as the main interrupter. The performance of three different designs of VIs are investigated. A test circuit based on ac short-circuit generators capable of supplying a range of stresses on HVdc CB is used. The detail of the test circuit has been discussed in [3]. Using this test circuit, the performance of the main components, namely, the vacuum interrupter (VI) and the metal oxide surge arrester (MOSA), which are common to most technologies of HVdc CBs are investigated. More than

This project has received funding from the European Unions Horizon 2020 research and innovation programme under grant agreement No 691714.

The authors are with KEMA Labs, Klingelbeekseweg 195, 6812 DE Arnhem, the Netherlands, e-mail: nadew.belda@kema.com, rene.smeets@kema.com, roy.nijman@kema.com

200 high-energy tests, in which over 850 current zero crossings (CZCs) are created, have been performed under various test conditions to identify the critical parameters having an impact not only on the performance of these components but also on the overall performance of a dc CB.

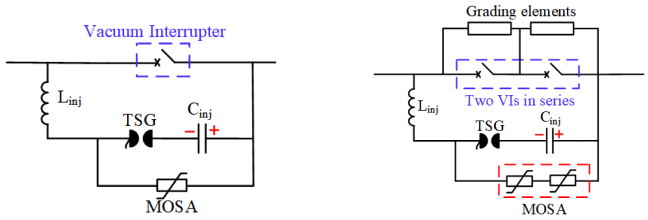
The remainder of the paper is organized as follows. In Section II, the design detail of the experimental dc CB along with its configuration and technical specification is presented. The actual test results of the three VIs are analyzed in detail in Section III. The stresses on MOSA are discussed in Section IV together with a brief description of the design of MOSA for HVdc CB. Finally the conclusions based on the results of the paper are presented in Section V.

II. Design Detail of the Experimental dc CB

A. Configuration and Components of Experimental dc CB

The electrical diagrams of a single interrupter and a double interrupter experimental dc CB are shown in Fig. 1a and 1b, respectively. The main components are; a VI or series connected VIs in the main current path, a pre-charged capacitor (C_{inj}) which supplies a counter injection current for current zero creation, an inductor (L_{inj}) in the current injection path which is used to limit the frequency and the peak value of the injection current, the triggered spark gap (TSG) that serves as a high-speed making switch and finally the MOSA, which is a crucial component for limiting and maintaining the TIV across the dc CB during current suppression and hence, absorbing the energy in the circuit. For the double interrupter setup (see Fig. 1b), there are voltage grading elements (capacitors are used in this project) across each VI to ensure equal TIV distribution during current interruption process. Proper dimensioning of these grading capacitors is essential for voltage sharing between the two VIs; otherwise unequal voltage distribution leads to cascaded re-ignitions of the VIs and ultimately to a failed current interruption.

In the diagrams depicted in Fig. 1a &1b, the MOSA is connected in parallel with the C_{inj}. Alternatively, it could be connected directly in parallel with the VI(s) as well; however, this results in a high-frequency transient voltage superimposed on the TIV during current commutation from L_{inj} into the MOSA. This is because by the time the C_{inj} is charged to the clamping voltage of the MOSA, the system current still flows through the L_{inj}. Since the commutation of current from a reactor cannot be instant, the C_{inj} keeps charging until the current commutation from the L_{inj} is completed; meanwhile the voltage across the C_{inj} stresses the VI(s). Therefore, to reduce the voltage stress on the VI(s) due to the transient overshoot during current commutation process, the design shown in Fig. 1 is chosen. In this case there is no need of current commutation from the L_{inj} during the entire current suppression period. Moreover, the more compact the loop between C_{inj} and MOSA is, the less the transient oscillation is. The design detail of the MOSA for HVdc CB application is described in Section IV. Fig. 2 depicts the photo of the laboratory test setup of the double interrupter experimental dc CB with the main components as labeled.



(a) Single Interrupter (b) Double Interrupter

Fig. 1: Electrical diagram of experimental dc CB

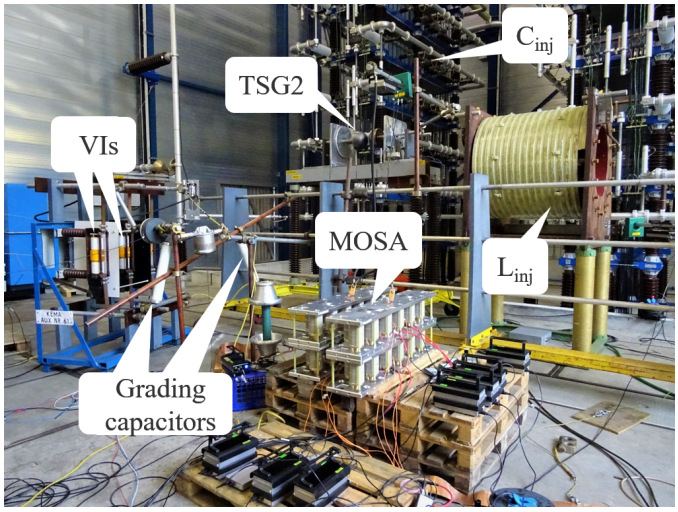


Fig. 2: Laboratory test setup of experimental dc CB

B. Technical Specification of the Experimental dc CB

The performance of a VI at different stages of the current interruption process depends on the contact design; shape and size, contact materials and composition, arc control mechanisms, etc. [12]. In order to investigate the impact of the VI contact design on the dc fault current interruption performance, VIs of three different, standard off-the-shelf VCBs produced by various manufacturers (anonymous) are used. These are all three-phase ac CBs with ratings shown in Table I.

In order not to exceed the ac voltage ratings of the VCBs, which is in the range between $36 - 38\ kV_{RMS}$ (see Table I), the TIV (and hence the MOSA clamping voltage) of a single interrupter dc CB is set to 40 kV with transient peak as high as 45 kV. In order to double the voltage rating of the experimental dc CB, two VIs are connected in series and; to ensure the doubling of the TIV, two series connected MOSA modules are used as shown in Fig. 1b. Fig. 2 actually shows a photo of a double interrupter test setup. The rated interruption current is 16 kA for both cases. Nevertheless, the charging voltage as well as the values of the C_{inj} and L_{inj} are adjusted so that the electrical stresses per component remain the same as for the single interrupter case.

C. Design of Counter Current Injection Circuit

The design parameters for the injection circuit components (C_{inj}, L_{inj}) are:

- Amplitude and frequency of the injection current
- Charging voltage of the capacitor (V_C)

TABLE I: Specifications of VCBs used in the investigation

VCB Type	rated voltage (kV_{RMS})	rated current (A_{RMS})	rated short-circuit current (kA_{RMS})	opening time (*ms*)
A	38	2500	31.5	37.5
B	36	2500	40	46.6
C	36	2000	31.5	37

The amplitude of the injection current is designed based on the maximum current interruption capability of the dc CB while considering sufficient number of CZCs. The amplitude of the injection current is determined by the (pre-)charging voltage of the C_{inj} and characteristics impedance of the injection circuit. The pre-charge voltage is normally equal to the system rated voltage for which the breaker is designed. This simplifies the charging of the C_{inj} from the system dc bus. The injection current frequency should be large enough to create sufficient CZCs in quick succession (without jeopardizing the breaker operation time) while taking the d*i*/d*t* at CZCs that the VI can handle into account. Using the characteristic impedance and the desired injection circuit frequency, the values of C_{inj} and L_{inj} are determined. For the experimental dc CB in this paper, the pre-charge voltage for a single interrupter setup is 27 kV (calculated from 40 kV TIV using 1.5 factor). For 16 kA current interruption, the peak value of the injection current is set to 20 kA at frequency of 4-5 kHz. Thus, C_{inj} of capacitance 31.8 μF is used together with L_{inj} of inductance 49.5 μH (including stray inductance of connections) in a single interrupter setup. Due to inherent losses in the circuit, the current from the injection capacitor decays quickly while the system current keeps rising. This limits the number of CZCs that can be created during current interruption. Thus, in this project, the injection circuit parameters are selected so that at least 4 CZCs can be created during the high-current test.

III. Test Results: Stress Analysis on VIs

A. Test Procedure

The stresses seen by the VI(s) depend on the magnitude of the interruption current. For example, it may not necessarily mean that a low current interruption is less severe than high current interruption. In order to investigate the impacts of interruption current magnitude on the performance of VI(s), three test currents are defined as follows.

1) Low current -2 kA
2) Medium current-10 kA
3) High current-16 kA

In fact the impacts of several other parameters are investigated at each test. Tests are repeated 10 times by maintaining the parameters of interest, for example, the arcing duration the VI(s). A test current is supplied by ac short-circuit generators operated at 16.7 Hz power frequency as discussed in [3]. The detail of the test procedure and timing sequence has been discussed in [13]. An example of the prospective current produced during a test is shown in Fig. 3 along with different timing signals. The test object (the experimental dc CB) is operated in such a way that the contacts of the VI(s) are separated after the short-circuit current starts to flow. This means the VCB needs to be tripped at T_1, prior to the onset of the prospective current which is at T_2. The breaker opening time which is the duration from T_1 until T_3 is precisely known for the VCBs, see Table I. Therefore, the trip command can be precisely sequenced in reference to the moment of short-circuit application as illustrated in Fig. 3. At T_4 the counter current is injected from the C_{inj} at a frequency mentioned above.

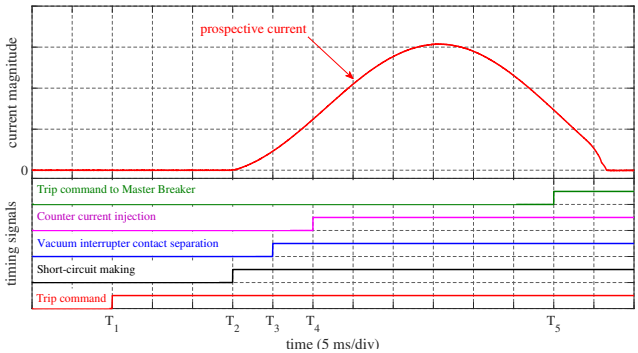


Fig. 3: Test method and procedure: prospective current and timing diagrams

B. Test Results of VI Type A

Fig. 4 depicts typical 10 kA current interruption by a single VI of type A. Current and voltage measurements near CZCs are shown in the zoomed plots. The contacts of the VI separate at T_3 followed by current conduction via vacuum arc. One of the crucial parameters determining the probability of current interruption is the *arcing duration* of the VI – the duration between the moment of contact separation until the 1^{st} CZC. It is related to the gap length between the contacts and hence, to the dielectric recovery of the VI, although the relationship to the latter is not linear [12]. Besides, during this period, the arc current might condition itself across the contact surface either by rotating or diffusing depending on the arc control mechanism, transverse magnetic field (TMF) or axial magnetic field (AMF), respectively. For the test result shown in Fig. 4, the arcing duration until the 1^{st} CZC is 2.9 ms even though the current interruption occurred at the 8^{th} CZC after a total of 3.7 ms arcing. This means the VI re-ignited during the first 7 CZCs. There are increasing (although not monotonic) re-ignition voltage spikes with alternating polarities seen in Fig. 4a. This shows that the VI is indeed attempting to interrupt the current at each CZC and dielectrically re-ignites.

The re-ignition voltage spikes observed at each CZCs are due to the charge remaining on the C_{inj} at the moments of CZCs, referred to as the initial TIV (ITIV). The rate at which the ITIV appears across the VI (d*u*/d*t*) is essentially determined by stray capacitor across the VI and; to a limited extent, by the injection circuit inductance. Thus, the ITIV is applied at extremely high d*u*/d*t* across the opening vacuum gap right after current zero. Normally this occurs before the residual arc plasma decays sufficiently. Given the very high d*i*/d*t* in this application, the plasma density at current zero may still be high, as recent post-arc current measurements

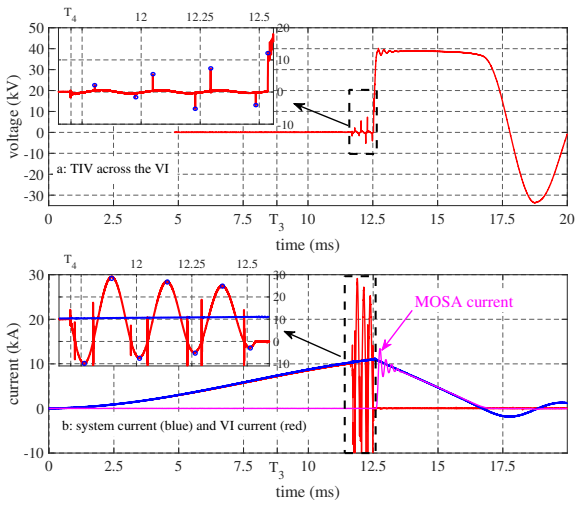


Fig. 4: 10 kA current interruption by VI of type A

have confirmed [2]. This residual arc plasma provides current conduction path and causes re-ignition. In reality, except at the 8^{th} CZC, the re-ignitions occur before the entire ITIV appears across the VI. Hence, it is not only the high d*u*/d*t* of the ITIV that determines the chance of re-ignition but also its magnitude. The impact of the latter become especially prominent when interrupting low current. The measured ITIV across the VI and the actual voltage across the capacitor are shown in Table II for comparison. The increase in the re-ignition voltage at successive CZCs is due to the increased contact gap and, at the same time, the decreased d*i*/d*t* near CZC. The latter is mainly caused by the decay in the counter injection current and, to some extent, by the slight increase in the system current. The lower d*i*/d*t* means the VI has more time for cooling of the arc.

From the zoomed portion of Fig. 4b, it can be seen that, because of superposition of the system current and the injection current, the current through the VI oscillates between high positive and low negative values (shown by blue circles at local peaks). This results in major loop and minor loop currents between successive CZCs and this has significant impact on the probability of a re-ignition at a CZC as well. In the classical theory of gas filled circuit breakers, there are two main causes for a re-ignition at a CZC; thermal and dielectric, the former being dominant after the major loop current flow. For example, the re-ignition at the 1^{st} CZC is entirely caused by thermal effect as there is no observable re-ignition voltage. At the 2^{nd} CZC, however, a re-ignition voltage of about 2.2 kV is observed. In general, recovery (thermal and dielectrical) can indirectly be observed by the increasing re-ignition voltage at each subsequent current zero crossing. The fact that reignition voltage is higher after a major loop than after a minor loop is an indication that recovery is more plasma dominated (or thermal) than voltage dominated (or dielectrical). The crucial parameters near CZCs including the major and minor loop current durations are shown in Table II.

From the moment of local current interruption at the 8^{th} CZC onwards, the system current is commutated to the injection branch of the dc CB, thus charging the C_{inj} until the

TABLE II: Parameters near CZCs during current interruption by a VI for the example case shown in Fig. 4

CZC number	1	2	3	4	5	6	7	8
di/dt $(A/\mu s)$	454	440	368	356	290	286	209	206
peak current[1]**(*kA*)**	10.1	9.8	29.2	7.2	27.2	5.0	25.3	2.7
loop duration (μs)	2890[2]	83.7	170	75.2	180	64.1	191	51.3
ITIV (*kV*)	Negl.	2.2	1.6	5.5	5.26	7.3	4	10.2
C_{inj} **voltage**[3]**(*kV*)**	22.5	21.5	18.6	17.5	14.5	13.7	10.5	10.2

[1] the peak value prior to a CZC
[2] arcing duration from contact separation till 1^{st} ZC
[3] actual voltage across C_{inj} at corresponding CZC

clamping voltage of the MOSA (the rated TIV) is reached. Once the TIV reaches the clamping voltage, the MOSA maintains a more or less constant TIV voltage, see Fig. 4a, until the system current is suppressed. Even if there is no thermal energy being injected into the VI contact gap at this stage, the VI must withstand the TIV during the current suppression and subsequently the system voltage after current suppression is over.

Nevertheless, it was observed on numerous occasions that this VI fails to sustain the TIV for sufficient duration after local current interruption. Henceforth, this kind of failure of the vacuum gap is referred to as a re-strike. In most of the cases a re-strike occurs before the capacitor is charged to the clamping voltage of the MOSA although the d*u*/d*t* of the TIV at this stage is relatively low compared to the d*u*/d*t* of the ITIV prior to this stage. At this point, the d*u*/d*t* of the TIV is dependent on the system current as well as on the capacitance of the C_{inj}. Moreover, due to the inherent behavior of the VI, in some cases a (late)restrike can occur even after sustaining the peak TIV. Fig. 5 shows a test result in which a late restrike occurred during current suppression period. As can be seen from the figure, the restrike happened about 1.2 ms after local current interruption. During this time, the system current has been suppressed by about 3 kA from its peak value. After the restrike the system current starts to rise again although the VI could clear before the system current exceeds the previous peak value. This is a unique feature of dc CBs based on current injection technique that a restrike may not necessarily lead to a complete failure to interrupt. The main impact of a restrike in this case is a longer total current interruption duration and an increased energy absorption in the MOSA. However, this is not always the case and the VI may not be able to clear after a restrike which was also observed on some occasions during the test campaign.

It can be seen from Fig. 5 that the oscillating current after the occurrence of the (late) restrike has a higher amplitude than before the restrike. This is because the C_{inj} is charged to the TIV which is normally 50% higher than the pre-charge voltage. Hence, the parameters near the CZCs including the d*i*/d*t*, the duration and the local peak values of the loop currents as well as the ITIV are also increased by (roughly) 50% compared to the corresponding values before the restrike. Moreover, the current interruptions (both before and after the restrike) tend to occur after minor loop currents (even numbered CZCs), see Fig. 6. In fact, for the VI type A, there are only a few cases where current interruption occurred on the 1^{st} CZC or after the major loop current. For example, among 98 tests, only 6 times the VI(s) could interrupt at the

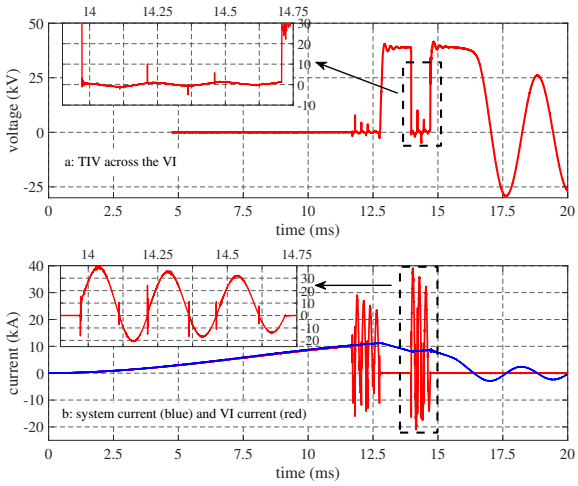


Fig. 5: Late restrike in the VI of type A during fault current suppression

1^{st} CZC. Of the remaining 92 tests, about 25% of the cases the VI(s) could clear on the 2^{nd} CZC whereas of the total 3^{rd} CZCs created only in less than 3% the VI(s) could interrupt. In general, a closer scrutiny of all the test results show that the re-ignition voltage is higher after minor loop current than after major loop current, confirming the lower stress to the gap during minor loop current flow.

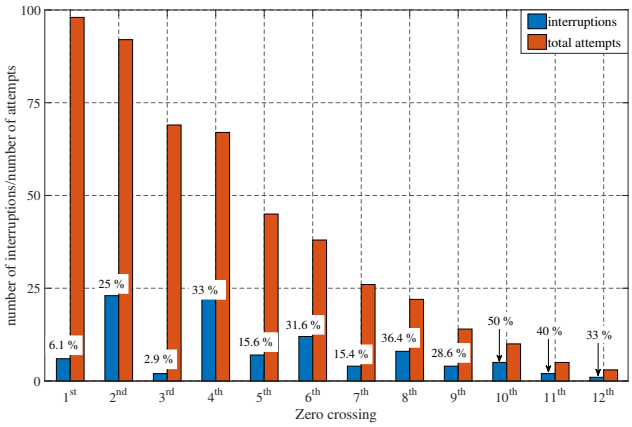


Fig. 6: Percentage of current interruption at a given CZC number

Another important observation is the impact of the rate-of-change of current (d*i*/d*t*) near CZCs. It is found that in no circumstance the VI of type A could clear when the d*i*/d*t* exceeds 620 $A/\mu s$ although up to 1000 $A/\mu s$ could be observed during the test campaign. Even though the recovery time of a VI is very short, it has a lower limit. Thus, when a CZ is created before the arc cools down sufficiently, it leads to re-ignition. In addition, the VI could clear only on a few occasions when the peak value of the current just before a CZC is larger than 20 kA. The latter is related to major loop current discussed before. The main conclusion here is that the probability of a re-ignition is determined not only by the d*i*/d*t* at a CZC but also by other parameters such as the total arcing duration, the duration and local peak of the current before that CZ. For example, at times the arcing duration was intentionally decreased to 1.5 ms and the VI of type A never interrupted at arcing times shorter than 2.9 ms prior to a CZC.

C. Test Results of VI Type B

Similar tests were performed using VI of type B while keeping the rest of the circuit components and the test parameters as for VI of type A. For type B VI, there is a slight dispersion in the moment of contact separation and hence, the precise control of the arcing duration is difficult. The performance of the VI of type B is, however, completely different than that of type A. For example, in about 75% of the tests the VI of type B interrupted the current at the 1^{st} CZC and, sometimes even at shorter arcing duration compared to the VI of type A. In about 16% of the tests, the VI failed to interrupt at all, more than half of which occurred during high-current tests on a single interrupter setup. For example, using a single interrupter setup, high-current test is performed 12 times of which 6 times the VI failed to clear even if the arcing duration until the 1^{st} CZC is prolonged to 3.5 ms and the total arcing duration until the last (4^{th}) CZC is 3.8 ms. Unlike the VI of type A, the performance of which improves along the number CZCs as illustrated in Fig. 6, the major attempt to clear by VI of type B is at the 1^{st} CZC. This is observed from all the failed interruption test results where the highest re-ignition voltage is seen at the 1^{st} CZC. In fact, there are attempts to clear on the later CZCs but the reignition voltages are much lower than at the 1^{st} CZC. Of all the tests in which reignition occurred, only in less than 10% of the cases the VI of type B could interrupt at later CZCs and there is no observable tendency to clear on an even numbered CZCs (after minor loop current) unlike the VI of type A.

A general observation from the failed interruption tests is that as the arcing duration until the 1^{st} CZC increases, the re-ignition voltage also increase. This confirms that the VI's dielectric strength and hence, attempt to clear improve with longer arcing duration. All the tests with arcing durations until the 1^{st} CZC longer than 3.6 ms resulted in successful interruption upon the 1^{st} CZC. The main conclusion from the test results is that, for a given rated interruption current, there is a minimum arcing duration that needs to be ensured before the CZ creation for the VI of type B.

Fig. 7 shows low-current interruption by double interrupters setup of type B VIs where 22 reignitions are observed. It can be seen that the most severe attempt to clear is on the 1^{st} CZC at which re-ignition occurred at ITIV of $-50\ kV$. After the re-ignition there is not significant attempt to clear until the 10^{th} CZC. From the 10^{th} CZC onwards, there is an increasing reignition voltage until the interruption occurred at the 23^{rd} CZC. The high reignition voltage observed at the 1^{st} CZC is due to the significant proportion of charge remaining on the C_{inj} when interrupting low current. This is the main cause of re-ignitions when interrupting low currents in addition to the high d*i*/d*t*. The former becomes critical for the double interrupter case especially when equal voltage grading across the VIs is not ensured.

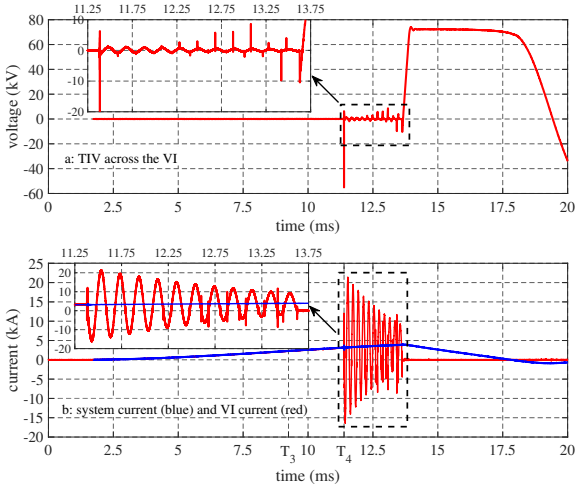


Fig. 7: Low current interruption by double interrupter of VI type B

D. Test Results of VCB Type C

Similar to VCB type B, VCB type C also has a slight dispersion in the opening time. For all the tests in which the arcing duration is in the range between 3.8−4.5 ms, the VI cleared on the 1^{st} CZC and no restrike was observed. However, when the arcing duration is in the range between 0.3−1.6 ms, restrikes were observed on a few occasions which finally led to failed current interruptions. Fig. 8 shows a test result in which a restrike occurred in the VI of type C. A critical observation in this case is that a restrike occurred not during the test with the shortest arcing duration, rather during a test with the longest arcing duration from the set i.e. 1.6 ms. The VI failed to clear after the restrikes even though up to 18 CZCs are created. In the test case shown in Fig. 8, the VI has been arcing for about 4.3 ms until the last CZC. This could have been sufficient for the VI of type A to clear. Similar phenomena that the VI(s) fail to interrupt once re-ignitions/restrikes occur are observed for the double interrupter tests of VI type C. In other words, this VI makes little attempt to interrupt the current after a re-ignition/restrike.

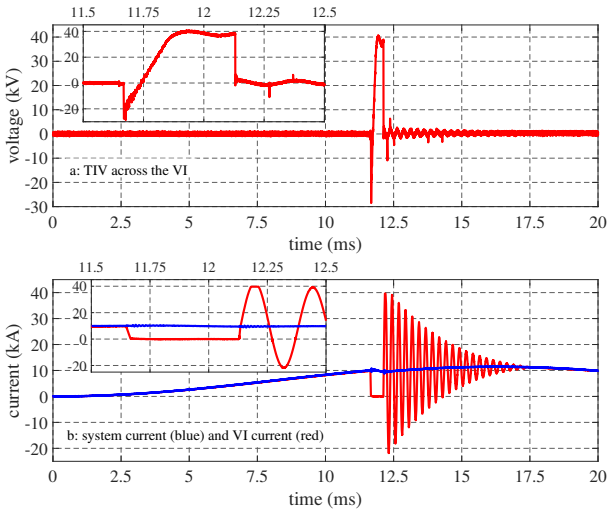


Fig. 8: Interruption failure after a restrike of VI type C

By far the main cause of re-ignitions/restrikes in the double interrupter setup is unequal TIV distribution. Initially, grading capacitors of 700 pF are put across each VI as shown in Fig. 1b. Evidently, this is not large enough to achieve equal voltage grading. Hence, the grading capacitors are increased to 2500 pF and this resulted in a reasonably equal voltage sharing between the two serially connected VIs. Then using the latter grading capacitors, series of tests are performed. For VI of type C, medium current tests are performed first with arcing duration in the range between 1.18−1.34 ms. In all the cases the VIs cleared at the 1^{st} CZC. Then, high-current tests are performed. In this case, a few failures to interrupt, mainly caused by extremely short arcing durations, were recorded.

The use of 2500 pF grading capacitors ensures more or less equal voltage distribution during the initial phase of the TIV generation. However, overall the use of only capacitive grading does not guarantee equal voltage sharing throughout the current suppression period. Nevertheless, even under equal voltage grading, a re-ignition or a restrike in one or both of the VIs can occur. Fig. 9 shows a test result in which a restrike occurs in one of the VIs during a high-current interruption test. In fact, this did not lead to a restrike of the overall dc CB because the second VI could sustain the entire TIV even if the TIV is maintained for about 10 ms. It can be seen that after the restrike the TIV slowly re-distributes across the two VIs. The main conclusion from the overall test results is that statistically better performance, compared to a single interrupter test setup, can be achieved by ensuring proper voltage grading in the double interrupter setup.

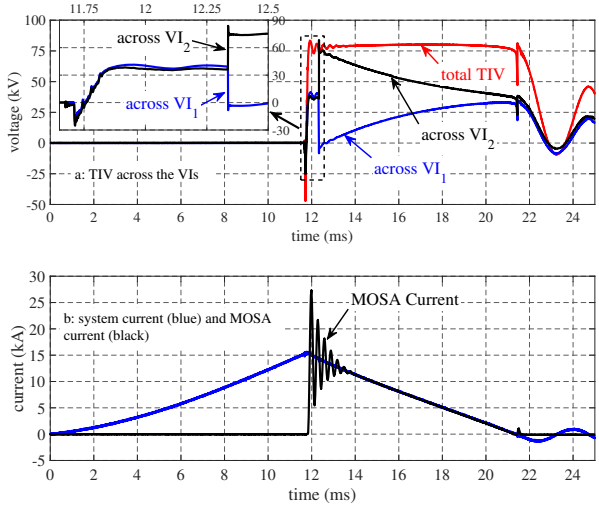


Fig. 9: Double interrupter test result showing a restrike in only one VI

The observations from the test results discussed in this section shows that there is a clear difference in performance of the three VIs used in this investigation. Very importantly, there is a clear difference between the VIs in the minimum arcing duration required for achieving current interruption. In addition, the VIs behave completely different during and after re-ignition or restrike occurs. For instance, these differences could be attributed to design differences among which is the

arc control mechanisms[1]. VI type A has TMF contacts whereas VI types B and C have AMF contacts.

IV. Test Results: Stresses on Metal Oxide Surge Arrester (MOSA)

The other key constituent of all HVdc CB technologies, which is subjected to unique stresses during dc current interruption, is the energy absorbing component i.e. the MOSA. In HVdc CBs, the MOSA is designed to serve two main functions; clamp and maintain the TIV to a desired level, and absorb the system energy during current suppression. For both functions, robust design of MOSA is necessary. The desired level of the TIV is determined by the system operation voltage while the energy absorption is dependent on the system as well as the circuit breaker parameters [11].

A. MOSA Design for HVdc CB Application

When designing MOSA for HVdc CB application, the desired TIV determines the height of the active part (the number of MO varistors in series) whereas the expected energy in the system determines the total volume of the MOSA. Since a large amount of energy is absorbed during dc fault current interruption, several parallel columns of MOSA are required to cope with the volumetric requirement. However, this requires a column matching procedure; a crucial design step when constructing multi-column MOSA. This is necessary to ensure equal current sharing during energy absorption which otherwise would lead to unequal energy distribution and hence, thermal overloading of one or more columns.

During the column matching procedure, lightning impulses are applied successively to a parallel arrangement of MOSA columns until stable current measurement is obtained. One among these columns is a reference column. Current through each column is measured and compared against the current measurement through the reference column. Columns with current measurements within acceptable margin, for example, $\pm 3\%$ from the reference column current, are accepted as matched.

It is important to note that after manufacturing all MO varistors are screened by applying 8/20 lightning impulses to check the V-I characteristics. Even after this, not all the MO varistors have identical V-I characteristics and hence, the MOSA columns built from the same batch of MO varistors do not necessarily have matching V-I characteristics. This is due to inherent imperfections in the manufacturing process that does not always lead to MO varistors with identical distribution of microscopic ZnO grains. The voltage across an MO varistor is determined by the number of ZnO grain boundaries conducting along the current path. Thus, it is difficult to ensure homogenous distribution of grain boundaries along all current paths even within the same MO varistor let alone in a large number of parallel MO varistors. First, the current flows in the path that results in the fewer number of grain boundaries until it is distributed across the entire cross-section. This is what results in localized current conduction especially at low current densities. When building multi-column MOSA consisting of large number of varistors, the problem of localized current path gets aggravated making some columns conduct more current than the others if necessary caution is not taken.

For the study in this paper, a MOSA module is designed to meet the ratings of the experimental dc CB discussed in Section II-B. The main specifications are as follows:

- Transient Interruption Voltage (TIV) - 40 kV
- Rated interruption current - 16 kA
- Rated energy - 2 MJ

Thus, based on the above specifications, the height and the volume of a MOSA module is determined using electric field, current density and energy per volume relationships [14]. Then, a proper MO varistor is chosen (preferably the largest diameter that can be manufactured in order to reduce the number of columns although it is reported that the optimal size for the highest per volume energy absorption may not be the largest diameter MO varistors [15], [16]). MO varistor with diameter 99 ± 1 mm and height 21.4 ± 0.6 mm having residual voltage of 7.4 kV at 10 kA discharge current is selected. It is reported in the literature that an MO varistor can handle up to $400\ J/cm^3$ [17], [18]. To be on the safe side, a $200\ J/cm^3$ is assumed and based on this, the volume of MOSA required for 2 MJ energy absorption is $10,000\ cm^3$. This results in 60 MO varistors of the selected dimension. To meet the TIV specified above, 6 MO varistors need to be put in series. This results in 10 parallel columns per MOSA module. Additionally, 2 columns are included to reduce the energy per volume to a more safer value ($170\ J/cm^3$) resulting in 12 parallel column per module. Besides, since it was intended for indoor experimentation, MOSA columns with bare varistors are used without any kind of housing as shown in Fig. 10a. Using the above procedure and information, 9 MOSA modules are constructed for investigation in an experimental dc CB.

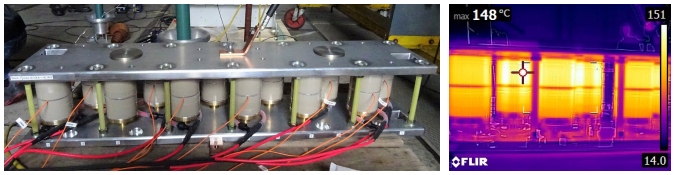
B. Discussion of MOSA Performance

The performance of the MOSA modules is then investigated under realistic test condition where different energy levels are injected during successive current interruptions. During the test campaign, current through 8 columns is measured using Rogowski current probes around each of the 8 columns and the temperature of the corresponding columns is measured using 8 Qualitrol optical temperature sensors with Omniflex-2 signal conditioning system, see Fig. 10a. As can be seen from the figure the fiber optic (FO) temperature sensors are mounted inside an aluminum plates placed at the midpoints of the MOSA columns.

Moreover, the MOSA columns' surface temperature is monitored using infrared camera as shown in Fig. 10b. The MOSA module columns are arranged in such a way that each column can be seen by infrared camera from front/rear side. Also the voltage across the MOSA module is measured using NorthStar VD150 voltage divider as can be seen in the test setup shown in Fig. 2.

Fig. 11 shows the MOSA temperature measurements during 18 consecutive current interruption tests. The same test (approximately equal energy) is repeated until the temperature

[1]Although the effect of arc control (intended for AC arcing) during the very short arc duration with relatively low current as in these dc applications is unknown and needs to be investigated.



(a) (b)

Fig. 10: a) MOSA module with column current and temperature measurement setup b) Thermal image of MOSA after successive energy absorption

of the MOSA reaches about $170°C$. Initially, the MOSA column temperature rise (on average) by about $25.7°C$, see Table III, and the temperature of the columns is more or less equal in the 8 columns showing uniform energy sharing. However, the temperature differences between the columns slightly increase as the MOSA is heated by successive energy absorption, see the zoomed sections in Fig. 11. This is partly related to the differences in cooling of the MOSA columns due to physical arrangement. The columns located in the middle have less convective cooling compared to the columns at the edges. Nevertheless, the increase in the temperature per a given energy injection slightly reduces as the overall MOSA temperature rises. This is shown in Table III where the temperature rise during the second to last test (Test #17) is (on average) about $20.1°C$. This shows more than $5°C$ difference in the temperature rise compared to that of the first test (Test #1) for roughly the same amount of energy injection. The reduction in temperature rise is due to the increase of the heat capacity, 2.85 kJ/$°C \rightarrow$ 3.53 $kJ/°C$ for the same volume of MOSA, with temperature.

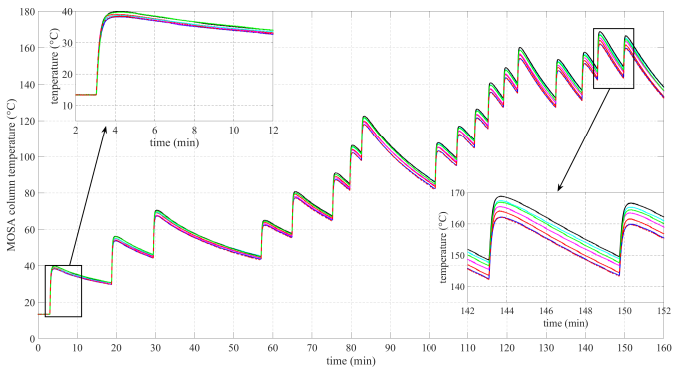


Fig. 11: Temperature measurements of MOSA columns over successive current interruptions

TABLE III: Temperature rise versus energy absorption of MOSA columns at different initial temperature: Test #1 at ambient and Test #17 at 145 $°C$

Column #	Test #1		Test #17	
	Energy (kJ)	Temp. ($°C$)	Energy (kJ)	Temp. ($°C$)
1	71.14	25.7	69.32	20.6
2	68.92	25.0	69.98	19.8
3	70.91	25.2	68.43	20.0
4	75.61	25.5	72.81	19.9
5	76.11	26.6	71.50	20.3
6	75.30	26.4	73.08	20.3
7	73.56	25.2	73.08	20.0
average	**73.07**	**25.66**	**71.17**	**20.13**

In addition to the total current through the MOSA module, the currents through 8 columns of the MOSA are also measured to verify equal current sharing. Typical current measurements through MOSA module columns are shown in Fig. 12. It can be seen that the current through the MOSA columns is not equal. It can be seen that column 2 conducts less than 66% of the current in column 6 and hence absorbs similar proportion of energy.

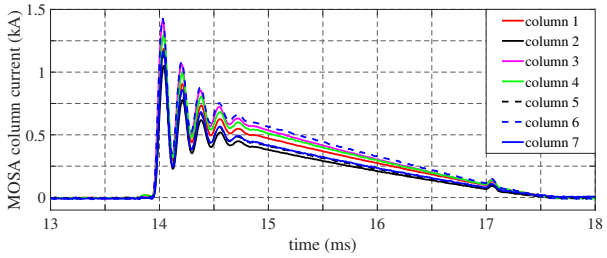


Fig. 12: Current per column of MOSA module during a typical test

It must be noted that during the successive current interruption tests shown in Fig. 11, the maximum energy absorbed by a MOSA module per test is about 1.0 MJ which is less than half the specified rated energy absorption. This is limited intentionally in order not to overheat the MOSA while performing as many tests as possible within a short period of time. Later, a few tests are performed on a double interrupter dc CB while injecting about 2.5 MJ energy per MOSA module. This results in energy per volume of slightly over 200 J/cm^3 which is a margin considered to be safe for MOSA to handle. During this test the MOSA conducts current for about 10 ms; one of such a test is shown Fig. 9. This is extremely long duration compared to the pulse duration in the conventional over-voltage protection application in power systems. The test is repeated 4 times in quick succession to investigate the performance limit of MOSA under rated energy absorption.

The temperature measurements of two columns (one column from each module) is plotted in Fig. 13. The temperature rise and the energy absorbed at each test is shown in the figure. The blue trace shows the temperature of MOSA module 1 while the red trace shows the temperature measurement of MOSA module 2. It can be seen from the figure that during the first test the temperature of the MOSA modules rise by $72°C$ when 5.2 MJ energy is injected into the series connection of the two modules. In the next test temperature rise of $68.6°C$ is observed for nearly the same amount of energy whereas in the third test temperature rise of $66.3°C$ is measured. The reduction in temperature rise per a given energy confirms the increase of the heat capacity of the MO varistors with temperature. By the third test the MOSA temperature exceeds $200°C$.

The fourth test is performed while the MOSA temperature is around $200°C$. Actually, both MOSA modules failed in the fourth test due to failures in the MO varistors which led to flash-over between the module terminals. Moreover, it is interesting to observe that the two MOSA modules did not fail at the same moment and in the same manner. First, MOSA module 2 failed due to extreme thermal stress in one of its columns. The failure of module 2 caused the failure of the module 1. This is because when one MOSA module fails, the remaining MOSA module has to deal with the energy in the circuit. In this case, the MOSA module 1 absorbed

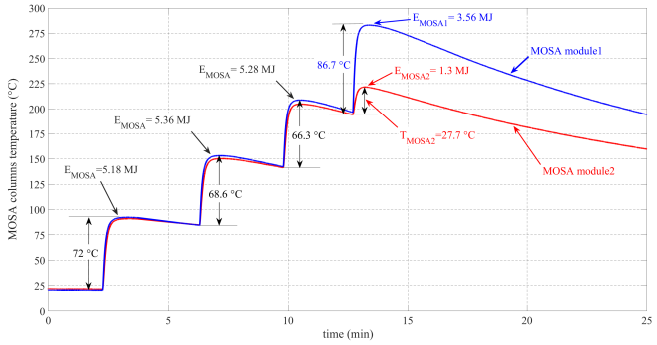


Fig. 13: Temperature measurement during successive high energy tests until destruction

3.56 MJ of energy (40% more than its rated value) before itself failed. During this test, the temperature of MOSA module 1 increased by $86.7°C$, heating up to actual temperature of $285°C$, whereas the temperature of MOSA module 2 increased only by $27.7°C$.

The actual current and voltage measurements during the destructive test is shown in Fig. 14. Measurements of system current, current through the MOSA modules and the TIV are shown. It can be seen that both MOSA modules initially conduct normally for about 2.2 ms until MOSA module 2 fails. The failure of MOSA module 2 led to flash-over between its terminals. This results in the TIV drop by 50 % as can be seen in part b of the figure. Since the resulting TIV is more or less equal to the source voltage during this period, the system current is no longer suppressed. Instead it is limited to more or less a constant value of 10.5 kA for about 5.5 ms after MOSA module 2 fails. The long duration current conduction of MOSA module 1 has led to localized current conduction which ultimately results in localized overheating. The latter resulted in punctures of the MO varistors in MOSA module 1 as can be seen in Fig. 15d.

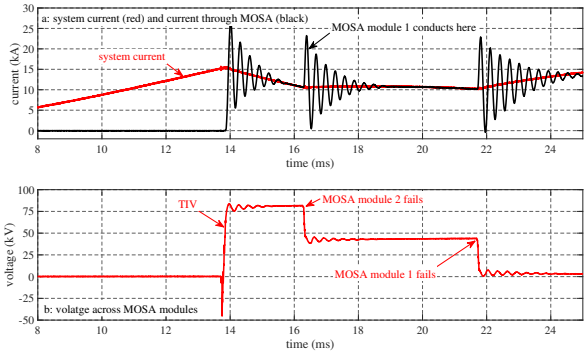
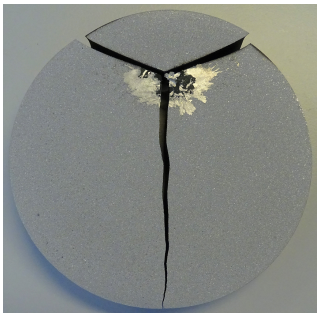


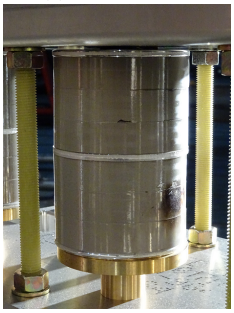
Fig. 14: Current and voltage measurement during MOSA destruction test

Not only the failure instants but also the failure modes of the two MOSA modules are different. Fig. 15a and 15b belong to MOSA module 2 where one of its MO varistors cracked before flash-over occurred between its terminals. Cracking occurs due to thermo-mechanical stress caused by nonuniform heating of MO varistor body over a short duration at high temperature gradient [14], [18]. After the test, all the 72 MO varistors in this module are visually inspected. Only one varistor (shown in 15b) of one column (shown in 15a) cracked while others are visually clean and do not show any trace of damage. This shows a failure of a single MO varistor is sufficient to cause a failure of the entire MOSA module. Fig. 15c and 15d belong to MOSA module 1 where punctures of varying diameters are observed in several varistors of many columns. These punctures also led to flash-over between the terminals of the module. In MOSA module 1 many varistors are punctured and in some cases arc traces are observed on some MO varistor coating, see Fig. 15c and 15d. Punctures occur due to localized heating when MO varistors conduct current for long duration which is the case for MOSA module 1.

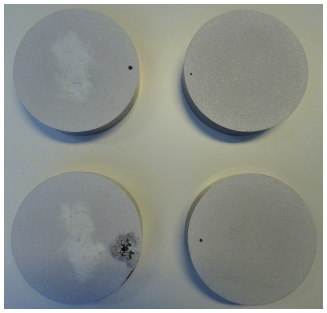
(a) Column burst



(b) Varistor cracked



(c) Surface arc traces



(d) Varistor punctured

Fig. 15: Failure modes of MO varistors after destructive tests

V. Conclusion

The paper presents dc fault current interruption performances of three different types of commercially available VIs. Owing to the differences in the contact system design; shape and size, contact material and composition as well as arc control mechanisms, the performances of the three VIs are completely different. Thus, the VIs can be optimized for dc current interruption. Moreover, re-ignitions and restrikes are very common which entails that the test methods need to take into account adequate voltage stress across the insulation gap (vacuum, SF_6, air) during the entire interruption process. Besides, it is not only the d*i*/d*t* near current zero crossings that determine the interruption performance of a VI but also other parameters such as the arcing duration of the vacuum gap, the magnitude of interruption current, the magnitude, the rate-of-rise and duration of the TIV are crucial.

Investigation of MOSA shows that a properly designed MOSA module performs well when the temperature is below 200 $°C$ and the energy injection per volume is limited to less than 200 J/cm^3. Energy adsorption at temperatures more than 200 $°C$ may result in damage of MO varistor(s), which

leads to overall failure of the HVdc CB. Different failure modes, namely, varistor cracks and punctures are observed when exceeding these limits.

ACKNOWLEDGMENT

The authors would like to thank WP10 members of PROMOTioN project for their useful inputs to the paper. The MOSA modules used in this experimental investigation have been designed at TU Darmstadt, Germany. The authors would like to thank Prof. Volker Hinrichsen and Mr. Peter Hock, both from TU Darmstadt, for their excellent cooperation.

REFERENCES

[1] "Technical requirement and specifications of state-ofthe-art hvdc switching equipment," CIGRE JWG A3/B4.34, Technical Brochure 683, 2017.
[2] S. Tokoyoda, T. Inagaki, H. Sadakuni, T. Minagawa, D. Yoshida, and H. Ito, "Development and testing of EHV mechanical DC circuit breaker," in *2019 5th International Conference on Electric Power Equipment - Switching Technology (ICEPE-ST)*. IEEE, oct 2019.
[3] N. A. Belda, C. A. Plet, and R. P. P. Smeets, "Full-power test of HVDC circuit-breakers with AC short-circuit generators operated at low power frequency," *IEEE Transactions on Power Delivery*, vol. 34, no. 5, pp. 1843–1852, oct 2019.
[4] L. Ängquist, S. Nee, T. Modeer, A. Baudoin, S. Norrga, and N. A. Belda, "Design and test of VSC assisted resonant current (VARC) DC circuit breaker," in *15th IET International Conference on AC and DC Power Transmission (ACDC 2019)*. Institution of Engineering and Technology, 2019.
[5] W. Grieshaber, J.-P. Dupraz, D.-L. Penache, and L. Violleau, "Development and test of a 120 kV direct current circuit breaker," in *CIGRE Session*, ser. 45. CIGRE Paris, 2014.
[6] J. Häfner and B. Jacobson, "Proactive hybrid hvdc breakers - a key innovation for reliable hvdc grids," in *The Electric Power System of the Future: Integrating Supergrids and Microgrids, CIGRE Symposium*. CIGRE, Sep. 2011.
[7] W. Zhou, X. Wei, S. Zhang, G. Tang, Z. He, J. Zheng, Y. Dan, and C. Gao, "Development and test of a 200kV full-bridge based hybrid HVDC breaker," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*. IEEE, sep 2015.
[8] G. Tang, Z. He, H. Pang, X. Huang, and X. ping Zhang, "Basic topology and key devices of the five-terminal DC grid," *CSEE Journal of Power and Energy Systems*, vol. 1, no. 2, pp. 22–35, jun 2015.
[9] Z. Zu, L. Xiaolin, C. Ming, H. Junjia, L. Yan, X. Shukai, Y. Zhao, L. Yanlin, C. Yishun, and Z. Xiaobin, "Research and development of 160kV ultra-fast mechanical hvdc circuit breaker," *POWER SYSTEM TECHNOLOGY*, vol. 42, no. 7, p. 2331, 2018. [Online]. Available: http://www.dwjs.com.cn/EN/abstract/article_27812.shtml
[10] H. Pang and X. Wei, "Research on key technology and equipment for zhangbei 500kV DC grid," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*. IEEE, may 2018.
[11] N. A. Belda, C. A. Plet, and R. P. P. Smeets, "Analysis of faults in multiterminal HVDC grid for definition of test requirements of HVDC circuit breakers," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 403–411, feb 2018.
[12] P. G. Slade, *The Vacuum Interrupter: Theory, Design, and Application*. CRC Press, 2007.
[13] N. A. Belda, R. P. P. Smeets, R. M. Nijman, M. Poikilids, and C. A. Plet, "High-frequency current interruption of vacuum interrupters in an experimental dc circuit breaker," in *5th International Conference on Electric Power Equipment - Switching Technology (ICEPE-ST)*. IEEE, 2019.
[14] V. Hinrichsen, *Metal-Oxide Surge Arresters in High-Voltage Power Systems*, 3rd ed. SIEMENS AG, 2011. [Online]. Available: www.siemens.com/energy/arrester
[15] M. N. Tuczek, M. Broker, V. Hinrichsen, and R. Gohler, "Effects of continuous operating voltage stress and AC energy injection on current sharing among parallel-connected metal–oxide resistor columns in arrester banks," *IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1331–1337, jun 2015.
[16] K. Eda, "Destruction mechanism of ZnO varistors due to high currents," *Journal of Applied Physics*, vol. 56, no. 10, pp. 2948–2955, nov 1984.
[17] K. Ringler, P. Kirkby, C. Erven, M. Lat, and T. Malkiewicz, "The energy absorption capability and time-to-failure of varistors used in station-class metal-oxide surge arresters," *IEEE Transactions on Power Delivery*, vol. 12, no. 1, pp. 203–212, 1997.
[18] M. Bartkowiak;, M. G. Comber, and G. D. Mahan, "Failure modes and energy absorption capability of zno varistors," *IEEE Transactions on Power Delivery*, vol. 14, no. 1, pp. 152–162, Jan. 1999.

Nadew Adisu Belda received the B.Sc. degree in electrical engineering from Bahir Dar University and M.Sc. degree in communication engineering from Addis Ababa University in 2009 and 2011, respectively, in Ethiopia. In 2015 he received joint M.Sc. degree in electrical power engineering from Eindhoven University of Technology (TU/e), the Netherlands (graduated with 'Cum Laude') and Royal Institute of Technology (KTH), Sweden.

Currently, Mr. Belda is innovation engineer at KEMA Laboratories, responsible for the development of test methods and design of test circuits for HVdc switchgear. His research works are part his Ph.D study at Technische Universität Darmstadt (TU Darmstadt), Germany, where he is an external Ph.D candidate. He is a member of IEEE, IEC and CIGRE; and actively participates in related international Working Groups. His research interests are HVdc switchgear with a focus on HVdc circuit breakers and investigation of transients in multi-terminal HVdc system.

Rene Peter Paul Smeets received a Ph.D degree for research work on switchgear in 1987. Until 1995, he was an assistant professor at Eindhoven University. During 1991 he worked with Toshiba Corporation in Japan. In 1995, he joined KEMA, the Netherlands. At present, he is with KEMA Laboratories of DNV GL, as a service area and innovation leader. In 2001 he was appointed part-time professor at Eindhoven University, the Netherlands in the field of high-power switching and testing technology. In 2013 he became adjunct professor at Xian Jiaotong University, China.

Dr. Smeets is convener/member of working groups and study/advisory committees of CIGRE in the field of emerging high-voltage equipment such as high-voltage vacuum -, HVDC switchgear and SF_6 alternatives. He is convener of two maintenance teams in IEC on high-voltage switchgear. Dr. Smeets is a work package leader of the EU project PROMOTioN, committed to demonstrate the full-power testing of various technologies of HVdc circuit breakers. He has published and edited three books and authored over 300 international papers on testing and switching in power systems. In 2008 he was elected Fellow of IEEE and since 2008 he is chairman of the Current Zero Club, a scientific study committee on current interruption. He received seven international awards.

Roy Maarten Nijman received the B.Sc. degree in electrical engineering from HAN technical college, Arnhem, the Netherlands in 2002. He started working for a Dutch electronics manufacturer and continued in the renewable energy sector for Vestas WindSystems A/S until 2008. Then he joined DNV GL KEMA Laboratories in 2008 as a test engineer at the High-Power Laboratory.

Mr. Nijman has gained experience over the past decade in short-circuit testing of High-Voltage Circuit Breakers, Power Transformers/Reactors, Surge Arresters, Disconnectors/Earthing Switches and Gas Insulated Switchgear. He is proficient with direct- and synthetic testing methods, both current- and voltage injection up to UHV level. He mentors new test engineers before they are capable of carrying out high-power tests independently.