Fault Discrimination in HVDC Grids with Reduced Use of HVDC Circuit Breakers

Willem Leterme, Mian Wang and Dirk Van Hertem
KU Leuven/EnergyVille
Kasteelpark Arenberg 10
3000 Leuven
Email: willem.leterme@esat.kuleuven.be

***Abstract*—HVDC grids are currently considered to accommodate the integration of renewable energy sources into the power system. Since HVDC circuit breakers might at present incur a large investment cost, fault clearing strategies with limited use of HVDC circuit breakers have been recently proposed. These strategies, here called partially selective, split the grid into a number of protection zones which encompass sub-grids of multiple converters, transmission lines or a combination of both. Although the application of such strategies within the HVDC grid has been studied recently, discrimination of faults between zones is not yet widely investigated. This paper analyzes the application of a communication-less protection algorithm introduced for fully selective protection in a partially selective protection strategy. A sensitivity analysis using a reduced model shows that the reach of these algorithms is determined by, on the one hand, the length of the cables and complexity of the grid within a protection zone and, on the other hand, the inductance of the series inductor associated with the breaker between the protection zones. A test case implemented in EMT-type software is used to demonstrate the fault clearing sequence in a partially selective strategy.**

***Index Terms*—circuit breakers, HVDC transmission, power system faults, power system protection**

I. Introduction

The increasing share of renewable energy sources such as wind power or photovoltaic sources requires an adaptation of the existing power system. First, power from sources such as offshore wind must be transported on submarine cables over increasing distances as new sites tend to be located farther from shore. Second, the variability of the power output of such sources requires more flexibility in power transmission compared with power generated by fossil-fueled power plants. Voltage source converter (VSC) high-voltage direct current (HVDC) multi-terminal systems or meshed grids can be used to provide both efficient power transfer over large distances and flexibility in power transmission. One of the challenges associated with VSC HVDC systems is protection against dc side faults [1].

Protection of a VSC HVDC grid using HVDC circuit breakers is challenging due to the nature of the fault currents to be interrupted [2]. Fault currents in HVDC systems do not exhibit natural zero crossings and exhibit, in the worst case, a high rate-of-rise. Therefore, HVDC circuit breakers must force the current to zero and absorb the energy stored in the system's inductance on a millisecond time range [3]. Several prototypes have been reported in the recent literature, e.g., in [4], [5], [6], [7]. All presently proposed HVDC circuit breakers require the presence of one or more series inductors to limit the rate-of-rise of the dc fault current.

Several strategies for clearing dc faults using HVDC circuit breakers have been presented in the literature [8]. These strategies make use of HVDC circuit breakers at every line end, here called a fully selective strategy, between protection zones encompassing multiple lines, in a partially selective strategy, or placed in series with the converters. These strategies aim at finding a trade-off between investment cost due to HVDC circuit breakers and limiting the impact of a fault on the dc system and interconnected ac systems. Protection algorithms for fully selective protection have received a lot of attention in the recent literature, as shown in [9]. By contrast, protection algorithms for a partially selective strategy with limited use of HVDC circuit breakers are not yet widely studied.

This paper proposes a communication-less protection algorithm for fault discrimination for use in partially selective fault clearing strategies with a limited number of HVDC circuit breakers. As such, it contributes to the step to be taken between protecting a HVDC grid without any HVDC circuit breaker and with HVDC circuit breakers at each line end. The algorithm is based on the principles introduced for selective fault clearing strategies in [10], [11]. The selectivity and sensitivity of the algorithm is investigated for a wide range of parameters using a reduced model. Thereafter, these results are validated using a case study implemented in PSCAD.

II. Proposed Protection Algorithm

In a VSC HVDC grid which is protected with a limited number of HVDC circuit breakers, also called a grid-splitting or partially selective protection strategy, protection algorithms are needed to operate the breakers at the end of each zone. In Fig. 1, an example HVDC grid is shown with three zones, L, M and N, which are separated using HVDC circuit breakers. To interrupt a fault current for a fault in Zone M, the HVDC circuit breakers Br_1 and Br_2, and the ac circuit breakers Br_3 and Br_4 are tripped. Thereafter, the faulted component is isolated using the switches placed at each line end and at each converter dc terminal. These switches do not have fault current interruption capability.

The work of W. Leterme, M. Wang, and D. Van Hertem is funded by the Horizon 2020 PROMOTioN project under grant agreement No 691714.

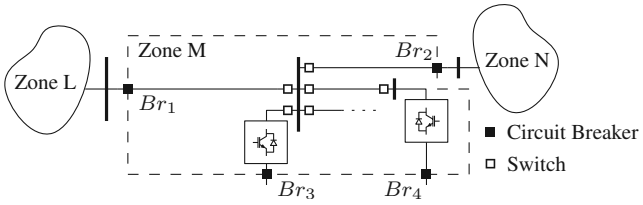

Fig. 1. Protection zones

The functional requirements for the (combination of) protection algorithms associated with the HVDC circuit breakers in such a strategy can be stated as follows: (i) they must detect all internal faults (i.e., they must be dependable), (ii) they must not operate for external faults (i.e., they must be secure) and (iii) they must quickly act to avoid voltage collapse in neighbouring zones [12]. Due to the counteracting requirements of speed on the one hand and reliability, i.e., dependability and security, on the other hand, these functional requirements might not be achieved using a single principle.

To achieve the required speed of operation, the protection algorithm under study in this paper is a communication-less principle which uses the inductive terminations of each zone to discriminate faults between zones. The inductive terminations of the protection zones bounded by the breakers are due to the series inductors required for all presently proposed HVDC circuit breaker prototypes. The inductors form a low-pass filter for the wavefronts of faults external to the protected zone. This can be used to discriminate external faults from internal faults, for which the traveling waves exhibit steep wavefronts. This principle was outlined in [10] and [11] for fully selective protection of VSC HVDC grids, i.e., employing circuit breakers at all cable ends. In [10], the possibility to use this principle in VSC HVDC grids with a limited number of HVDC circuit breakers was briefly mentioned.

The detection function used in this paper is based on the one introduced in [13]:

$$S_1 = u'(t) - R_\mathrm{c} i'(t), \tag{1}$$

where $u'(t)$ and $i'(t)$ are the superimposed components of the waveforms measured during a fault and R_c is an impedance to match the characteristic impedance of the cable at which the measurements are done. $i'(t)$ takes positive values for currents flowing in the direction of the protected zone. The advantage of using this detection function is that, due to the almost ideal termination impedance, the network topology behind the relay does not need to be studied.

The possibility of using the detection function in a communication-less algorithm is investigated. To this end, the superimposed components $u'(t)$ and $i'(t)$ are obtained by taking the first derivative of the measured quantities and the resulting detection function is compared against a threshold:

$$S_1 > S_1^{\mathrm{thr}}. \tag{2}$$

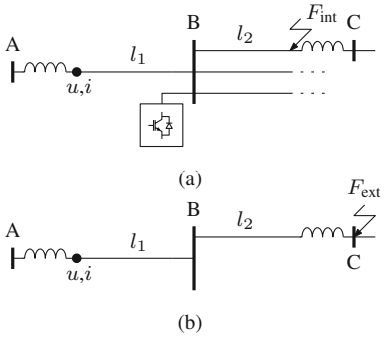

Fig. 2. Analysis of worst case for internal fault (a) and worst case for external fault (b)

III. Protection Algorithm Sensitivity Analysis

A. Test case

The test system used to analyze the sensitivity of the traveling-wave based algorithms is based on the one shown in Fig. 1. Two of the transmission lines, i.e., those connected to zones L and N, are terminated by a breaker and associated series inductor. In the test system, the parameters for the transmission lines (submarine cables) and converters (Modular Multilevel Converters (MMCs)) are taken from [14] and recapitulated in Table I and III.

The analysis considers only the superimposed fault circuit by applying a step input in the voltage at the fault location (see also [15]). The Numerical Inverse Laplace Transform (NILT) described in [16] is used to obtain the waveforms of the superimposed components. To avoid non-linear effects, the converters are modeled according to the model given in [17].

In the sensitivity analysis, the performance of the algorithm associated with the breaker located at Bus A is considered for internal faults (Fig. 2a) and external faults (Fig. 2b). To analyze the performance, minimum and maximum values of the detection functions for internal and external faults were determined.

The minimum value of the detection function for internal faults was determined using the topology of Fig. 2a, since it results in the lowest transmission of waves originating from F_{int} to bus A. The transmission lines departing from bus B were assumed to be reflectionless. A voltage correction factor of 0.95 was applied to account for voltage variations during normal operation.

The maximum value of the detection function for external faults was obtained with the test system shown in Fig. 2b, since it results in maximum transmission of waves originating from bus C towards bus A. To incorporate worst case fault conditions taking into account voltage variations, a voltage correction factor of 1.05 was applied.

The sensitivity analysis was performed by adapting the line inductor value L_{br} and line length l_2, whereas l_1 was kept constant at 350 km. The line length l_2 was varied from 25 to 350 km with increments of 25 km, whereas the inductor value L_{br} was set to 10, 50 or 100 mH. The NILT was performed using 1000 samples in a time window of 10 ms.

The voltage and current signals were processed with a finite impulse response (FIR) filter of ten samples with coefficients $b_0..b_4 = 1$ and $b_5..b_9 = -1$.

B. Results

For internal faults, the maximum value of the S_1 decreases with increasing cable length l_2 and number of cables attached to bus B n (Fig. 3). Increasing l_2 results in a higher attenuation and distortion of the wave, whereas increasing n results in a lower transmission of the wave towards the cable at which the relay is located.

Discrimination between remote internal faults and external faults requires either a low complexity of the grid topology in the protected zone, short transmission lines or high inductance of the series inductors between the protection zones. For instance, if $n = 1$, discrimination with $L_{\text{br}} = 10$ mH can only be achieved if the cable length is lower than 50 km. In all other cases involving $L_{\text{br}} = 10$ mH, the minimum value of the detection function for internal faults lies below the maximum one for external faults (Fig. 3). For $L_{\text{br}} = 50$ mH and $n = 2$, discrimination can in theory be achieved for l_2 within 200 to 225 km. For $L_{\text{br}} = 100$ mH, regardless of n, discrimination can in theory be achieved for all l_2 up to or even exceeding 350 km.

The reach of the proposed algorithm with respect to the (topology-wise) worst and best case for internal faults shows a large variation. For instance, if a threshold of 50 is chosen for S_1, the difference in reach is 200 km (Fig. 3, where the line S_1=50 intersects with the values associated with $F_{\text{int}}, n = 0$ and $F_{\text{int}}, n = 2$ at l_1=300 and l_1=100, respectively).

The transmission line attached to bus B which yields the maximum value for F_{ext} as function of l_2 and L_{br} determines the reach l_2^* of the algorithm on all lines attached to bus B. To ensure proper discrimination between internal and external faults, the threshold must be set above this maximum value. This value is determined by l_2 and L_{br} as shown in Fig. 3. The reach on the other lines is then, in the worst case, also limited to l_2^*, with * indicating the line length of the critical transmission line.

If a reach higher than l_2^* is required, the algorithm must be complemented by alternative algorithms or communication to avoid non-selective tripping of the breaker at bus A. These are in this paper not considered.

IV. Case Study

The test system for the case study considers a HVDC grid with six converters, split into three protection zones (indicated by red, orange and blue dashed lines in Fig. 4). The protection zones are chosen such that, in case of a fault in one of the zones, the other zones can continue operation as a point-to-point link. Protection zone configurations were chosen to demonstrate the possibilities and limitations of the proposed algorithm. For practical application, optimization of protection zones should be done on a project-base bound to specific project requirements.

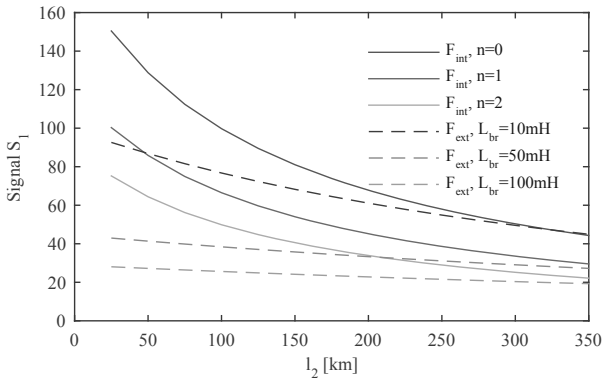

Fig. 3. Minimum and maximum detection functions for internal fault and maximum detection function for external fault as function of l_2, n and L_{br} ($l_1 = 350$ km).

TABLE I
Converter and Grid Parameters

Parameters	Value	Unit
Rated apparent/active power	1265/1200	[MVA/MW]
Rated dc voltage	$\pm$ 320	[kV]
Rated transformer voltages	400/333	[kV]
Transformer leakage impedance	0.18	pu
Arm capacitance C^{arm}	22	[μF]
Arm inductance L^{arm}	42	[mH]
Arm resistance R^{arm}	0.6244	[Ω]
Converter dc smoothing reactor	10	[mH]

To divide the protection zones at the DC side, HVDC circuit breakers are placed in lines L_{12}, L_{14}, L_{25} and L_{45} at the buses connected to converters 1 and 5, respectively. The inductance of the series inductors associated with the breakers is 100 mH. At the ac side, every protection zone is bounded by ac circuit breakers.

The converter parameters and line lengths are given in Tables I and II, respectively. The converters are modeled with the continuous model described in [18] and protected according to the overcurrent criterion described in [19]. The converter ac breakers are opened within 60 ms after detecting an arm overcurrent. The HVDC circuit breakers are modeled as hybrid breakers with an opening time of 2 ms. The simulation time step is 5 μs.

In the case study, the protection associated with the breaker at line L_{12} is investigated. First, suitable thresholds were determined based on Fig. 3. Second, these thresholds were compared with the results obtained in PSCAD. Third, the algorithm and fault clearing sequence was assessed for a solid fault located 25 km from converter 2.

A. Threshold Determination

The algorithm associated with the breaker located at L_{12}, Br_{12} must not trip for a solid fault at bus 5. The maximum value for S_1 is obtained for the case in which only L_{12} and L_{25} are in the path between this fault and the measurements at Br_{12}. From Fig. 3, this value is 19.3. The test system

TABLE II
TRANSMISSION LINE LENGTHS IN KM

L_{12}	L_{13}	L_{14}	L_{24}	L_{25}	L_{45}	L_{56}
350	150	300	100	350	400	200

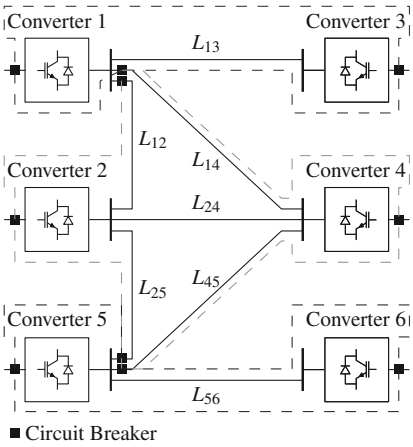

Fig. 4. Test system topology and protection zones (dashed colored lines).

implemented in PSCAD provides a result of 19.78. The threshold S_1^{thr} should thus be at least 19.3. Taking a margin into account, the threshold is in this paper set to 25.

B. Reach

The reach for the algorithm associated with Br_{12} is expected to be the lowest for faults on L_{45}. The reach of the algorithm associated with Br_{12} for faults on line L_{25} and L_{45} is limited due to attenuation and distortion of waves due to cable propagation and reflections at the buses connected to converters 2 and 4. For faults on L_{45}, the distance between the fault and the measurements at L_{12} can take the highest value, i.e., maximum 850 km for faults occurring at the converter 5 end of L_{45}. Furthermore, traveling waves created by faults on L_{45} are reflected at the buses at converter 4 and 2, respectively, before reaching the measurements at L_{12}. As a consequence, for faults on L_{45}, the detection function constructed using the measurements at L_{12} takes the lowest value.

By communicating trip signals between the algorithms for Br_{12} and Br_{14}, the reach of the communication-less algorithm on L_{25} and L_{45} can be improved compared with separate algorithms for both breakers. With local communication between breakers at a bus, faults on L_{45} no longer determine the worst case for the algorithm associated with the measurements at L_{12}, since faults on this line can be dealt with by the algorithm associated with Br_{14}. The worst case for the algorithm associated with Br_{12} is a fault at the line end of L_{25} closest to converter 5. The detection function value predicted in the sensitivity analysis is 29.5, whereas the one in PSCAD is 29.08.

TABLE III
CABLE PARAMETERS

	Outer radius [mm]	ρ [Ω m]	ϵ_{rel} [-]	μ_{rel} [-]
Core	25.13	1.72e-8	-	1
Insulation	48.38	-	2.3	1
Sheath	50.13	21.4e-8	-	1
Insulation	54.13	-	2.3	1
Armour	59.73	1.38e-7	1	10
Insulation	64.73	-	2.3	1

TABLE IV
THRESHOLDS FOR THE REDUCED MODEL AND PSCAD MODEL

Fault Location	U_{dc} [pu]	n	Converter 2	Reduced	PSCAD
L_{25} (at Br_{25})	0.95	1	in service	29.53	29.08
$Bus5$	1.05	0	out of service	19.30	19.78

C. Fault Clearing Sequence

The fault clearing sequence is illustrated using a solid fault on L_{25} located at 25 km from converter 2.

The fast action by the protection algorithms and HVDC circuit breakers avoids voltage collapse and excessive fault currents in the healthy part of the system. During fault detection and opening of the breakers associated with the faulted protection zone, the voltage in the healthy part of the grid decreases quickly whereas currents increase fast (Fig. 5, time interval [2-4.2] ms). After opening of the HVDC circuit breakers in lines L_{12} and L_{14}, the voltage in the healthy part of the grid exhibits a transient overvoltage due to insertion of the breaker surge arrester prior to reaching a stable value (Fig. 5a), whereas the current reduces to zero (Fig. 5b).

Due to the fast action by the protection, power flow in the healthy part of the system can continue whereas the power flow in the faulted part is reduced to zero (Fig. 6). After opening the breakers, Converters 1 and 3 and Converters 5 and 6 continue power exchange in a point-to-point connection. In this paper, the oscillations in the active power seen in Fig. 6 have not been subject to in-depth analysis and converter controls were not optimized to dampen these.

Restoration of the faulted part using switches without fault current interruption capability might only be possible after several hundreds of milliseconds. In the faulted part of the system, the fault current shows a slow decrease after opening the HVDC circuit breakers and converter ac breakers (Fig. 7). The slow decrease in the current is due to the release of stored energy in the arm inductors. If switches without current breaking capability are used to isolate the faulted line, opening must be delayed until the current has decayed to zero, which in this case is at $t = 0.64$ s ($i < 0.1$ kA).

V. CONCLUSION

Fast fault discrimination in HVDC grids with reduced use of HVDC circuit breakers is challenging due to the potential large distances within, and the complexity of, the intermediate grid between the fault and the measurement location. This paper

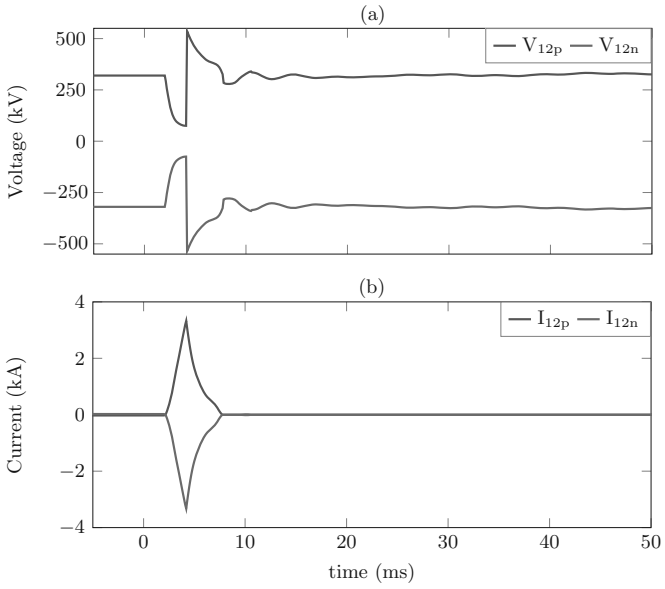

Fig. 5. (a) Dc voltages and (b) dc currents measured at the relay position.

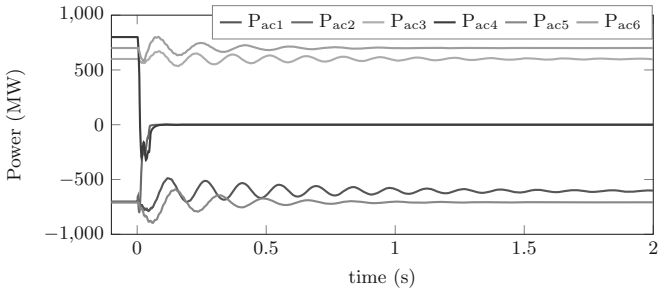

Fig. 6. Active power measured at the transformer secondary side.

investigated a communication-less principle based on traveling waves to quickly discriminate faults within the protection zone from external ones. Although the algorithm is able to detect faults in remote parts of the grid, the reach of the proposed protection algorithm is limited since traveling waves are attenuated, distorted and only partly transmitted before reaching the measurement location.

A sensitivity analysis using a reduced model showed that the reach of the proposed algorithm increases with increasing inductance of the breaker inductor between the protection zones, decreasing length of transmission lines and decreasing complexity of the grid topology within the protected zone. The results obtained in the sensitivity analysis were confirmed by a comparison against a detailed test system implemented in PSCAD. Finally, successful fault clearing in the faulted zone and continuous operation of the healthy zones within this test system was demonstrated.

REFERENCES

[1] W. Leterme and D. Van Hertem, "Dc fault phenomena and dc grid protection," in *HVDC Grids: for offshore and supergrid of the future*, D. Van Hertem, O. Gomis-Bellmunt, and J. Liang, Eds. Hoboken, NJ: J. Wiley & Sons, 2016, ch. 17.

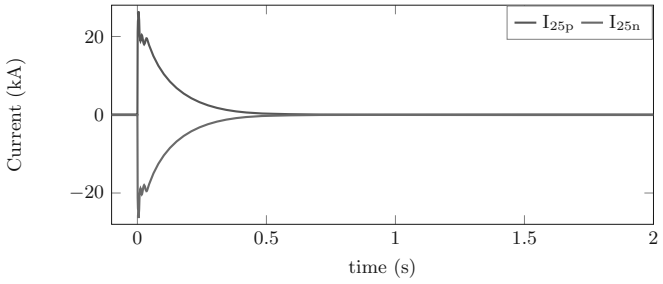

Fig. 7. Fault currents in cable L_{25}.

[2] M. K. Bucher, M. M. Walter, M. Pfeiffer, and C. Franck, "Options for ground fault clearance in HVDC offshore networks," in *Proc. IEEE ECCE*, Raleigh, NC, USA, 15-20 Sep. 2012, pp. 2880–2887.
[3] C. Franck, "HVDC circuit breakers: A review identifying future research needs," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 998–1007, Jan. 2011.
[4] J. Häfner and B. Jacobson, "Proactive Hybrid HVDC Breakers: A key innovation for reliable HVDC grids," in *Proc. CIGRÉ Bologna Symp.*, Bologna, Italy, 13-15 Sep. 2011, 8 pages.
[5] C. Davidson, R. Whitehouse, C. Barker, J. Dupraz, and W. Grieshaber, "A new ultra-fast HVDC circuit breaker for meshed dc networks," in *Proc. IET ACDC*, Birmingham, UK, 10-12 Feb. 2015, 7 pages.
[6] K. Tahata, S. Ka, S. Tokoyoda, K. Kamei, K. Kikuchi, D. Yoshida, Y. Kono, R. Yamamoto, and H. Ito, "HVDC circuit breakers for HVDC grid applications," in *Proc. AORC-CIGRE 2014*, Tokyo, Japan, 27-29 May. 2014, 9 pages.
[7] L. Ängquist, S. Norrga, and T. Modéer, "A new dc breaker with reduced need for semiconductors," in *Proc. EPE'16 ECCE Europe*, Karlsruhe, Germany, 5-9 Sep. 2016, 9 pages.
[8] W. Leterme and D. Van Hertem, "Classification of fault clearing strategies for HVDC grids," in *Proc. CIGRÉ Lund*, Lund, Sweden, 27-28 May 2015, 10 pages.
[9] I. Jahn, N. Johannesson, and S. Norrga, "Survey of methods for selective DC fault detection in MTDC grids," in *Proc. IET ACDC 2017*, Manchester, UK, Feb. 14-16 Feb. 2017, 7 pages.
[10] J. Sneath and A. D. Rajapakse, "Fault detection and interruption in an earthed HVDC grid using ROCOV and hybrid dc breakers," *IEEE Trans. Power Del.*, vol. 31, no. 3, pp. 973–981, Jun. 2016.
[11] W. Leterme, J. Beerten, and D. Van Hertem, "Nonunit protection of hvdc grids with inductive dc cable termination," *IEEE Transactions on Power Delivery*, vol. 31, no. 2, pp. 820–828, April 2016.
[12] F. Dijkhuizen and B. Berggren, "Zoning in high voltage dc (HVDC) grids using hybrid dc breaker," in *EPRI HVDC and FACTS Conference*, Palo Alto, CA, 28 Aug. 2013, 10 pages.
[13] A. Johns, "New ultra-high-speed directional comparison technique for the protection of e.h.v. transmission lines," *IEEE Proc. Gen., Transm. and Distr.*, vol. 127, no. 4, pp. 228–239, Jul. 1980.
[14] Promotion, "Deliverable 2.1: Grid topology and model specification," 2016.
[15] M. Vitins, "A fundamental concept for high speed relaying," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-100, no. 1, pp. 163–173, Jan 1981.
[16] D. J. Wilcox, "Numerical laplace transformation and inversion," *International Journal of Electrical Engineering Education*, vol. 15, no. 3, pp. 247–265, 1978.
[17] W. Leterme and D. Van Hertem, "Reduced modular multilevel converter model to evaluate fault transients in dc grids," in *Proc. IET DPSP 2014*, Copenhagen, Denmark, 31 Mar.-3 Apr. 2014, 6 pages.
[18] N. Ahmed, L. Ängquist, S. Norrga, and H.-P. Nee, "Validation of the continuous model of the modular multilevel converter with blocking/deblocking capability," in *Proc. IET ACDC 2012*, Birmingham, UK, 4-6 Dec. 2012, 6 pages.
[19] W. Leterme, N. Ahmed, L. Ängquist, J. Beerten, D. Van Hertem, and S. Norrga, "A new HVDC grid test system for HVDC grid dynamics and protection studies in EMTP," in *Proc. IET ACDC*, Birmingham, UK, 10-12 Feb. 2015, 7 pages. [Online]. Available: https://www.esat.kuleuven.be/electa/hvdcresearch/hvdc-test-grid