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Development of a protection strategy for future DC networks based on low-speed DC circuit breakers

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SUMMARY

Multi-terminal high voltage direct current (MTDC) grids are considered to be an interesting solution to integrate bulk renewable energies located far away the consumption areas. One of the most challenging issues for the development of such MTDC grids remains the protection against DC faults. Although several types of HVDC breaker technologies have already been proposed and demonstrators tested by manufacturers, the coordination of such devices to ensure a proper protection system has not yet been proved. Difficulties encountered during the development of such DC grid protection system address, among others, the reliability of the protection scheme and its ability to ensure the AC and DC systems stabilities during and after the fault clearance. Therefore not only a reliable primary protection scheme, but also a robust backup scheme, have to be developed.

This paper presents a novel protection scheme based on converter breaker; its key element, namely a low-speed mechanical DC breaker, is located at each DC converter output. This strategy belongs to the non-selective fault clearing philosophy whose protection priority is given to the fault current clearance by opening the converter circuit breakers without any discrimination. The selectivity of the protection is thereafter ensured by the opening of mechanical DC breakers located at each end of faulty line.

To validate the protection strategy, primary protection scheme as well as back-up solutions in case of main component failures have been considered. Protection schemes are validated through detailed EMT simulations for a 3-terminals DC grid in bipolar configuration and with cable links. Technical requirements of the main components such as DC circuit breakers are highlighted in the paper. Moreover, an optimized pre-insertion resistor for a fast grid voltage restoring after faulty line isolation is also described.

To demonstrate the adequacy of the proposed protection strategy a particular emphasis is given to the impact of a DC fault on the AC transient stability. Benchmark cases of a future MTDC grid with high renewable energy source penetration will be presented to identify advantages and limits of such protection scheme.

KEYWORDS

HVDC Grid - Protection - DC Circuit-Breaker (DCCB) – AC/DC Stability

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1. INTRODUCTION

A main challenge related to the development of future MTDC grids concerns their protection against DC short circuit fault. A DC fault is characterized by its rapid propagation along the grid, no natural current zero crossing and currents that can reach tens of kA in some cases. DC grid protection is requested to perform fast faulty line identification and fast fault clearing while ensuring minimum disturbance to the interconnected AC transmission system. New HVDC breaker technologies have demonstrated possibilities to clear a current up to 15-20 kA using either ultra-fast hybrid DC breakers or mechanical DC breakers with breaking times of respectively 2-3ms [1], [2] and 5-10ms [3], [4]. During the last few years, together with the DC breaker technical breakthrough, several protection philosophies have been suggested in the literature. The following classification of the existing fault clearing strategies has been proposed in [5] and [6] :

- Fully selective fault clearing strategy;
- Partially selective fault clearing strategy;
- Non-selective fault clearing strategy.

In a fully selective fault clearing strategy each line is considered a single protection zone and the faulty line is preliminary identified before the selective tripping of the DC breakers. This strategy minimizes the impact of a fault on the DC grid but requires a large number of DC breakers, current limiting devices and robust non-unit fault identification algorithms.
In a partially selective fault clearing strategy, the DC grid is dived in few zones, each zone including several lines, busbar and converters. In case of fault, the healthy zones are disconnected from the faulty one in such a way that a large part of the grid can continue its power flow with minimum of disturbance.
In a non-selective fault clearing strategy, the whole DC grid is considered as one protection zone. Therefore, once a DC fault is detected, the entire grid is de-energized. The faulty line is thereafter discriminated and isolated. Finally, power flows are restored on the healthy part of the MTDC grid.
This paper describes the development of a novel non-selective fault clearing strategy called converter breaker strategy as presented in [7]. Section 2 explains the protection system layout and components, and the detailed primary and backup protection sequences. In section 3 some relevant results coming from Electro Magnetic Transient (EMT) simulations on a MTDC test benchmark are presented. Section 4 defines the technical requirements for the protective component and Section 5 discusses the impact of a DC fault on the stability of the interconnected AC grid.

2. FAULT CLEARING STRATEGY DESCRIPTION

2.1. Layout and component description

The location of the protection equipment required for a bipolar HVDC grid system employing the converter breaker strategy is illustrated on Figure 1. This fault clearing strategy can be employed together with AC/DC converters without fault current blocking capability, such as the half-bridge MMC converters. The protection equipment includes:

- Converter breaking module (C_{BM}) associated to each MMC converter and located at their DC side;
- Line breaking module (L_{BM}) associated to each transmission line and located at both line ends;
- Pre-insertion resistor (C_{PIR}) in series with the converter breaking module.

Each breaking module performs the functions of fault current breaking, isolation, measurement and tripping control system. They are composed of a DC circuit breaker (DCCB), a high speed switch (HSS) with very low DC breaking capability for isolation function, voltage and current sensors and a protective relay to ensure the control function.

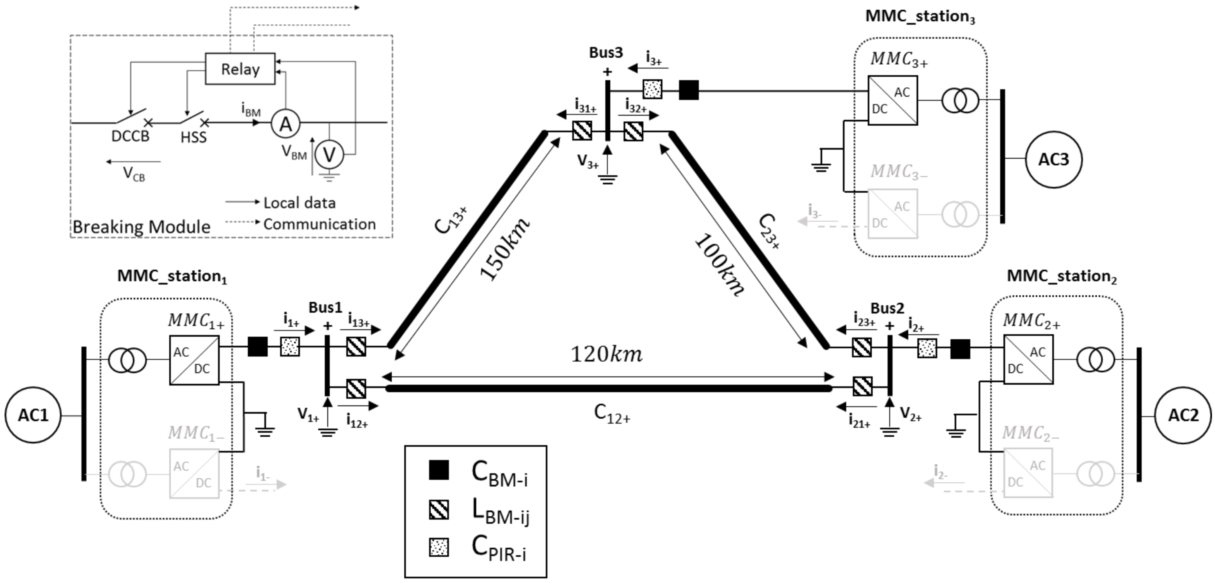

Figure 1 : Illustration of protection system architecture (one pole)

2.2. Primary sequence

This section presents the primary protection sequence that will be operated when a short-circuit fault occurs on a DC transmission line of the MTDC grid. Four main steps can be identified in a non-selective fault clearing strategy: the suppression of AC grid fault current contribution, the faulty line isolation, the grid voltage restoration and the power flow restoration. The generic flowchart is depicted in Figure 2.

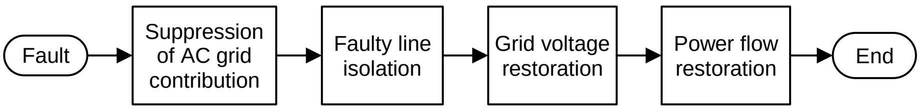

Figure 2 : Generic flowchart for the non-selective fault clearing strategy

In the proposed converter breaker strategy, the first step is accomplished by DC converter breakers which are tripped right after the fault detection in order to suppress the AC fault current contribution. Because of the fast propagation speed of the fault, all converter breakers are tripped almost in the same time, with a maximum difference of few ms, depending on the fault distance. It should be noted that after fault arrival and before DCCB breaker opening, MMC converters are rapidly blocked and the AC contribution to the fault passes through the freewheeling diodes. During this period, a fault identification algorithm can be operated to discriminate the faulty line. After converter breaker opening, the MMC can be deblocked and converters can be used as STATCOM to sustain the AC voltage by injecting reactive power into the grid.

The second step, faulty line isolation, starts after the operation of the fault identification algorithm and it is performed by the line breakers. The reason to use line breakers instead of more simple high speed switches as proposed in [12] relies on their breaking capability, required in order to accelerate the protection sequence in case of a converter breaker failure, as it will be discussed in subsection 2.3.

After the faulty line is isolated, the converter breakers reclose and the grid voltage restoration begins. The reclosing order is sent independently to each converter breaker after a fixed delay, called “reclosing time”, has been elapsed. The reclosing time, here set to 50ms, needs to be long enough to ensure that the faulty line isolation has been performed, even in case of a breaker failure backup sequence. The breaker reclosing is implemented through an optimized PIR which avoids inrush currents that could damage the converter power electronics and which allows a fast grid voltage restoration. After voltage restoration, the power flow can be re-established by MMC controllers. A more detailed flowchart of the primary protection sequence is shown in Figure 3.

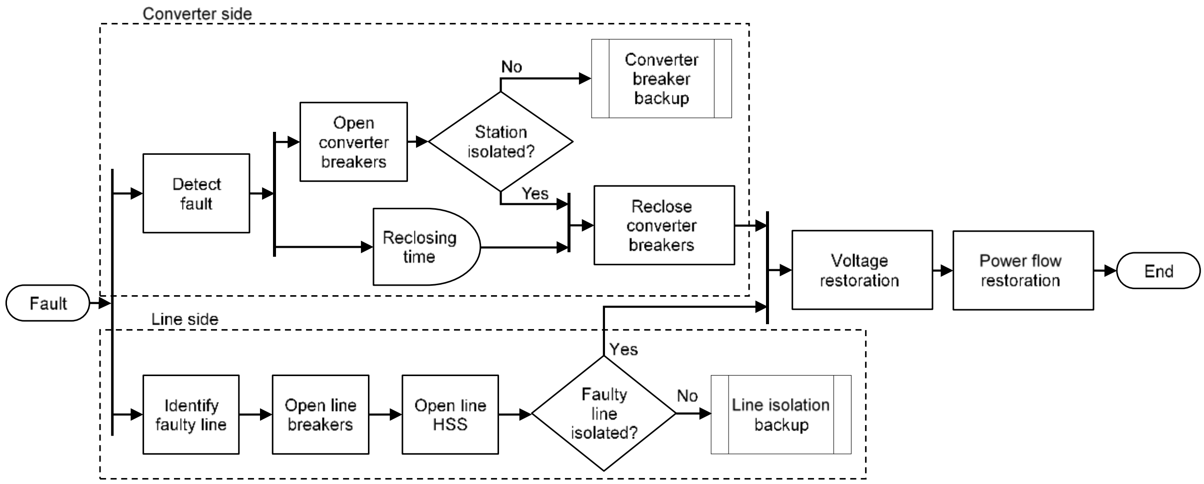

Figure 3 : Primary sequence

2.3. Converter Breaker failure backup sequence

In case one converter breaker fails to open, its associated MMC converter remains blocked and maintains the contribution to the fault current. However, because of the disconnection of N-1 converters stations (where N is the number of stations on the DC grid) the fault current does not reach the line breaker current capability and the breaker opening of faulty line can still be performed. Once the fault current is close to zero, the HSS in series with the failed converter breaker is able to open and isolate the converter from the grid. The healthy part of the grid is thereafter ready to restart the power flow. Figure 4 shows the converter breaker failure backup sequence; it can be seen that the AC breaker opening can be considered as ultimate backup.

2.4. Line Breaker failure backup sequence

In case of line breaker opening failure the sequence is the same as for the primary sequence. Indeed, even if a line breaker fails to open, the fault current is still cleared by the converter breaker. The HSS associated to the failed line breaker will open when the HSS opening conditions are ensured and it will isolate the faulty line. As already mentioned, the reclosing time of the converter breaker delay needs to be long enough to ensure the operation of the line HSS in case of a line breaker failure. Figure 5 shows the line breaker failure backup sequence. The opening of the adjacent line breakers is considered as ultimate backup in case both converter breaker and line breaker would fail.

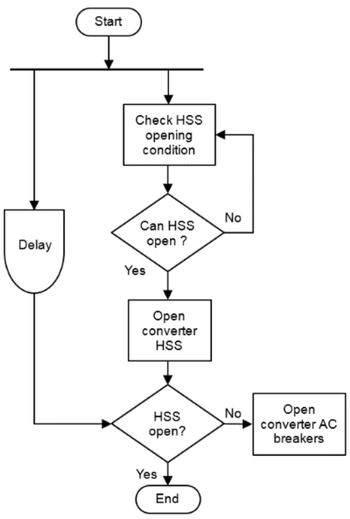

Figure 4 : Converter breaker failure backup sequence

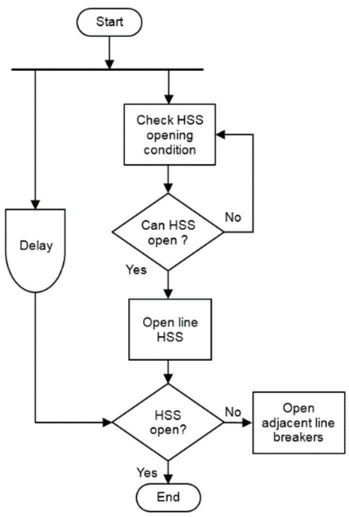

Figure 5 : Line breaker failure backup sequence

3. Test benchmark

3.1. System modelling

The fault clearing strategy for a DC line fault has been validated through off-line simulations performed on a MTDC test benchmark. The test grid is a three-terminal meshed grid in bipolar configuration as shown in Figure 1. The MTDC grid connects three AC grids through three AC/DC converter stations. Half-Bridge MMCs are considered and transmission lines are composed of underground XLPE cables. For sake of simplicity, it is supposed that all converter stations are solidly grounded. Simulations are performed on EMTP-RV© software. Relevant system parameters are shown on Table 1.

Table 1 : MTDC test grid parameters

	Symbol	Description	Value	
AC Side	V_{AC}	Rated voltage	400	kV
	f	Frequency	50	Hz
	X/R	AC grid ratio	10	
	S_{SC}	Short-circuit power	30	GVA
		Model	Ideal voltage source	
MMC converters	S_{AC}	Transformer rated power	500	MVA
	x_T	Transformer reactance	0.18	pu
	V_{DC}	Rated voltage	±320	kV
	I_{DC}	Rated current	1500	A
	S_{MMC}	Rated power (per pole)	500	MVA
	L_{ARM}	Arm inductance	16	mH
		Model	Arm switching function	
		Number of sub-modules/arm	400	

Cables are modeled using a frequency dependent (wideband) model and their lengths are shown in Figure 1. The fault is located on cable C_{13}, close to station 1, and it is modeled by an instantaneous short-circuit among core, screen and ground.
DC circuit breakers are modeled using an ideal switch in parallel with a capacitor (20µF) and a surge arrester with limiting voltage rated at 1.5pu. The breaker operation time is set to 12ms.
The MMC converters are regulated using an energy based control system employing the virtual capacitor control for outer loop [9] and a discrete-time controller for inner loops on currents [10] which allow high dynamic responses to power changes. The chosen control strategy for the MTDC grid is the master/slave scheme; power and voltage references during the entire process are shown in Table 2.

Table 2 : MTDC control strategy, power and voltage references

MMC Station	**Before fault**	**During fault clearing (after deblocking)**	**During voltage restoration (after DCCB reclosing)**	**During power restoration**
MMC1	V_{dc} control (320 kV, -250 MVAR)	P,Q control (0 MW, 250 MVAR)	V_{dc} control (320 kV, -250 MVAR)	V_{dc} control (320 kV, -250 MVAR)
MMC2	P,Q control (250 MW, 200 MVAR)	P,Q control (0 MW, 200 MVAR)	P,Q control (0 MW, 200 MVAR)	P,Q control (250 MW, 200 MVAR)
MMC3	P,Q control (100 MW,-100 MVAR)	P,Q control (0 MW, -100 MVAR)	P,Q control (0 MW, -100 MVAR)	P,Q control (100 MW, -100 MVAR)

Before fault event, MMC1 controls the DC voltage (V_{dc}) and the reactive power (Q) while MMC2 and MMC3 control the active (P) and reactive powers.
During fault clearing, once the converter breakers are in open position and converters deblocked, all converters are set in P,Q control mode with zero active power reference. During this time, the converters act as STATCOM.
At the beginning of the voltage restoration, immediately after the reclosing of converter DCCB, the control mode of MMC1 switches to V_{dc},P reference with zero active power and 1pu reference voltage.

Once the voltage is reestablished the power restoration on the healthy part of the grid can start. Active power references of MMC2 and MMC3 are ramped up to the previous value as before fault event.

3.2. Simulation results

Simulation results of the primary sequence and converter breaker failure backup sequence are shown respectively in Figure 6 and Figure 7. From top to down there are: the currents at the MMCs output, the current through the breakers of the faulty line, the busbar voltages, the active and reactive power exchanged by the positive pole with the connected AC grids. The references for voltage and currents are the same as shown in Figure 1.

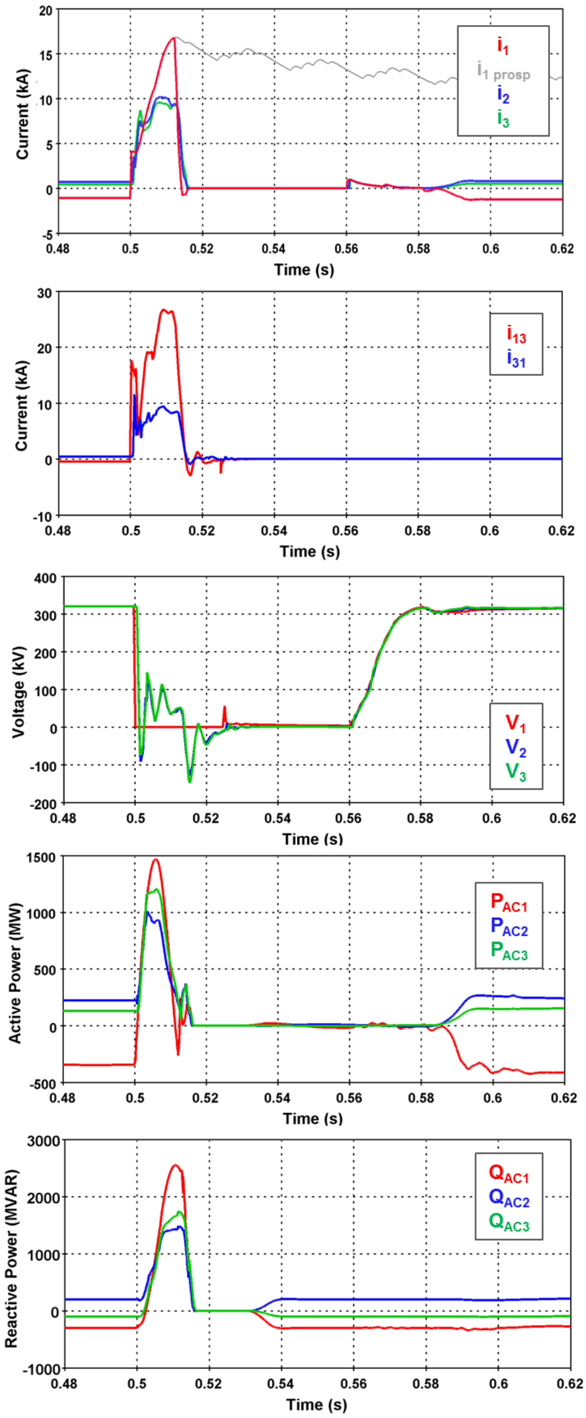

Figure 6 : Simulation results of primary sequence

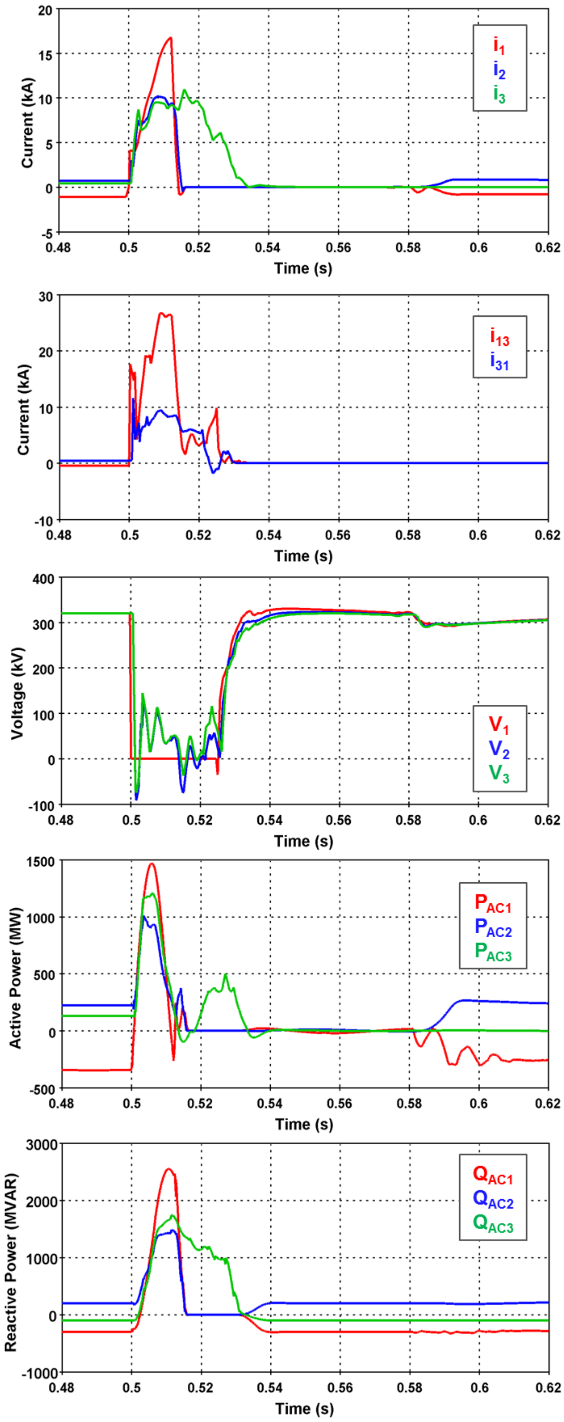

Figure 7 : Simulation results of converter breaker failure backup sequence

3.2.1. Primary sequence

After its propagation time, the fault, occurring at t=0.5s, is detected at each converter station. The MMCs immediately block and a tripping signal is sent to each corresponding converter DCCB. After the converter DCCB operation time (12ms), the fault current suppression starts, at around t=0.512s, rapidly bringing the current to zero. The current to be cleared by the converter DCCB is limited to the maximum contribution of one converter and reaches a value of less than 20kA, as it can be observed looking at the prospective fault current i_1, in Figure 6. Fault currents are much higher at line side, reaching around 27 kA in this particular fault scenario. The utilization of converter breakers to clear the fault avoid the need for line breakers with such high breaking capability. After the fault arrival at the line protective relay, the identification algorithm takes around 10ms to discriminate the faulty line. There is no need to perform an ultra-fast discrimination and a unit algorithm based on fault current direction calculation is considered acceptable. The line DCCB are therefore tripped at around t=0.51s and after the line DCCB operation time (12ms), the current suppression starts.
When converter currents are lower than a safety limit, the MMC are deblocked, at around t=0.53s and the reactive powers are ramped up at the previous values.
Once the reclosing time (50ms) is elapsed, the converter DCCBs reclose (10ms) and the grid voltage is restored to 1pu in around 20ms thanks to the PIR operation. At time t=0.58s, the power flow is resumed by ramping the P reference of converters from zero to pre-fault values in 10ms. The complete sequence lasts around 100ms.

3.2.2. Converter breaker failure backup sequences

In this case, it is assumed that the converter DCCB at the output of MMC3 fails to open. In Figure 7, it can be seen that MMC3 maintains the fault current contribution up to the opening of the line breakers which are tripped at around t=0.51s. Right after fault isolation, the voltage is restored because the MMC3 remains connected to the grid. The value of 0.7 p.u. comes from the fact that this converter is blocked. When the converter current at MMC3 output is lower than few amps, the HSS opens to isolate the converter from the grid.
The healthy converter DCCBs reclose at t=0.55s and the power is restored in the same way as for the primary sequence case. The backup sequence lasts around 100ms.

4. COMPONENT DESIGN

4.1. Converter Breaker and Line Breaker

The converter and line breakers need to be designed considering the maximum DC fault current contribution coming from a MMC converter when there is a short circuit at its terminals. Considering a design of arm inductances that allows a maximum short circuit current of 20 kA, the breaking capability of DC breakers is defined at this value. Because the converter output fault current is intrinsically limited, the breaker operation time can be fixed at 10-20ms without need of ultra-fast operation. Another related consequence is that DC limiting reactors in series with the breakers are not necessary, which entails a very low energy absorption requirement for the surge arrester in parallel with the breaker.

Table 3 : Requirements for DCCB

	Converter DCCB	Line DCCB
Breaking capability	20 kA	20 kA
Breaker operation time	10-20 ms	10-20 ms
DC limiting reactor	Not required	Not required
Surge arrester energy requirement	~ 1 MJ	~ 1 MJ
Open-close operation	O - 50ms - CO	O

The converter breakers need to be designed to perform very quick auto-reclosing sequences. The time duration between the opening and reclosing tripping signal has to be equal to the reclosing time of the primary sequence as described in §3.2.1, which has been set to 50ms. The breaker must be able to withstand reclosing on permanent faults, without damaging the pre-insertion resistor. Mechanical low-speed DC breakers could be compliant with the required technical specifications shown in Table 3.

4.2. High Speed Switch

The HSS of a breaking module has the aim to physically isolate the faulty line. The HSS could also embody the residual current breaker, which is necessary to extinguish the oscillating current that appears after DC breaker opening and which is due to the oscillation between the system inductance and the circuit breaker capacitance [8]. A fast operating standard breaking chamber with low DC interruption capability could fit the requirements shown in Table 4.

Table 4 : Requirements for HSS

	HSS
DC Breaking capability	Few A
AC Breaking capability	Few kA
Opening time	10 ms
Closing time	10 ms

4.3. Pre-Insertion Resistor

The proposed PIR topology to be used in series to each converter breaking module is shown in Figure 8. It is a variable resistor composed of two or more resistances R_n that can be short-circuited by parallel switches SW_n. The optimized number of resistances is determined in order to ensure a rapid grid voltage restoration and meanwhile limiting the inrush current due to cable charging. Simulation results, see Figure 6, confirms that for this particular benchmark grid a two-step PIR is appropriate in order to restore the voltage in less than 20ms and avoid inrush currents higher than 2pu of the rated MMC current. The chosen resistances R_1 and R_2 are respectively of value 200 Ω and 50 Ω while SW_1 and SW_2 are closed with a delay of 10ms and 20ms.

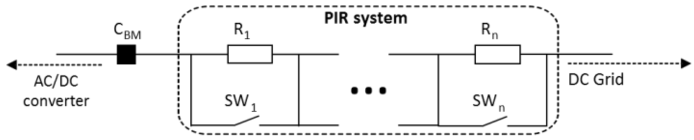

Figure 8 : Proposed topology for the PIR

5. AC SYSTEM IMPACT

When an MTDC or a part of it is embedded into an AC grid, a DC fault might lead to the loss of synchronism between interconnected areas. In this section, transient stability in case of a DC fault cleared by means of the converter breaker strategy is discussed. For this study, a three-terminal DC grid is supposed to interconnect two AC networks (AC1 and AC2) as shown in Figure 9. The system AC1 is composed of two synchronous areas (Area 1 and Area 2) connected through an AC line. When a DC fault occurs, power injections of the faulty pole are interrupted until the protection sequence is complete. Depending on the severity of the engendered power imbalance, synchronism between Area 1 and Area 2 can be lost. This study aims at showing the impact of the amount of DC power lost, the duration of the protection sequence and the inertia of the system, on transient stability of AC1.
For the assessment of stability as function of different parameters of the system, simplified models had been used. Therefore, each area has been represented by a synchronous generator described by its two-order analytical model and MMC stations are represented by constant power injections. In Figure 9, the power production of each area is noted P_{m1} and P_{m2}. Powers P_{L1} and P_{L2} describe the effect of the power consumption into the two areas. P_{MMC1} and P_{MMC2} are the power injected into the DC grid by each MMC station. Angle δ represents the voltage angle difference between both areas. X_l is the equivalent reactance of the group of AC lines interconnecting Areas 1 and 2.
In order to quantify the transient stability margins, the Critical Time to Return to Operation (CTRO) has been proposed in [11]. The CRTO is the maximum time during which the DC power can be interrupted

without the system losing its transient stability. The results of this chapter correspond to the CTRO in case of a DC pole to ground fault in a bipolar system. This kind of fault entails a loss of 50% of the DC transmitted power during fault clearing. Figure 10 shows the value of the CTRO calculated for different scenarios. Each scenario is determined by the value of the aggregated equivalent inertia H and the power transmitted through stations MMC1 and MMC2. The aggregated inertia H corresponds to the parallel sum of the inertia constants of the two generators, divided by the power exchanged between both regions [11]. The scenarios have been generated based on the following assumptions:

- The exchanged power between Areas 1 and 2 is incremented by increasing the production in Area 1 (P_{m1}) and the consumption in Area 2 (P_{L2});
- All the incremented production in Area 1 is transported through the MTDC grid. Additionally, the power supplied by MMC3 remains the same for all the scenarios. Therefore, the power incremented in Area 1 is absorbed by MMC1 and injected in Area 2 using the station MMC2.

An example of the characteristics of the system used for one scenario can be found in Table 5. The values marked with a star (*) vary in each evaluated scenario. For all cases, the pre-fault voltage angle difference δ_0 is set to 30 degrees, the power transmitted through the AC line is constant (3.2GW) and the power injected by the MMC3 remains the same (2GW). Additionally, for the sake of simplicity reactive power injections are set to zero for all cases.

Table 5 : Example of characteristics of the power system parameter for one scenario

	Area 1	**Area 2**
Production P_m	26.2 GW*	18.8 GW
Consumption P_L	17 GW	30 GW*
MMC station injected power P_{MMC}	6 GW*	-8GW*
AC Voltage	340 kV	340kV
Exchanged power through AC line P_{ac}	3.2 GW	
Pre-fault state voltage angle between regions	30 deg	

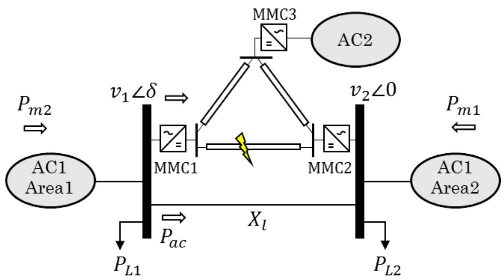

Figure 9 : MTDC and AC system test benchmark

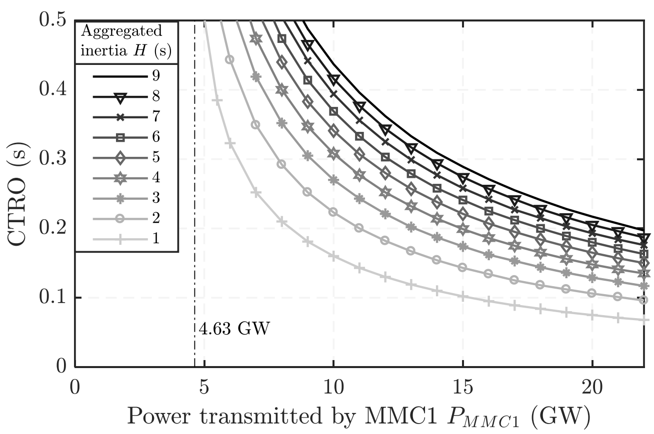

Figure 10: Critical Time to Return to Operation CTRO

From the results in Figure 10, it can be seen that stability margins are reduced when the power transmitted by the DC grid increases. This means that the power lost during the fault also increases. It must be also noticed that for low values of P_{MMC1}, no CTRO is found. This means that if the faulty pole is lost permanently, the system does not lose its transient stability, whereas the frequency stability could be lost. Indeed, there is a threshold value of P_{MMC1} for which the system remains stable regardless the aggregated inertia. For the studied power system, this is equal to 4.63GW. Additionally, it can be observed that the CTRO decreases when the aggregated inertia of the system decreases. In section 3 it has been shown that the proposed protection strategy lasts around 100ms for a complete restoration of the active power after fault occurrence. It can be observed that for a CTRO of 100ms the transient stability is lost only if the DC grid transfers an important amount of power, e.g. around 15GW for MMC1 (thus, -17GW for MMC2) with an aggregated inertia of 1s. Such a low value of inertia can be reached for example, if the new installed production in Area 1 is composed of renewable energy systems.

6. CONCLUSION

Several DC fault clearing methods have been suggested in literature in order to protect the DC grid against short circuit fault. Because of the severe impact of a fault on the behaviour of the DC system, namely very high fault currents and rapid voltage drops, those proposed methods are not limited to selective fault clearing strategy, as commonly performed in standard AC transmission protection scheme. The novel proposed protection method is a non-selective fault clearing strategy that eliminates the fault by means of DC breakers installed at each converter output.

The converter breaker strategy employs low-speed circuit breakers without using DC limiting reactors, therefore limiting their cost, complexity and easing interoperability aspects among DC breakers of different manufacturers. Moreover it facilitates the extensibility of the grid due to the fact that the DC breakers have to clear only the contribution coming from one converter.

It is a reliable strategy; simulations confirmed that the time necessary to bring back the power to the entire healthy grid is limited to about 100ms, even in case of breaker failure backup sequences.

Result from analytical calculations of DC fault impact on AC transient stability also proved that the proposed protection strategy is likely to be compatible with the requirements coming from a future DC grid embedded in the European AC system and transmitting a great amount of renewable power energy.

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