Full-Power Test of HVDC Circuit-Breakers with AC Short-Circuit Generators Operated at Low Power Frequency

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***Abstract*—This paper provides a pragmatic solution to the challenge of testing fault current interruption of high-voltage direct current (HVDC) circuit breakers (CBs). The critical parameters in the design of a test circuit capable of supplying the necessary stresses: current, energy and voltage (both during and after interruption) are discussed. In addition, a practical implementation of a test circuit based on ac short-circuit generators operated at low power frequency, which is capable of testing the current interruption performance of the proposed technologies of HVDC CBs, is discussed. Tests validating the proposed method and circuit have been conducted on a prototype of an HVDC CB and the test results are presented. Because the performance of some technologies of HVDC CBs can depend on the magnitude of the interrupted current, four test duties are defined and demonstrated in the paper. Moreover, testing of HVDC CBs using ac short-circuit generators poses new challenges such as the application of dielectric dc stress after current interruption, and the protection of both the test-object as well as the test-circuit components when the HVDC CB fails to interrupt. Methods to overcome these challenges are developed and practically demonstrated in a test laboratory. Finally, taking into account the available resources of the author's test laboratory, the capability to test multiple series-connected modules of different technologies of HVDC CBs is verified and example cases are demonstrated. Six short-circuit generators (13500 MVA @ 50 Hz) and up to ten step-up transformers (up to 550 kV) were actually used.**

***Index Terms*—HVDC circuit-breakers, HVDC short-circuit tests, HVDC Transmission, Multi-terminal, Test Circuit, Testing**

I. Introduction

HIGH-VOLTAGE dc circuit breakers (HVDC CBs) are expected to play an important role in the protection of multi-terminal and meshed HVDC grids [1]. Several concepts of HVDC CBs have been proposed and realized into prototypes [2]–[7]. A 200 kV hybrid type and a 160 kV active current injection type HVDC CB have been installed and commissioned at Zhoushan [8] and Nan'ao [9] radial, multi-terminal HVDC grids in China, respectively. The realization of the ±500 kV Zhangbei meshed HVDC grid, also in China, will initially include 16 HVDC CBs of different types [10]. However, to date no full-power tests of HVDC CBs performed at an independent and accredited test facility have been reported in the literature.

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Currently no international standards specifying test requirements of HVDC CBs exist. Generic test requirements have been derived from system studies carried out as part of the EU funded 'Progress on Meshed HVDC Offshore Transmission Networks' (PROMOTioN) project in [11], [13] which can be broadly classified into four categories: dielectric, operational, breaking and endurance tests. Among these tests, short-circuit current breaking/interruption tests are the most challenging.

Current interruption tests of HVDC CBs are complicated due to the requirement of supplying a range of sufficiently high rates-of-rise of fault current and subsequently a large energy stress. In [14] current interruption tests of HVDC CB performed as part of product development and the associated test circuits have been reviewed. A test circuit using ac short-circuit generators operated at low power frequency has been selected as the most favorable, especially when the duration of the interruption process is much shorter than the ac voltage half cycle [13], [14]. Moreover, ac short-circuit generators are already in use for ac equipment testing; therefore, without significant investment, these can readily be used for testing HVDC CBs.

The paper discusses the practical implementation of an HVDC CBs test method and its procedure using ac short-circuit generators operated at low power frequency. There are two major issues of using ac short-circuit generators for testing HVDC CBs: protection in case the test object (TO) does not clear the short-circuit current, and the application of dc voltage after current interruption for dielectric stress. Methods to overcome these challenges are developed and validated with experiments in a test laboratory. Because the interruption performance of some technologies of HVDC CBs can depend on the magnitude of the interrupted current, it is necessary to perform tests with current magnitudes ranging from load current to the maximum interruption capability. Four different test duties have been defined and tests were conducted accordingly. Then, the dc current interruption performance of a mechanical HVDC CB composed of a high-voltage vacuum interrupter with active current injection is analyzed. The contribution of this paper can, thus, serve as a starting point for standardization of testing methods and procedures for HVDC CBs.

The remainder of the paper is organized as follows. In Section II temporal stages of current interruption process of HVDC CB are discussed. In Section III, background of current interruption test requirements as obtained from system studies is briefly described. A theoretical analysis of a test

circuit based on ac short-circuit generators and the practical implementation of this test circuit are presented in Section IV and in Section V, respectively. In Section VI, the performance demonstration of the test circuit is presented along with test results of a prototype HVDC CB. Section VII provides discussion on the challenges of testing multi-module HVDC CBs and the inherent limitations of the author's test facility. Finally, the conclusions based on the results of the paper are presented in Section VIII.

II. Stages of Current Interruption Process to be Verified

In [11] qualitative test requirements of HVDC CBs based on system simulation studies are presented. The key design parameters of HVDC CBs which need to be verified during a (type) test are discussed. In this section, the critical temporal parameters to be verified during a test are presented combined with their definitions and other terminologies related to the operation of HVDC CBs as proposed in [15]. These terminologies are described with reference to Fig. 1.

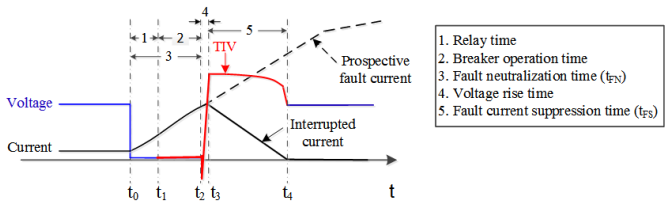

Fig. 1. Diagram for illustration of timing definitions and terminologies related to HVDC CB operation.

Relay time – the time interval between fault inception and the sending of trip order to the HVDC CB, (from t_0 – t_1, in Fig. 1). Although this is a characteristic of the protection system and is not part of the test requirements of the HVDC CB, it has a significant impact on the interrupted current. During a test, the trip signal is sent by the test circuit and fully controllable. If the HVDC CB has self-protection functionality, this can be tested separately.

Breaker operation time – the time interval between the reception of the trip order and the beginning of the rise of the the transient interruption voltage (TIV), (from t_1 – t_2, in Fig. 1). This determines the speed of operation of the HVDC CB which is an important parameter for the envisaged application in an HVDC grid. Thus, it must be clearly noted during tests.

Fault neutralization time (t_{FN}) – the time interval between fault inception and the instant when the fault current starts to decrease, (from t_0 – t_3, in Fig. 1). This is important from system perspective since at the end of this time the system voltage starts to recover.

Voltage rise time – the time required to build the TIV, (from t_2 – t_3, in Fig. 1). The rate-of-rise of the TIV is important because the mechanical switching device's dielectric recovery speed must be coordinated with this.

Fault current suppression time (t_{FS}) - the time interval between the peak of the interrupted fault current and the instant when the current has been suppressed to zero (arrester leakage) current level, (from t_3 – t_4, in Fig. 1). This time depends on several system and CB related parameters. From the CB perspective, two events take place during this period. The HVDC CB absorbs magnetic energy stored in the system's inductance and the TIV sustained by the surge arrester appears across the HVDC CB during this period. From system perspective, the voltage recovers during this period.

Transient Interruption Voltage (TIV) – the voltage that the HVDC CB generates during current interruption, see the red trace in Fig. 1. During a test, the HVDC CB must clearly demonstrate this voltage which is higher than the rated operation voltage of the CB with sufficient margin. 50% margin has been suggested as typical compromise between system insulation coordination and CB performance.

Rated short-circuit breaking current – The maximum current that the HVDC CB can interrupt within a specified breaker operation time.

These and other more terminologies are described in detail in [15].

III. Brief Review of Background from DC Grid Fault Transient Study

In order to define the test requirements, multi-terminal HVDC (MTDC) grid fault studies have been reported in a previous publication, [11]. Interactions of different technologies of HVDC CB with the HVDC grid during fault current interruption are investigated in [16]. To define a test current that must be supplied by a test circuit, fault current envelopes for different topologies of voltage source converters (VSCs) under various fault conditions are derived in [17]. The focus in the latter study is mainly the fault current supplied by a single converter. However, there are several other contributions to a fault current in an MTDC grid [18].

Fig. 2 shows simulation current and voltage during a pole-to-ground fault in a MTDC grid built from bipolar modular multi-level converter (MMC) based VSCs. The left and right y-axes are for current and voltage traces, respectively. A fault occurs on a cable connected to a dc bus where not only a converter is connected but also two incoming cables from remote converters [13]. Initially the system is at steady state with nominal/load current and nominal system voltage.

The proposed technologies of HVDC CBs require a series current limiting reactor to reduce the rate-of-rise and hence, within the breaker operation time, limit the magnitude of the fault current to within the interruption capability. A 150 mH reactor is used in series with the active current injection HVDC CB in the simulation result shown in the figure. In fact several factors determine the rate-of-rise and magnitude of fault current in an HVDC grid which include the strength of the connected ac network, the converter short-circuit impedance (transformer and arm reactor), system grounding, number of incoming lines connected to the same dc bus, the location and distance of a fault, the fault resistance, etc. [11], [19].

Considering Fig. 2, a pole-to-ground fault is applied at t_0 which is instantly followed by a steep rise of the current. The detail of fault current development and sequence of events following a fault in a MTDC grid is presented in [11], [20].

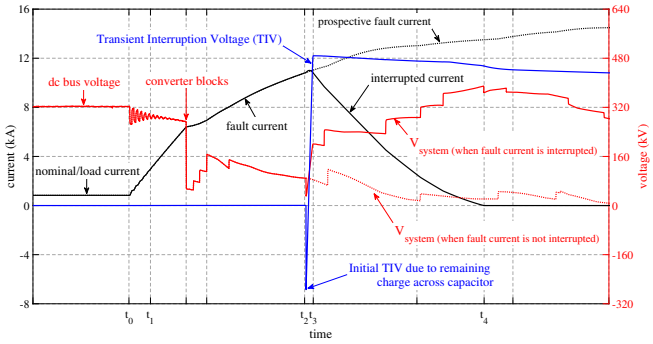

Fig. 2. Simulation fault current, dc bus voltage and TIV during dc fault interruption by active current injection HVDC CB

The dotted traces in the figure show the resulting current and voltage when no action is taken by the HVDC CB and/or the protection system. The traces by solid lines show simulation results when the HVDC CB successfully clears the fault current. At t_1 a fault is detected and a trip command is sent to the HVDC CB on the faulted cable. This marks the beginning of the breaker operation time. At t_2 the breaker is ready to withstand the TIV, thus the fault current is commutated to the energy absorbing branch (metal oxide surge arrester (MOSA) banks). From this moment on, the MOSA voltage (TIV) suppresses the fault current until it reaches a leakage level that can be cleared by a series residual current breaker at t_4.

It must be noted that the system voltage recovers from the moment the fault current is commutated to the MOSA branch, i.e. the moment the HVDC CB builds the TIV. Thus, there is significant contribution of electrical energy from the system during the current suppression period. The step changes on the system voltage observed after converter blocks is due to the commutation overlaps in the converter arms caused by arm reactors. In other words, more than one upper or lower converter arms are conducting at a time resulting in average voltage between conducting phases. The steps in the system voltage occurs when one of the arms ceases to conduct [11].

The HVDC CBs are typically realized by connecting several modules in series to achieve high-voltage rating. Interruption tests can be performed on a single module or multiple modules. When performing tests on a single module, equivalent stresses that would appear across a single module which form part of a full-pole HVDC CB must be considered [11], [21]. In some cases, pre-conditioning of the HVDC CB, such as pre-heating semi-conductor switches, to mimic worst case normal service conditions is necessary.

IV. Test Circuit Design Based on AC Short-Circuit Generators: Theoretical Analysis

In [14] it was shown that a test circuit based on ac short-circuit generators operated at low power frequency can be used for testing the fault current interruption and energy absorption capability of HVDC CBs. In this section the design consideration of such a test circuit is discussed. Fig. 3a shows a simplified schematic with the necessary circuit elements ac voltage source, Master Breaker (MB), Making Switch (MS), circuit impedance (R and L) and test object (TO). The ac short-circuit generators are represented as a simple ac voltage source behind impedance.

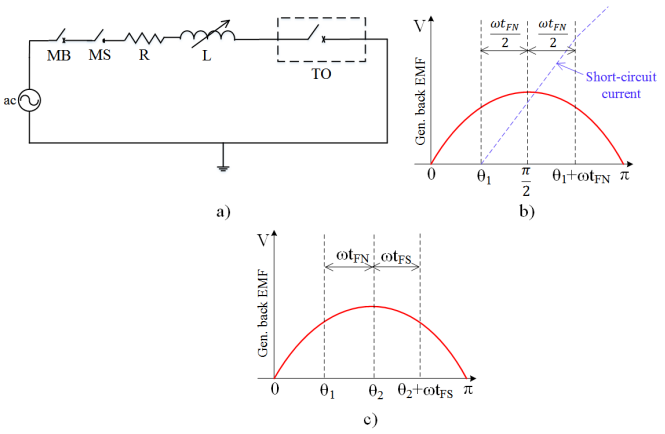

Fig. 3. a) Simplified schematic of HVDC CB test circuit supplied by ac source b) Voltage waveform, making angle for maximum rate-of-rise of current during fault neutralization period, c) Optimized making angle for rate-of-rise of current and energy absorption

Referring to Fig. 3a, the fundamental equation during fault neutralization time (t_{FN}) is

$$\hat{V}\sin(\omega t+\theta_1) - Ri(t) - L\frac{di}{dt} = 0 \tag{1}$$

where $\omega = 2\pi f$, and f is the ac generator power frequency, θ_1 is the making angle (a point in time on the voltage wave when a short-circuit is applied, see Fig. 3b), R is the parasitic resistance in the circuit and L is the equivalent inductance in the circuit. The maximum average rate-of-change of current (di/dt) over t_{FN} is obtained when $\theta_1 = \pi/2 - \omega t_{FN}/2$, see Fig.3b. The solution of (1) is,

$$\begin{aligned} i(t) = I_m\left[\sin(\omega t+\theta_1-\phi) - \sin(\theta_1-\phi)\exp(-t/\tau)\right] \\ +I_o\exp(-t/\tau) \end{aligned} \tag{2}$$

where $I_m = \frac{\hat{V}}{\sqrt{R^2+(\omega L)^2}}$ is the peak value of symmetric current, $\phi = \tan^{-1}(\omega L/R)$ is the phase angle, $\tau = L/R$ is the circuit time constant and I_o (if it exists) is the value of the initial current flowing at the moment when the short circuit is applied.

Assuming a negligible voltage rise time, the peak interrupted current is $I_p = i(t_{FN})$ with $i(t)$ as in (2). The moment the HVDC CB starts to generate the TIV, it starts to absorb energy. This marks the beginning of the fault current suppression (t_{FS}) period. The circuit equation during this period becomes,

$$\hat{V}\sin(\omega t+\theta_2) - Ri(t) - L\frac{di}{dt} - V_{CB} = 0 \tag{3}$$

where V_{CB} is the TIV of the HVDC CB. Since the same ac source is supplying power during both t_{FN} and t_{FS} periods, $\theta_2 = \omega t_{FN} + \theta_1$, see Fig. 3b, where the time reference is changed to the beginning of t_{FS} for mathematical convenience.

The energy absorption branch of the HVDC CB is assumed to have sufficient number of parallel MOSA columns to absorb

the energy stress with each column operating in a highly non-linear region of its *I–V* characteristics. Thus, (3) can be solved by assuming constant TIV during t_{FS} and the solution is expressed as,

$$i(t) = I_m\left[\sin(\omega t + \theta_2 - \phi) - \sin(\theta_2 - \phi)\exp(-t/\tau)\right] + I_p\exp(-t/\tau) - \frac{V_{CB}}{R}(1-\exp(-t/\tau)) \quad (4)$$

From the solution in (4), the duration of t_{FS} can be determined numerically by setting $i(t) = 0$ and solving for t. The energy that the HVDC CB absorbs during t_{FS} can then be estimated analytically as follows,

$$E = \int_0^{t_{FS}} V_{CB} i(t)dt = \frac{1}{2}LI_p^2 + \int_0^{t_{FS}} \hat{V}\sin(\omega t + \theta_2)\, i(t)dt \quad (5)$$

Where $i(t)$ is given by (4). The energy in (5) is contributed by two sources; the energy stored in the circuit inductance at the beginning of the fault suppression time ($\frac{1}{2}LI_p^2$), and the energy being supplied by the source (ac short-circuit generators) during the fault suppression time. The latter corresponds to the energy supplied by the HVDC grid as system voltage recovers as discussed in Section III and in detail in [11], which in most of the cases is larger than the former.

Similar to the maximally achievable di/dt during t_{FN}, the maximum energy that can be supplied by the source is achieved when $\theta_2 = \pi/2 - \omega t_{FS}/2$. A further increase in supplied energy can be realized by prolonging the availability of the ac source voltage by lowering the power frequency. The lower the frequency the more the energy that can be supplied by a source. Thus, for a given fault neutralization time, a making angle of $\theta_1 < \pi/2 - \omega t_{FN}$ is a good compromise between di/dt as well as energy, see Fig. 3c. This entails that the power frequency of a test circuit must be chosen such that $t_{FN} > 1/(4f)$. It must be noted that the ac source voltage is not directly applied to the HVDC CB during current interruption. However, it follows from the above analysis that it is a crucial test circuit design parameter during both periods and its magnitude must be carefully determined and distributed over both periods.

It is mentioned in the introduction section that the test circuit based on ac short-circuit generator is the most suitable and the test circuit components are readily available in most ac short-circuit test laboratories. However, this method in itself is not complete and additional features such as the ability to apply dielectric DC voltage stress after current suppression are required to enable safe and comprehensive testing of the short-circuit current interruption performance of HVDC CBs. This is discussed in detail in the next section.

V. Implementation and Description of the Test Circuit

A schematic of the full test circuit based on ac short-circuit generators is shown in Fig. 4. The test circuit is composed of four parts; namely, a power source, over-current protection, a dc voltage source for dielectric stress and an arcing time prolongation circuit, each of which are indicated in separate dashed boxes. The purpose of each part is described separately in this section.

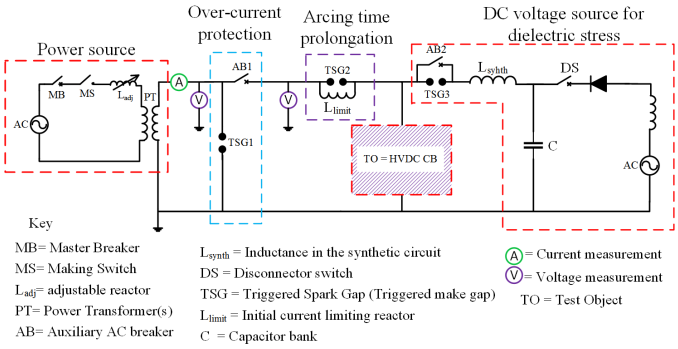

Fig. 4. Schematic of complete test circuit for testing short-circuit current interruption performance of HVDC CBs

A. Power source

This is the short-circuit power source supplying the necessary current, voltage and energy stresses during the current interruption. It consists of a parallel combination of ac short-circuit generators and power transformers capable of operating at low power frequency. The short-circuit generators have a master breaker (MB) and a making switch (MS) in each phase, see Fig. 4. For testing HVDC CBs, only half a cycle of ac current is needed. The MSs are used to control the making angle (θ_1) whereas the MBs clear the power source at first power frequency current zero.

When operating short-circuit generators at low power frequency, the generated voltage and hence the available power are reduced proportionally. Therefore, multiple series-connected power transformers are needed to step-up the test voltage to a desired level[1] and several short-circuit generators are connected in parallel to compensate for the reduced current at the transformer's high-voltage terminal (a typical connection of multiple generators and transformers is shown in [14]). The generator sub-transient reactance and the transformer leakage reactance together with the adjustable reactors (L_{adj} in Fig. 4) constitute the total inductance in the circuit needed to realize the rate-of-rise of current and energy to be absorbed by the HVDC CB.

B. Over-Current Protection

If the test-object (TO) for any reason does not operate or clear, it will be subjected to the full prospective half cycle current from the power source (until the MB clears). This could result in the damage to the TO and/or to the components of the test installation. To mitigate this risk, additional circuitry has been implemented – see the dashed box labeled protection in Fig. 4. It consists of a plasma triggered spark gap bypass (TSG1) and an auxiliary HVAC SF_6 breaker (AB1).

The triggered spark gap (TSG1) is controlled by a real-time current level detector which sends a firing signal if the pre-set threshold value is exceeded. During the actual test, the auxiliary breaker is always tripped together with the TO because it needs to provide galvanic isolation between the

[1]The desired level does not necessarily mean the rated voltage of the HVDC CB but a voltage sufficient to produce the needed current and energy stresses corresponding to a certain test duty.

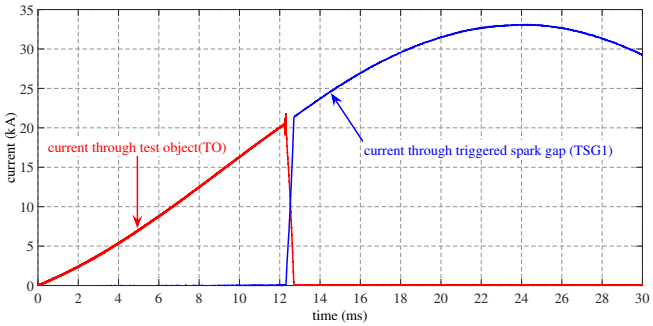

Fig. 5. Demonstration of successful over-current protection by triggered bypass spark gap in parallel with the test breaker. The spark gap TSG1 receives a triggering signal when an over-current of 20 kA is detected

power source and the TO after the current is interrupted. If galvanic isolation is not provided by AB1, the ac source and the DC voltage source interact, thus making it difficult to maintain a DC voltage supply to the TO after current suppression. It could also cause damage to the DC voltage source installation. Therefore, when TSG1 is fired due to over-current detection, the arc voltage of AB1 enhances the current commutation from the TO to the TSG1[2] This is demonstrated in the test laboratory as shown in Fig. 5. In the results shown, the generator produces a current with a prospective peak of 33.5 kA and the detection threshold of the level detector is set at 20 kA.

C. DC Voltage Source for Dielectric Stress Application

When in service, the HVDC CB is subjected to the system voltage (dc) immediately after current interruption. In a test circuit supplied by ac short-circuit generators, this voltage must be provided by a separate source. Using a similar principle as for synthetic testing of HVAC CBs, a dc voltage can be applied, for example, from a charged capacitor bank as shown in Fig. 4. However, unlike for HVAC CBs where the moment of current zero is determined from circuit parameters and power frequency, for HVDC CBs the instant at which the dc voltage should be applied cannot be precisely determined in advance. Thus, the post-current-suppression current-zero of the HVDC circuit breaker line current, i.e. the current through AB1, must be accurately detected in real-time.

For precise timing, the dc voltage is applied first by firing triggered spark gap TSG3 (upon current-zero detection), see dashed box labeled as dielectric source in Fig. 4, causing a charge balancing current to flow from dielectric voltage source to the HVDC CB. To ensure dielectric stress when this current ceases to flow through TSG3, a pre-triggered HVAC CB (AB2 in Fig. 4) in parallel with TSG3 is bypassing TSG3 shortly after firing.

Fig. 6 shows test results demonstrating the method of applying dc dielectric stress after current interruption. This was performed on a capacitor (C1) as a TO in the test laboratory in the absence of an HVDC CB. The schematic of the test circuit

[2]The arc voltage of AB1 does not affect the test current and voltage. The arc voltage of AB1 is in the order of a few hundred volts. This can be compensated for by slightly increasing the source voltage magnitude.

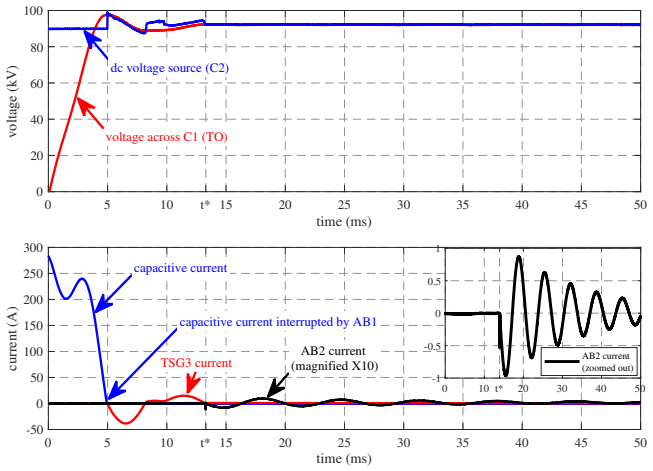

Fig. 6. Experimental demonstration of DC voltage stress application right after current interruption

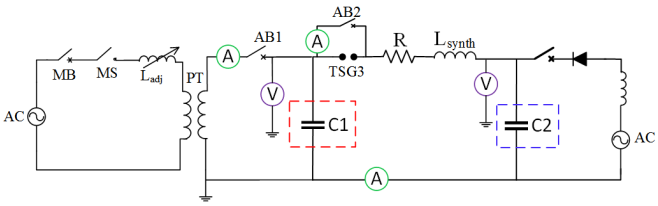

Fig. 7. Schematic of a test circuit for demonstration of DC voltage stress application method to HVDC CBs after current suppression

used for this demonstration is shown in Fig. 7. This is based on the fact that the proposed HVDC CB technologies constitute capacitors either in the form of snubber circuits and/or as a pre-charged capacitor for counter current injection. This capacitor is charged to the same voltage as the TIV during fault current suppression. In order to mimic the actual situation during current suppression, capacitive load current is interrupted by AB1 as shown in Fig. 7. In this case, the capacitor C2 is used to represent the dc voltage source and is initially pre-charged whereas the capacitor (C1) is used to represent the capacitance of the HVDC CB. When the current is interrupted by AB1, C1 is charged to the peak value of the ac source voltage which is 100 kV, corresponding to the value of the TIV of an HVDC CB module at the end of the fault current suppression time. The test was combined with real-time current-zero detection where the interruption of the short-circuit current from the generator is detected. This must not be confused with local current zero in the main current path of the HVDC CB[3]. Hence, upon detection of current interruption (current-zero at 5 ms in Fig. 6), a triggered spark gap TSG3 is fired. This results in current conduction of TSG3 due to the voltage difference between the two capacitors. The dc voltage source capacitor (C2) is pre-charged to 90 kV. A relatively large impedance (L_{synth})[4] is used to limit the oscillating current between the two capacitors,

[3]The operation of the test circuit does not rely on the internal measurements of the TO

[4]In addition, (L_{synth}) is chosen to be large enough to limit current flowing into the capacitor bank of the DC voltage source in case AB1 fails to isolate the generator side from the rest of the circuit.

C1 and C2. This current is shown by the red trace labeled TSG3 current in Fig. 6[5]. During arcing of TSG3 the auxiliary breaker AB2, tripped in advance, closes at t^*, see Fig. 6. Then, a small residual charge exchange current (< 1 A) continues to flow as shown in the figure (magnified X10 for visibility) or see the actual current measurement in the zoomed plot on the bottom graph of Fig. 6.

D. Arcing Time Prolongation in the Auxiliary Breaker

AB1 provides galvanic isolation between the power source and the TO after current interruption, enabling the application of dc voltage stress to the TO from another source. Thus, AB1 is subjected to a differential voltage between the ac generators and the dc voltage source applied to the TO after current interruption. For AB1 to provide such a functionality, it must have already gained sufficient arcing duration by the time the TO suppresses the short-circuit current. In addition, AB1 has a duty of interrupting a residual current or (in some cases) an oscillating current that remains after the short-circuit current is suppressed by the TO.

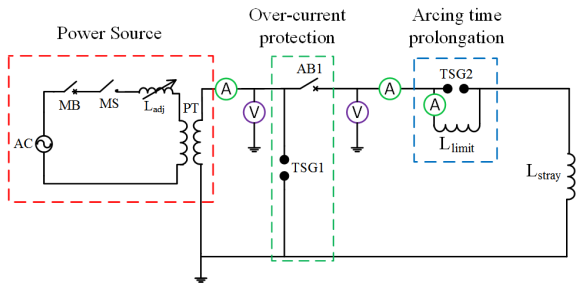

Fig. 8. Schematic of a part of the test circuit used for demonstration of arcing time prolongation

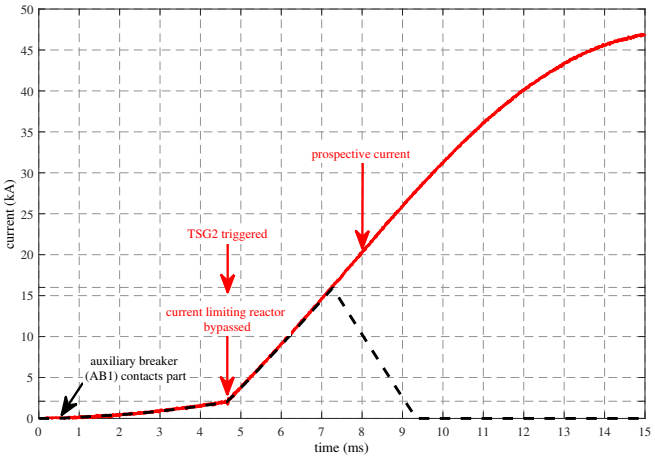

Fig. 9. Experimental demonstration of arcing time prolongation in the auxiliary breaker combined with verification of over-current protection

Any HVAC CB has a minimum arcing time before it can interrupt and isolate. For most HVDC CBs, the total interruption time ($t_{FN} + t_{FS}$) is shorter than the HVAC CB minimum arcing time, so arcing in the HVAC CB must start before HVDC CB operation. Thus the arcing time of AB1 must be prolonged artificially by postponing the trip order to the TO whilst ensuring a flow of current through AB1. This is demonstrated in the test laboratory with the test circuit schematic shown in Fig. 8. The test result is depicted in Fig. 9. The making switches (MS) are closed at the beginning of the source voltage half cycle before AB1 is opened at 0.7 ms when about 80 A current is flowing. For a certain duration, an additional reactor, L_{limit}, is inserted in series (see, the dashed box labeled as arcing time prolongation in Fig. 4) to let AB1 reach its minimum arcing time at a current level near the normal load current of the HVDC CB. Then, at 4.7 ms, or at the desired making angle (θ_1), the actual short-circuit current is initiated by bypassing this reactor by a triggered spark gap TSG2, causing the current to start to rise at the required d*i*/d*t*, in this particular case at about 5.5 kA/ms. In this way additional arcing time of 4 ms is gained for the AB1.

VI. PERFORMANCE DEMONSTRATION OF THE TEST CIRCUIT

The HVDC CB with active current injection scheme is composed of a vacuum interrupter in the main current path and a series connection of a pre-charged capacitor and a reactor in parallel to the vacuum interrupter [6]. A MOSA stack is connected in parallel with the injection capacitor to limit the TIV and absorb the magnetic energy stored in the system. An artificial current zero through the vacuum interrupter is created by closing a high-speed making switch which can be achieved within 8 ms from the trip command [21]. The capacitor and the reactor determine the frequency (in the order of several kHz) and, together with the pre-charging voltage determine the magnitude of injection current.

A. Test set-up

The test set-up with a 80 kV prototype of an active current injection HVDC CB is shown in Fig. 10. The parts of the HVDC CB include high-voltage vacuum interrupter and the high-speed making switch contained in one enclosure, current injection capacitor bank, current injection branch reactors, MOSA and the HVDC CB control cubicle.

The triggered spark gap (TSG1) and the auxiliary ac CB (AB1) shown in Fig. 10 are part of the test circuit, not the test breaker.

B. Test procedure

To verify the performance of the HVDC CB when interrupting various current magnitudes, four test duties named as T100, T60, T30 and T10, shown in Table I are defined. Before the actual test of the HVDC CB, the test circuit parameters are set for a specific test duty, as noted in Table I. Initially the test circuit parameters are designed to supply energy not exceeding 1.5 MJ[6]. To control (and limit) the energy dissipated

[5]The duration of current conduction through a spark gap very much depends on the voltage difference at the moment of dielectric injection, gap length of the spark gap itself, the impedance between the two capacitors and the differences between the capacitances as well.

[6]The motivation is to perform as many tests in the available short duration of time, because multiple short-interval energy injection leads to accumulative temperature rise

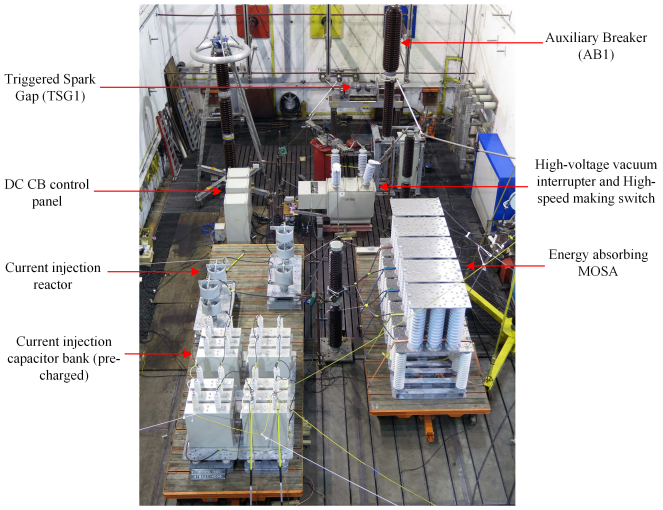

Fig. 10. Test set-up of prototype active current injection HVDC CB (supplied by MEU–Mitsubishi Electric Europe) tested at KEMA Laboratories.

in the breaker, the source voltage is initially adjusted to 19 kV peak. Later, when 4 MJ energy dissipation is demonstrated, the source voltage is raised to 40 kV while increasing the circuit inductance proportionally to keep the test current at the same level, see Table I.

TABLE I
TEST CIRCUIT COMPONENTS AND PARAMETER VALUES FOR VARIOUS TEST DUTIES AT 16.7 HZ POWER FREQUENCY OF A TEST CIRCUIT

Test Duty	Inductance (mH)	Current(kA)	Energy (MJ)
T100	10.5	16	1.5
T60	16.7	10	1.0
T30	33.4	5	0.5
T10	167.2	2	0.5
T100	20.5	16	4

For each test duty, a prospective current is demonstrated first with the TO remaining in closed position. The aim is to verify the desired making angle (θ_1) as well as the rate-of-rise of a test duty current so as to adjust the timing of a trip signal to the TO. For each test duty, bidirectional current interruption tests were conducted.

C. Test Results

Fig. 11 shows test results of test duty T100 (16 kA) current interruption both in the forward and reverse direction. The prospective current is superimposed in each graph for comparison. In both tests, the current injection capacitor of the TO is charged with the same polarity. The current through the vacuum interrupter of the TO is depicted in each graph as well. As can be seen from Fig. 11c, in the case of reverse current interruption, the injection current is superimposed onto the short-circuit current through the vacuum interrupter in the first half cycle and then creates current zero in the next one.

During both the forward and reverse current interruption tests, the TO suppresses the current from just over 16 kA which would otherwise increase to a peak value of 33.5 kA. During some of these tests the auxiliary breaker AB1 is intentionally kept in a closed position. Since at this step the main focus is on current interruption, the dc voltage stress after current suppression is not applied to the prototype HVDC CB. Hence, after current is suppressed by the TO, there is an oscillation of a few hundreds of Hz due to the interaction between the charged capacitor of the TO and the inductance in the test circuit. In a practical operation in an HVDC grid, this is prevented by the residual current breaker which is connected in series with HVDC CB. The traces in Fig. 11b) and d) show the TIV generated by the TO during the energy absorption time[7]. The high-frequency oscillation observed at the peak of the TIV is due to stray inductance in the loop between the capacitor and the MOSA of the TO.

Fig. 12 depicts T60 (10 kA) and T10 (2 kA) current interruptions. Similarly, bidirectional current interruption were conducted at these test duties as well. It is clear from Fig. 12 that the TO successfully interrupted the low duty currents as well. For test duty T10 (Fig. 12c and d), AB1 is tripped simultaneously with the TO and clears the previously mentioned post current suppression oscillating current. Instead, a decaying dc voltage (see Fig. 12d) can be observed after current suppression which is due to the charge trapped in the TO's injection capacitor at the moment the current is suppressed to zero. Initially this is considered to provide dielectric stress after current interruption; however, this is against best test practice since this stress is produced by the TO itself and not by an external test circuit, as in service. Nevertheless, it can be seen that AB1 is providing galvanic isolation between the power source and the TO thus, making it ready for dc dielectric voltage stress application as described in Section V.

Another observation from the TIV traces in Fig. 11 and 12 is the increasing residual charge voltage across the injection capacitor (with decreasing interruption current) at the moment of local current zero creation in the vacuum interrupter. Upon local current interruption, this voltage appears immediately across the vacuum interrupter and is higher during the lower current interruption duties, e.g. T10. This observation, in fact, is the rationale of including this duty.

In Fig. 13 T100 (16 kA) current interruption test results where 4 MJ energy is absorbed is shown. This is achieved by adjusting the test parameters as mentioned in the preceding subsection. In this case, AB1 is also tripped in parallel with the TO and hence, the dc voltage due to trapped charge across the TO's injection capacitor after current interruption is observed. An important observation from this test result is the duration of the TIV. The TIV of more than 110 kV is maintained for about 4 ms, thus stressing the TO as well as the test circuit for the same time as an inherent dielectric stress part of the test.

VII. CAPABILITY AND CHALLENGES OF TESTING MULTI-MODULE/FULL-POLE HVDC CIRCUIT BREAKERS

The test results of HVDC CB prototypes reported in the technical literature are mainly demonstrations of performance of local current-zero creation of single module breakers rated

[7]The vacuum interrupter is arcing from the moment of contact separation until local current zero. However, due to the low vacuum arc voltage, in comparison to the peak TIV, this is not visible in the oscillograms.

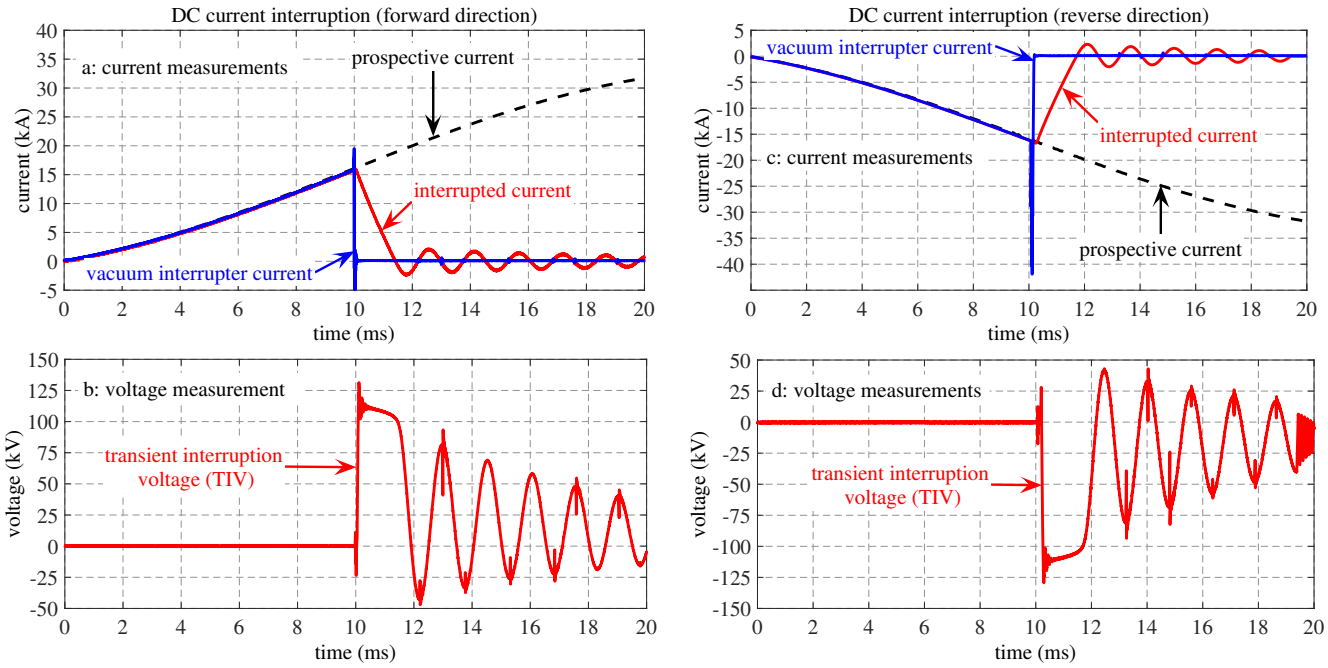

Fig. 11. 16 kA (T100) bidirectional DC short-circuit current interruption test results of active current injection HVDC CB in a test circuit supplied by short-circuit generators at 16.7 Hz. The dashed trace shows prospective current

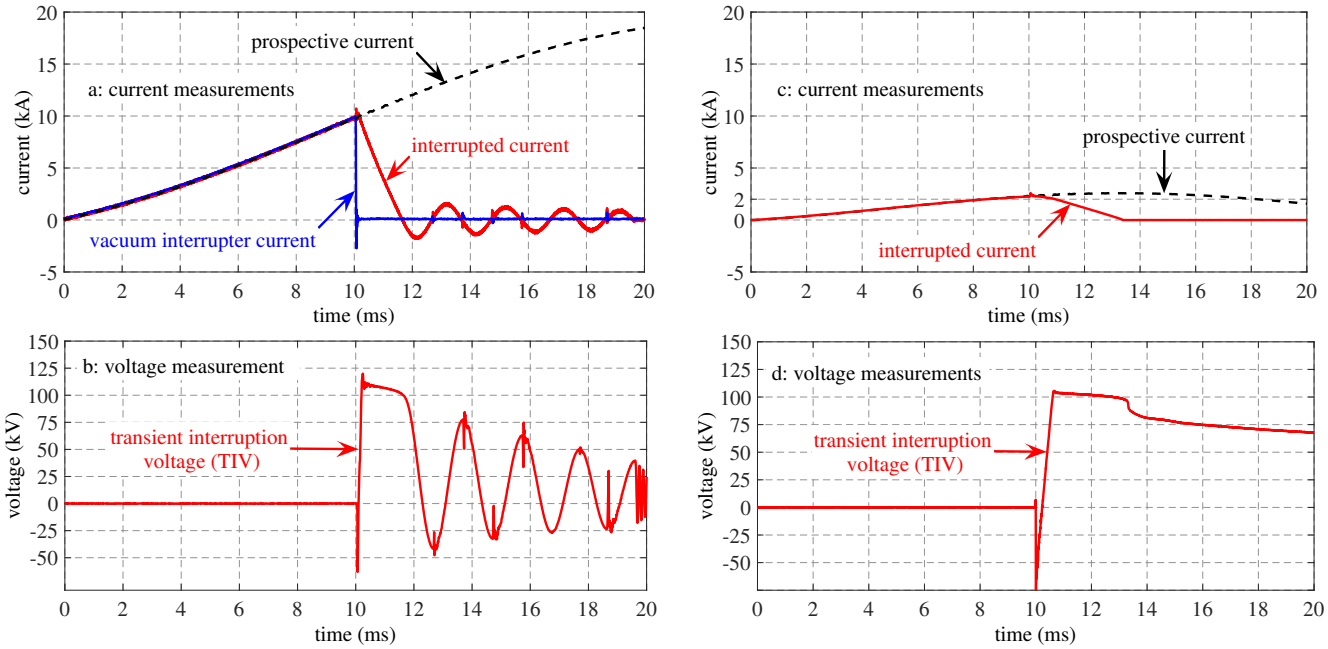

Fig. 12. T60 (10 kA) and T10 (2 kA) current interruption test results of active current injection mechanical HVDC CB in test circuit supplied by short circuit generators at 16.7 Hz.

for 80–120 kV. However, it is essential to verify the complete interruption process of a full-scale equipment. There are two main requirements the test environment must fulfill to test a multi-module/full-pole HVDC CBs. First, it needs to have sufficient power to supply the rated stresses: current, energy and voltage. Second, and a unique challenge of testing HVDC CB is that, the test installation should be able to withstand the TIV generated by a full-pole HVDC CB.

In addition, although the first requirement can be met by availability of short-circuit power for testing, a lot depends on the parameters of the HVDC CB; e.g., the breaker operation time and the energy rating. The breaker operation time along with the maximum current to be interrupted dictate the di/dt of the current whereas the energy rating dictates the magnitude of source voltage and power frequency, as discussed in Section IV.

Considering the actual installation at KEMA Laboratories with up to six short-circuit generators (of 2250 MVA each

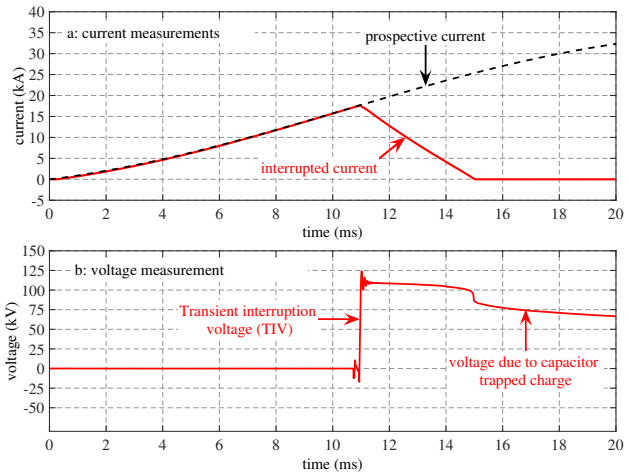

Fig. 13. Demonstration of 4 MJ energy absorption when interrupting T100 forward current

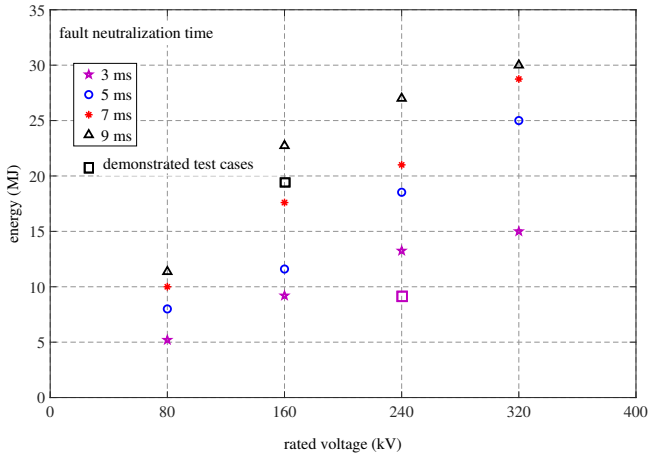

Fig. 14. Maximum energy supply versus voltage ratings considering different technologies of HVDC CBs at KEMA laboratories. This is considering 16 kA rated short-circuit breaking current.

at 50 Hz) and 550 kV (rms) insulation level, the maximum energy that can be supplied to different technologies of HVDC CB at different rated voltages is depicted in Fig. 14. Four HVDC CB technologies with breaker operation times of 2, 4, 6 and 8 ms, and capable of interrupting 16 kA are considered. For all the cases it is assumed that TO receives a trip signal 1 ms after short-circuit making resulting in the fault neutralization times shown in the figure and current with di/dt in the range of 1.8–5.3 kA/ms. Except for a few cases (at higher rated voltage) where it is not possible to achieve the desired di/dt at a desired voltage, the peak values of the source voltage are adjusted to the same value as the rated voltage. It can be seen that the maximum energy that can be supplied to the HVDC CB depends on the CB parameters. For example, at rated voltage of 320 kV, up to 30 MJ can be supplied to an HVDC CB with breaker operation time of 8 ms whereas up to 15 MJ can be supplied to a CB having 2 ms breaker operation time.

Several example cases have been demonstrated at the test laboratory of which two cases are shown in Fig. 15. These results are obtained by operating six short-circuit generators at 30 Hz and 16.7 Hz in a) and b), respectively. The test in Fig. 15a) is performed considering a HVDC CB, with breaker operation time of 2 ms, rated for 200 kV and above. Prospective current with a rate of rise of 5 kA/ms is achieved in this case. If an HVDC CB rated for 240 kV (three 80 kV breaker modules) is tested with this test set-up and 16 kA is interrupted, about 10 MJ of energy needs to be dissipated by the breaker.

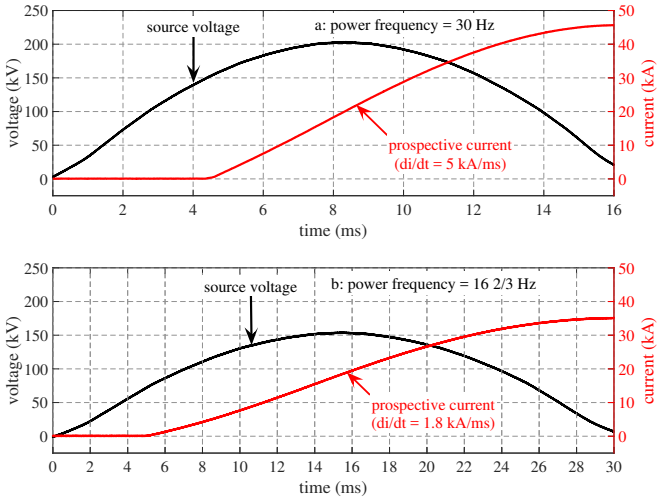

Fig. 15. Demonstration of prospective current at different voltage considering various technologies of HVDC CBs having different breaker operation times.

Similarly, the test result in Fig. 15b) is conducted considering HVDC CBs having breaker operation time of 8 ms. The prospective current having di/dt of 1.8 kA/ms is obtained using a source voltage of 155 kV peak. This means, at least two HVDC CB modules each rated for 80 kV can be tested with the test set-up used in the demonstration. For example, assuming an HVDC CB rated for a 160 kV system, 20 MJ needs to be absorbed by the HVDC CB when interrupting 16 kA. It must be noted that the same test set-up can be used for testing HVDC CBs with higher voltage rating, except a smaller amount of energy is absorbed in the latter case due to reduced fault suppression time as a result of the increased TIV. This type of test is a very valuable test for full-pole breakers to verify correct coordination and synchronization between all series connected modules, while verifying energy absorption capability on single or double module test objects.

VIII. Conclusion

The paper presents a complete test circuit for verifying short-circuit current interruption performance of HVDC circuit breakers. The test circuit is based on ac short-circuit generators operated at low power frequency and synthetic dc voltage application, both available in high-power laboratories. The design of a test circuit and its practical implementation are presented along with detailed analysis of theoretical background. The challenges associated with the test method, such as protection of the test object and the test circuit, as well as

the application of dielectric dc voltage stress, are identified and addressed with practical high-power demonstrations in the test laboratory. The test circuit is verified by testing the current interruption performance of an 80 kV prototype of an active current injection HVDC circuit breaker. The test results for bidirectional current interruption performance of the mentioned breaker with four different test duties (current ranging from 2 kA - 16 kA) and energy absorption levels up to 4 MJ are presented. The capability of a test facility with respect to testing multi-module/full-pole HVDC circuit breakers of different technologies is presented along with demonstration of example cases.

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