SUMMARY

Future multi-terminal DC networks are envisioned for the large-scale integration of renewable energy sources into today’s power systems. To minimise the downtime of HVDC networks and thereby reduce the impact of DC contingencies on surrounding AC networks, faulted DC lines must be separated quickly and reliably from the remaining part of the network.

Even though the fast separation of faults in HVDC networks is often associated with DC circuit breakers, protection systems based on fault blocking converters and DC high-speed switches have been proposed as a reasonable alternative for the protection of DC networks in the recent past.

The focus of previous contributions regarding these protection systems has been on the separation of faulted lines. However, post-fault system restoration can have a significant influence on the power outage caused by a DC fault as well as the overall system recovery time. Particularly challenging during this restoration process is the post-fault DC voltage rebalancing in HVDC systems in monopole configuration, which still is the most frequently used configuration for MMC-based systems.

This paper therefore investigates the applicability of different schemes to rebalance the pole voltages during the DC voltage restoration process (i.e. dynamic braking and AC grounding systems) and evaluates their impact on the performance of the protection strategy. Moreover, a rebalancing method, which does not rely on specific equipment, but only on the control of the fault blocking converters is proposed. This method appears to be a feasible alternative, since the overall protection system performance is competitive to the other methods involving specific equipment, even though no extra components need to be installed in the network.

KEYWORDS

HVDC Network – Protection – Modular Multilevel Converter – Fault Blocking Converter

1. INTRODUCTION

Several initiatives, which comprise transmission grid operators, vendors and academia, envision multi-terminal DC networks as a technically and economically promising solution for the large-scale integration of renewable energy sources into the power generation portfolio. Especially for the connection of wind power plants and the interconnection of different synchronous areas, HVDC networks are considered to be built in the North and Baltic Sea in Europe. Regardless of the technological, operational and economic drivers of future multi-terminal HVDC networks, some key aspects – especially regarding the protection of these systems – are still under investigation. To limit the downtime of HVDC systems, which might transmit several gigawatts of electric power, a faulted line must be separated quickly and reliably from the remaining part of the network.
concepts have been proposed to enable a fast fault separation in HVDC networks, most relying on fast DC circuit breakers. However, separation methods based on fault blocking converters (FBC), such as full-bridge modular multilevel converters (MMC), and high-speed switches (disconnectors with residual or nominal current interruption capability) have shown to be a competitive alternative in certain DC networks [1, 2]. Due to reduced requirements on the switching devices and no need for current limiting line inductors, the mass and volume of these systems is expected to be significantly smaller compared to protection schemes based on fast HVDC breakers [1, 3]. In contrast to fault feeding converters, such as half-bridge MMCS, fault blocking converters (FBC) have the ability to interrupt the fault current contribution from the AC system to the DC system in case of DC faults without the need for AC or DC circuit breakers. The most established FBC is the full-bridge (FB) MMC which will be used for the first time in the German project Ultranet [4]. Moreover, other promising FBC configurations are currently under consideration, which have similar functionality as FB-MMCs but reduced losses during normal operation, such as mixed stack MMC configurations [5] or the Alternative Arm Converter [6]. Such FBCs can limit or interrupt the fault current contribution from the AC to the DC system and prevent a fault current contribution of the MMC capacitors, due to their high degree of controllability. In addition, they can even actively support to quickly de-energise the DC network [1]. Consequently, the grid voltage and the fault currents decay to values close to zero. The separation of the faulted lines in near-zero current and reduced voltage conditions can be achieved by so-called DC high-speed switches (HSS) with residual DC current interruption capability. Subsequently to the separation of the faulted line, the converters restore the DC grid voltage and the power flow in the healthy part of the MTDC network.

The focus of previous contributions regarding protection systems based on FBCs has been on the separation process of faulted lines [2, 7]. However, the post-fault system restoration can have a significant influence on the power outage caused by a DC fault as well as the overall system recovery time. A particular challenge during the restoration process is the post-fault DC voltage rebalancing in HVDC systems in monopole configuration, which still is the most frequently used configuration for MMC-based DC systems. The objective of this work is to assess the problem regarding voltage rebalancing in multi-terminal HVDC systems protected by FBCs, to analyse existing strategies and to propose a new rebalancing method. After an introduction to the FBC-based protection strategy and definition of functional requirements, the main contributions are as follows:

- **Problem statement**: The effect of an asymmetrical voltage restoration is presented and scenarios in which DC pole voltage rebalancing schemes are required are identified.
- **Existing schemes**: The applicability of pole voltage rebalancing schemes, which are considered for DC circuit breaker based protection systems, is evaluated.
- **Novel method**: A method is proposed which solely based on the control of the FBCs and does not require additional equipment dedicated to the pole voltage rebalancing.
- **Comprehensive evaluation**: The impact of the rebalancing methods on the overall performance of the FBC-based protection system is evaluated based on a variety of fault scenarios.

All investigations are based on a minimal meshed MTDC offshore network defined in the European Horizon 2020 project PROMOTioN.

2. **HVDC NETWORK PROTECTION BASED ON FBCs**

To evaluate and derive appropriate methods for the post-fault voltage restoration in MTDC networks protected by FBCs, a fundamental understanding regarding the protection of MTDC systems, the FBC-based protection strategy and the functional requirements is essential.

2.1. **Functional Requirements on Multi-Terminal HVDC Protection**

The key objectives of HVDC grid protection systems, which are derived from AC protection systems, are to ensure human and component safety as well as a secure operation of the overall power system [8–11]. Compared to today’s point-to-point HVDC systems, in which DC faults result in a long-term outage of the entire HVDC link, future MTDC networks might require a fast separation of faulted DC lines. Especially, if the lost transmission capacity of a DC grid towards a country or synchronous zone exceeds the network’s permitted maximum loss of infeed and causes a critical frequency deviation [12] — e.g. a
power loss of more than 3 GW to the Continental European or 1.8 GW to Great Britain’s transmission grid [13] – a long-term outage of the entire HVDC network cannot be tolerated [12, 14]. In order to enable the interoperability of existing AC grids and HVDC networks protected by FBCs it must be ensured that the protection complies with the concept of a temporary stop $P$, which implies that a temporary outage or shortage of the HVDC transmission capability does not result in any disturbance of the surrounding AC systems and their stability [10].

To assess HVDC protection strategies, quantifiable values reflecting their performance need to be defined. A DC fault clearing process in DC networks can be separated into two phases: First, the duration between fault inception and the separation of the faulted zone from the healthy HVDC network and second, the duration between fault separation and restoration of the HVDC network to normal operation conditions [10]. To evaluate the duration of these phases and to evaluate the impact of an HVDC protection system on the HVDC network and the surrounding AC transmission system the following Key Performance Indicators (KPIs) are used [1]:

- $t_{\text{sep}}$: Fault separation time – Time until all relevant fault separation devices are opened and the faulted line or zone is separated.
- $t_{\text{v,rest}}$: Voltage restoration time – Time until the DC voltage is restored within its normal operation limits at all DC nodes (here within ± 5% of the nominal DC voltage [11]).
- $t_{\text{p,rest}}$: Active power restoration time – Time until the active power is restored within a tolerance band to its post fault steady state value (here within ± 10% of the rated converter power).

It is the objective of this work to analyse different DC voltage restoration methods and investigate their impact on the fault separation and the active power restoration time.

### 2.2. Protection Strategy Based on Fault Blocking Converters

The sequence of the FBC-based protection strategy for a single busbar on a HVDC network is illustrated in Figure 1 (a). If a fault occurs in the network at the time $t_0$, the travelling waves propagate through the system and the protection relays located at each HVDC busbar detect the fault at $t_{\text{det}}$. These relays trigger the fault current reduction process of each converter, i.e. a DC fault current zero control, and the fault localisation process. If a fault is localised on a line connected to the converter’s busbar, the corresponding relay selects the HSS located at the end of the faulted line.

As soon as the opening conditions of the selected HSSs are fulfilled, these switches separate the faulted line from the remaining DC network. The opening conditions of the HSS usually comprise a current interruption threshold $I_{\text{HSS,thres}}$ and a DC grid pole-to-ground voltage threshold $V_{\text{PG,thres}}$ [1].

Before the converter can start the grid recovery process, it has to be ensured that the HSS at the other line end is successfully opened too. This can either be achieved via a DC grid communication system or a predefined automatic restart time, in which fault separation processes are expected to be accomplished. In this work, the grid recovery process is initiated by an external communication signal generated by a central DC grid relay. Therefore, the status of the HSSs after fault separation are sent to the DC grid relay, which sends the restart signal to all converters after all four HSS (two per line) are successfully opened [1].

### 2.3. DC Fault Control

In case of a DC fault, the simplest approach to interrupt the fault current contribution from the AC to the DC side is to block the converter by blocking all its power electronic switching devices. In previous contributions, it is shown that a fault current zero control and especially a control of the fault current through the relevant HSS is beneficial for the fault separation process [1, 7].

The principle of such a selective fault current control is illustrated in Figure 1 (b). ① After fault detection, all converters within the affected protection zone control their terminal current $i_t$ to zero – Terminal current zero control (TCZC). ② If a fault is identified on a line connected directly to a converter’s busbar, as illustrated in Figure 1 (b), the corresponding converter changes its fault control mode to line current control (here $i_{L2}$), in order to fasten the fault current reduction through the relevant HSS. Consequently, the current through the relevant HSS is selected as input to the line current zero control (LCZC). Subsequently, to the opening of the HSSs, the converter switches back to terminal current zero control mode. If no fault is localised directly at a busbar, the corresponding converter remains in TCZC until the restart process is initiated [1].
3. INVESTIGATED HVDC SYSTEM AND MODEL DESCRIPTIONS

The investigations of this work are carried out in an MTDC test network of the PROMOTioN project. This network is illustrated in Figure 2. All transient simulations are carried out in PSCAD|EMTDC™ with a time step of $\Delta t = 20 \mu s$. The transmission lines are modelled using a Frequency Dependent Phase Model. The cables are parametrized according to 320 kV XLPE submarine cables. Assuming that armour and sheath are regularly grounded, the concentric conductors of the cable are eliminated mathematically. In contrast to MTDC networks protected by fast DC circuit breakers, no line inductances are required for the limitation of fault currents. All four converters are modelled as full-bridge MMCs either in monopolar or in bipolar configuration with dedicated metallic return. The most relevant parameters of the converters are summarised in Table 1. Each converter is modelled using a Type 4 – Detailed Equivalent Circuit Model. Hence, the model is suitable for DC fault studies [15].

The HSS used within this work comprises a solid-state based residual current breaker (RCB) and an ultra-fast disconnector, as illustrated in Figure 3 [1]. The RCB is set up of two antiparallel series connections of three IGCTs with a rated voltage of 6.5 kV. During the current breaker process a surge arrester limits the transient interruption voltage across the RCB and absorbs the stored residual energy of the circuit. The rated voltage of the RCB’s surge arrester is set to $V_{SA,RCB} = 15$ kV (at $i_{SA,RCB} = 1$ kA). This design results in an on-state resistance of approximately $R_{HSS,on} = 1.5$ mΩ and a power loss per HSS of $P_{loss,HSS} = 5.3$ kW under full load [1].

Since all converters of the affected protection are involved in the fault separation process, the fault discrimination can be split into two main parts – fault detection and fault localisation – without affecting

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1. Within the simulations of this work, the maximum absorbed energy of a RCB surge arrester is $E_{SA} = 13$ kJ.
the security of the components. The detection is realised via a single-ended method comprising a combination of an undervoltage as well as a voltage and a current derivative protection. The security of the HVDC grid components does not depend on the fault separation. Hence, the fault discrimination can be realised as a double-ended scheme without a compromise in safety, i.e. a longitudinal DC line current differential protection. For signal processing, a time delay of $\Delta t_{\text{det}} = 0.1$ ms is added to the fault detection and localisation [1]. For a comprehensive analysis of the voltage restoration, a systematic variation of fault scenarios within the DC network is considered. Therefore, pole-to-ground (PG) faults are examined at multiple locations (at 0%, 50% and 100% of each line), which are shown in Figure 2, with different fault-to-ground resistances $R_f = [0.1 \Omega, 20 \Omega]$.

The location of the components and faults, as well as the nomenclature used within this work is illustrated in Figure 2.

Table 1: Converter settings of the full-bridge converters

<table>
<thead>
<tr>
<th>Converter Station Parameter</th>
<th>Monopole</th>
<th>Bipole</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated power</td>
<td>$S_r$</td>
<td>1265 MVA</td>
</tr>
<tr>
<td>Rated active power</td>
<td>$P_r$</td>
<td>1200 MW</td>
</tr>
<tr>
<td>Rated DC voltage</td>
<td>$V_{dc,r}$</td>
<td>640 kV</td>
</tr>
<tr>
<td>Rated AC voltage at the converter</td>
<td>$V_{ac,\text{conv}}$</td>
<td>350 kV</td>
</tr>
<tr>
<td>Arm inductance</td>
<td>$L_S$</td>
<td>42 mH</td>
</tr>
<tr>
<td>Number of submodules per arm</td>
<td>$n_{\text{sm}}$</td>
<td>350</td>
</tr>
<tr>
<td>Rated submodule voltage</td>
<td>$V_{\text{sm,r}}$</td>
<td>1.9 kV</td>
</tr>
<tr>
<td>Submodule capacitor</td>
<td>$C_{\text{sm}}$</td>
<td>8.8 mF</td>
</tr>
<tr>
<td>Output converter inductance</td>
<td>$L_{\text{DC}}$</td>
<td>10 mH</td>
</tr>
</tbody>
</table>

![Figure 3: Schematic of the solid-state based high-speed switch](image)

4. PROBLEM STATEMENT

The prospective DC grid voltage profiles (without counter measures regarding pole balancing) and the corresponding active power profiles for an exemplary PG fault in different grid configurations are illustrated in Figure 4. The fault case is a low impedance fault ($R_f = 0.1 \Omega$) in the middle of line $L_{12}$ at $t_f = 0$ ms (cf. Figure 2). In both cases, the fault currents through the HSS12 and HSS21 are controlled to zero and the HSS are able to separate the faulted line $L_{12}$, as shown in Figure 5 for HSS12. In both cases the current through the HSSs rise quickly due to the transient discharge of the positive pole to the fault. Subsequently to the fault detection and localisation the current through the HSSs are control to zero and the HSS are able to separate the faulted line in near-zero voltage and current conditions. Afterwards, the DC voltage is restored.

A PG fault in a bipole network does not cause significant changes in the voltage of the unaffected pole (here the N pole), due to the networks low-impedance DC side grounding. In case of a DC network in symmetrical monopole configuration, the same fault causes an asymmetrical overvoltage on the unaffected pole, since the DC side is not effectively grounded. Consequently, the

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2 Due to the symmetrical design, only PG faults of the positive pole are considered.

3 These values are used for the performance analysis of the fault clearing strategy and do not intend to reflect realistic fault resistances.
pole voltage imbalance and the corresponding overvoltage on the unaffected pole must be suppressed by appropriate counter measures in order to protect the grid’s components and to resume normal operation conditions.

Since DC faults with the involvement of both DC poles result in a symmetrical discharge of both poles, the P and the N poles charge symmetrically during the voltage restoration process. Hence, there is no need for an advanced voltage restoration method or any additional measures.

<table>
<thead>
<tr>
<th>Symmetric Monopole</th>
<th>Bipole (with DMR)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Graph" /></td>
<td><img src="image2" alt="Graph" /></td>
</tr>
</tbody>
</table>

Figure 4: Prospective DC grid voltage and active power transmission profiles for an exemplary pole-to-ground fault in a symmetric monopole and a bipole MTDC network

<table>
<thead>
<tr>
<th>Symmetric Monopole</th>
<th>Bipole (with DMR)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image3" alt="Graph" /></td>
<td><img src="image4" alt="Graph" /></td>
</tr>
</tbody>
</table>

Figure 5: Current though HSS12 for an exemplary pole-to-ground fault in a symmetric monopole and a bipole MTDC network

5. DC VOLTAGE REBALANCING

The classic applications for pole voltage rebalancing schemes are HVDC systems based on half-bridge MMCs in symmetrical monopole configuration, which are protected by DC circuit breakers. Within these systems, PG faults result in a persistent overvoltage on the unaffected pole. Consequently, pole rebalancing is a necessary step to protect the components against temporary overvoltages and to restore the system to normal operation. There are two main counter measures to these overvoltages: dynamic braking systems (DBS) or AC side grounding schemes permitting zero sequence currents [16]. The applicability of these schemes in the FBC-based protection systems needs to be analysed. Moreover, it
is possible to balance the pole voltages by discharging the healthy pole prior to the voltage restoration [17]. Since the existing method for this balancing operation has the drawback of an interruption on the reactive power controllability of the MMCs, a new method is proposed within this work.

5.1. Dynamic Braking Systems

As DBS, a conventional circuit with lumped braking resistors is analysed within this work as it is used for today’s offshore wind applications [18]. These DBS systems are usually installed at the onshore converter of HVDC links connecting offshore wind power plants to enable a fault-ride-through (FRT) of the HVDC system and the wind turbines during faults in the onshore AC transmission grid [18]. The schematics and the ratings of the DBS used within this work are shown in Figure 6 and Table 2 [16]. Within the test system, the DBSs are located at Bus 1 and Bus 2, which are representing the onshore stations.

Table 2: Parameters of the dynamic braking system [16]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Braking resistor</td>
<td>(R_{\text{DBS}})</td>
<td>171 (\Omega)</td>
</tr>
<tr>
<td>Maximum reference current</td>
<td>(I_{\text{DBS,,max}})</td>
<td>2 kA</td>
</tr>
<tr>
<td>Proportional control gain</td>
<td>(K_{P,\text{DBS}})</td>
<td>0.5</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>Hi/Lo</td>
<td>1.1/1.05 p.u.</td>
</tr>
<tr>
<td>PWM frequency</td>
<td>(f_{\text{PWM,,DBS}})</td>
<td>2 kHz</td>
</tr>
</tbody>
</table>

Figure 6 shows the DC grid voltage and the AC active power profiles for the same exemplary fault scenario as presented in section 4 (PG fault in the middle of line \(L_{12}\)). The DBS system is able to restore and balance the pole voltages within \(t_{\text{VR,\,rst}} = 70.9\) ms in this case. The active power transmission resumes within the \(\pm10\%\) tolerance band in \(t_{\text{PR,\,rst}} = 100.5\) ms. During this operation the braking resistors dissipate \(E_{\text{DBS,C1}} = 6\) MJ and \(E_{\text{DBS,C2}} = 5.2\) MJ, which is significantly smaller than the energy dissipated during an onshore AC FRT (order of a few 100 MJ) [16].

The voltages across the affected DBS switches \(T_{\text{DBS,n}}\) for the DBS\(_{C1}\) and DBS\(_{C2}\) are shown in Figure 7 (left). The maximum voltage in this case is \(v_{\text{T,\,DBS}} = 473\) kV. This voltage, however, strongly depends on the voltage imbalance between the DC poles prior to restoration and could therefore increase to twice the nominal DC pole voltage. Consequently, the insulation level of the DBS IGBT stacks need to be dimensioned for these voltages or the IGBTs need to be protected by surge arrestors. Alternatively, a more complex DBS design, e.g. based on surge arresters, could be applied [16].

Figure 7: Voltage (left) and power (right) profiles with DBSs for DC pole rebalancing

5.2. AC Side Grounding and Zero-Sequence Control

An alternative to braking systems on the DC side are grounding systems on the AC side of the converter. There are different solutions such as star point reactors, Yyd (grounded on the converter side) and zig-zag transformers. Due to their relatively small apparent power consumption during steady state operation, zig-zag grounding transformers are applied within this work to enable zero-sequence currents,
as shown in Figure 8. In order to enhance the performance of the rebalancing system and the stability of the converter control, the AC grounding is combined with a zero-sequence control of the AC converter currents [16]. The schematics and ratings of the zig-zag transformer are shown in Figure 8 and Table 3 [16]. Similar to the DBS of section 5.1, the zig-zag transformers are located at the onshore converters C1 and C2.

Table 3: Parameters of the zig-zag grounding transformer [16]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated power</td>
<td>$S_n$</td>
</tr>
<tr>
<td>Leakage impedance</td>
<td>$L_Z$</td>
</tr>
<tr>
<td>Neutral resistor</td>
<td>$R_Z$</td>
</tr>
</tbody>
</table>

The DC grid voltage and the AC active power profiles for the exemplary fault (PG fault in the middle of line $L_{12}$) are shown in Figure 9. Due to the zero-sequence current path, the imbalance between the pole voltages decay and both pole voltages resume within the ±5% tolerance band in $t_{V_{rst}} = 64.4$ ms. Active power transmission resumes at all stations within the ±10% tolerance band in $t_{P_{rst}} < 111.3$ ms.

5.3. Converter Controlled Rebalancing

Since the overvoltage on the healthy DC pole is caused by a pole voltage unbalance prior to the DC voltage restoration, it can be avoided by removing this unbalance before the restoration is initiated. Since the only low-impedance grounding in the DC system is the fault itself, the healthy pole is discharged via the fault location, as shown in Figure 10.

Figure 8: Zig-zag grounding transformer [16]

Figure 9: Voltage (left) and power (right) profiles with zig-zag transformer for DC pole rebalancing

Figure 10: Schematic diagram of the discharge process of the healthy pole via the converter and the fault location
One method to suppress the pole voltage and therefore discharge the healthy pole through the fault location is to temporarily bypass all submodules of an FBC. Thereby, both DC poles are short-circuited via the converter arm reactors. To limit the converter currents, this suppression operation is switched on and off similar to a DBS [17]. The advantage of this method is that no additional equipment is required for the pole voltage balancing. A major drawback, however, is the interruption in controllability and therefore the reactive power support to the AC system of every converter operating in pole voltage unbalance suppression mode. Moreover, this method might cause transients in the DC grid.

In order to avoid these downsides, a controlled unbalance suppression method is proposed within this work. Therefore the DC terminal pole-to-pole voltage \( V_{TP} \) is controlled to zero – terminal voltage zero control (TVZC) [7]. As illustrated in Figure 11 (right) not only the DC current but also the DC pole-to-pole voltage is controlled to zero before the fault is separated from the healthy part of the protection zone. Consequently, the healthy pole is discharge via the fault location and both poles are already balanced prior to fault separation. Therefore, no further DC voltage balancing actions are required during

Figure 11: Protection sequence with DC side pole rebalancing (left) and corresponding voltage and active power profiles for the exemplary fault case (right)

the DC voltage restoration process. Figure 11 (left) presents the DC grid voltage and the AC active power profiles for the exemplary fault scenario.

In this case, the DC voltage is restored to the ± 5 % tolerance band within \( t_{Vrst} = 81.4 \) ms. Even though this time is significantly larger than in the cases with the DBS and zig-zag transformer, the power restoration is accomplished in \( t_{Prst} = 113.4 \) ms, which is similar to the other cases.

5.4. KPI Comparison

For the comprehensive evaluation of the rebalancing methods, the KPIs are calculated based on all fault scenarios illustrated in Figure 2. Each value presented in Table 4 is the maximum value of all 24 fault cases. Since no energy stored in the healthy pole is dissipated during the restoration process, the active power restoration time of the monopole system without any rebalancing scheme is shorter than the systems with rebalancing schemes.

All three restoration methods are capable of rebalancing and restoring the pole voltages in under \( t_{Vrst} < 100 \) ms in all fault cases. While both the DBS and the zig-zag grounding transformer restore the DC voltage without a significant increase in the active power restoration time compared to the case without a balancing scheme, the controlled rebalancing method increases the maximum active power restoration time of the converters C2-C4 operating in power control mode by approx. 30 ms. However, no additional equipment for the pole voltage rebalancing is required.
Due to the effective DC grounding of the bipole network configuration, all KPIs are smaller in this case than in the monopole cases and no rebalancing method is required.

Table 4: Comparison of the voltage rebalancing methods

<table>
<thead>
<tr>
<th></th>
<th>Monopole no bal.</th>
<th>Monopole DBS</th>
<th>Monopole Zig-zag</th>
<th>Monopole TVZC</th>
<th>Bipole</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault separation</td>
<td>23 ms</td>
<td>23 ms</td>
<td>23 ms</td>
<td>46 ms</td>
<td>19 ms</td>
</tr>
<tr>
<td>DC grid voltage recovery</td>
<td>&gt; 1 s</td>
<td>93 ms</td>
<td>72 ms</td>
<td>87 ms</td>
<td>71 ms</td>
</tr>
<tr>
<td>Active power recovery C1</td>
<td>101 ms</td>
<td>106 ms</td>
<td>115 ms</td>
<td>117 ms</td>
<td>82 ms</td>
</tr>
<tr>
<td>Active power recovery C2-C4</td>
<td>83 ms</td>
<td>88 ms</td>
<td>101 ms</td>
<td>112 ms</td>
<td>63 ms</td>
</tr>
</tbody>
</table>

6. CONCLUSION

The rebalancing of the DC pole voltage after or during the fault handling process is an important aspect of the overall FBC-based protection strategy, if it is applied to an HVDC network in monopole configuration. If a DBS system is included in the HVDC network to ensure a FRT of the system during faults in the AC transmission systems, this might be used for rebalancing purposes as well. Since the voltage stresses imposed on the DBS switches might be larger during the rebalancing method than in the FRT operation, the DBS must be protected against such overvoltages.

It is presented that pole rebalancing can also be accomplished using AC grounding schemes providing a sufficient zero-sequence current path, such as zig-zag grounding transformers.

Within this work, an alternative rebalancing method is proposed, which is solely on the control of the FBCs. A benefit of this approach is that no additional equipment is required for the rebalancing of the pole voltages.

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BIBLIOGRAPHY


