Design of a DC Fault Current Reduction Control for Half-Bridge Modular Multi-Level Converters

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Keywords

≪HVDC≫, ≪MMC≫, ≪Converter control≫, ≪DCCB≫.

Abstract

HVDC DC grids composed of half-bridge modular multi-level converters (HB MMC) can be protected against DC faults using DC circuit breakers (DCCBs). However, the rapid increase of DC fault currents during DC pole-to-pole faults on symmetric monopolar HVDC systems or DC pole-to-ground faults on bipolar HVDC systems poses a challenge on the design of DCCBs due to the requirement on handling very large amount of energy during the DC fault clearing process.

Blocking of the MMC converters immediately after the DC fault stops the fault current contribution of the HB MMC submodules, and reduces the design requirement of the DCCBs (energy absorption and interruption capability), but at the cost of disrupting continuous operation of the Hybrid AC/DC grid and potentially deteriorating stable post fault system recovery.

This paper introduces a method that helps to reduce the DC fault current contribution of the HB MMC submodule capacitors using the converter controls of the MMCs within the HVDC grid in order to reduce the requirements of DCCB designs. The proposed method achieves this during a DC pole-to-pole fault on a symmetric monopolar HVDC system or a DC pole-to-ground fault on bipolar HVDC system through the use of modified circulating current controls of the MMC HVDC. The parameters of the proposed controller are selected taking into consideration the operational limits of the converters.

Introduction

Modular Multilevel Converter (MMC) based HVDC grids are gaining more attention as promising options for integrating large-scale offshore wind farm and interconnection of various asynchronous AC systems in a flexible, economic and reliable way [1].

In large-impact HVDC grids where a total interruption of the power transfer has severe consequences on the stability of the associated AC networks [2], the use of DC circuit breakers (DCCBs) enables selective

isolation of faulty DC lines or cables in the presence of DC faults, while maintaining power transfer on the healthy parts of the HVDC grid.

However, depending on the size of the line inductors present in the DC lines, the location of the fault and the opening times of the hybrid or mechanical type DC circuit breakers, the DC fault current might propagate to the healthy parts of the HVDC grid. The opening times of the hybrid or mechanical type DC circuit breakers [3] fall typically within a time range of $2-10$ *ms* [4–8].

If the fault propagates to the healthy parts of the HVDC grid, it might force the MMC HVDC converters to block, and this can disrupt continuous operation of the healthy parts of the HVDC grid.

Ways to slow down the penetration of the DC fault into the healthy parts of the HVDC grid such as introduction of additional passive components and use of active fault current control scheme are presented in literature [9]. The passive component method presented in [9] uses DC-link capacitors or additional line inductors.

The goal of this paper is to introduce a converter control method that helps to reduce DC fault currents, and the requirements of DCCBs, via modification of the standard circulating current control schemes presented in literature such as the proportional resonant controller type [10] or the rotating frame (DQ) type circulating current controllers [11].

The parameters of the proposed control scheme are selected considering the operational limits of the converters such as modulation index limits, and converter arm over-current limits.

The effectiveness of the proposed method is also analyzed on a three terminal meshed DC grid built in PSCAD for this purpose.

Description of the proposed control structure

Different types of standard active and passive circulating current reduction methods for MMC are documented in literature. Among the active methods are the Proportional-Resonant controllers and the rotating frame DQ-type circulating current controllers [10]- [11].

The control scheme proposed in this paper for reduction the DC fault current is based on modification of the reference voltage input into the circulating current controller, named u_c^*, during the DC fault.

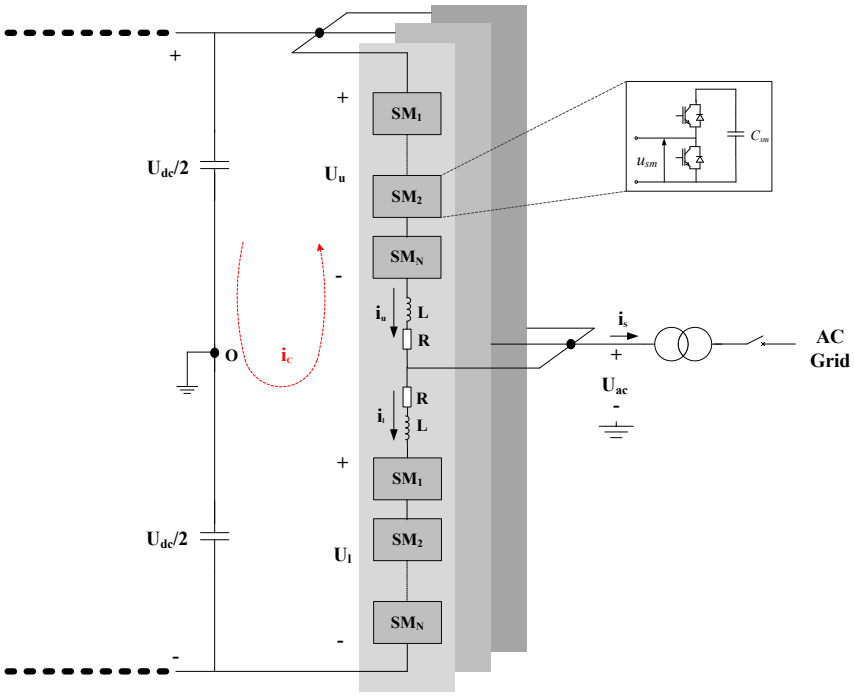


Fig. 1: Equivalent Circuit of the Half Bridge MMC

Using Fig. 1, the output voltage u_s, and the internal voltage that drives the circulating current, u_c, can be defined as follows :

$$u_s = \frac{(u_l - u_u)}{2} \tag{1}$$

$$u_c = \frac{(u_l + u_u)}{2} \tag{2}$$

The circulating current i_c is composed of the DC current as well as second harmonic component. It is calculated from the arm currents as

$$i_c = \frac{i_u + i_l}{2} \tag{3}$$

Applying Kirchhoff's Voltage Law (KVL) to the arm circuits shown in Fig. 1, we can write,

$$\frac{u_{dc}}{2} = Ri_u + L\frac{di_u}{dt} + u_u + u_{AC} \tag{4}$$

$$\frac{u_{dc}}{2} = Ri_l + L\frac{di_l}{dt} + u_l - u_{AC} \tag{5}$$

Adding (4) and (5), substituting for u_c and i_c and rearranging we get (6).

$$u_c = \frac{u_{dc}}{2} - Ri_c - L\frac{di_c}{dt} \tag{6}$$

Assuming the circulating current control, which is designed to remove the second harmonic current, works properly also during a DC fault, the only circulating current component that remains will be related to the DC fault current. Hence, modifying the internal voltage u_c can help to suppress the fault current contribution from the MMC submodule capacitors, without the need to block them, provided that the arm currents and modulation index limits of the converter are not exceeded.

Re-arranging and solving for the circulating current i_c in Laplace domain from (6) we get (7)

$$i_c = \frac{1}{sL + R}\left(\frac{u_{dc}}{2} - u_c\right) \tag{7}$$

The relationship between the circulating current and the voltage difference that drives the circulating current can be represented by a first order system transfer function given in (7). Since the plant can be approximated as a first order system, a simple controller like a proportional controller can be enough to adjust the closed-loop response of the system [12].

Modifying the upper arm voltages and lower arm voltages by Δu, which is proportional to the change in DC voltage or DC fault current, we can modify (2) to get a new reference voltage, u_c^* that drives the circulating current given by (8).

$$u_c^* = \frac{(u_u - \Delta u) + (u_l - \Delta u)}{2} \tag{8}$$

It should be noted though that the output voltage, u_s will not be influenced by this change provided that the converter is operating under its normal operational limits. This is because both the upper and lower arm voltages are reduced by the same amount in (1).

The proposed controller hereunder named as the DC fault current reduction controller, is designed to discriminate DC current present during normal power transfer from the DC fault current, as the DC current is also part of the circulating current which is normally not controlled by the circulating current controllers.

This is achieved by activating the DC fault current reduction controller only when a pole-to-pole DC

fault is detected by the DC protection relay using the relevant DC fault detection algorithms suitable for a given fully selective DC protection strategy [13]-[14].

The structure of the proposed control modification for a DQ-type circulating controller is presented in Fig. 2. The circulating current calculated as the average of the sum of the arm currents in each phase is fed into a second order notch filter which filters out the second harmonic components that might be present in the DC current, leaving out mainly transient DC current components. The difference of the nominal arm DC current in each phase and the transient DC fault current is then filtered out through a low pass filter, whose cut off frequency is selected to be high enough not to limit the bandwidth of the DC fault reduction controller which needs to act very fast at the onset of a DC fault. The low pass filter makes the derivative part less sensitive to unwanted high frequency noises as well.

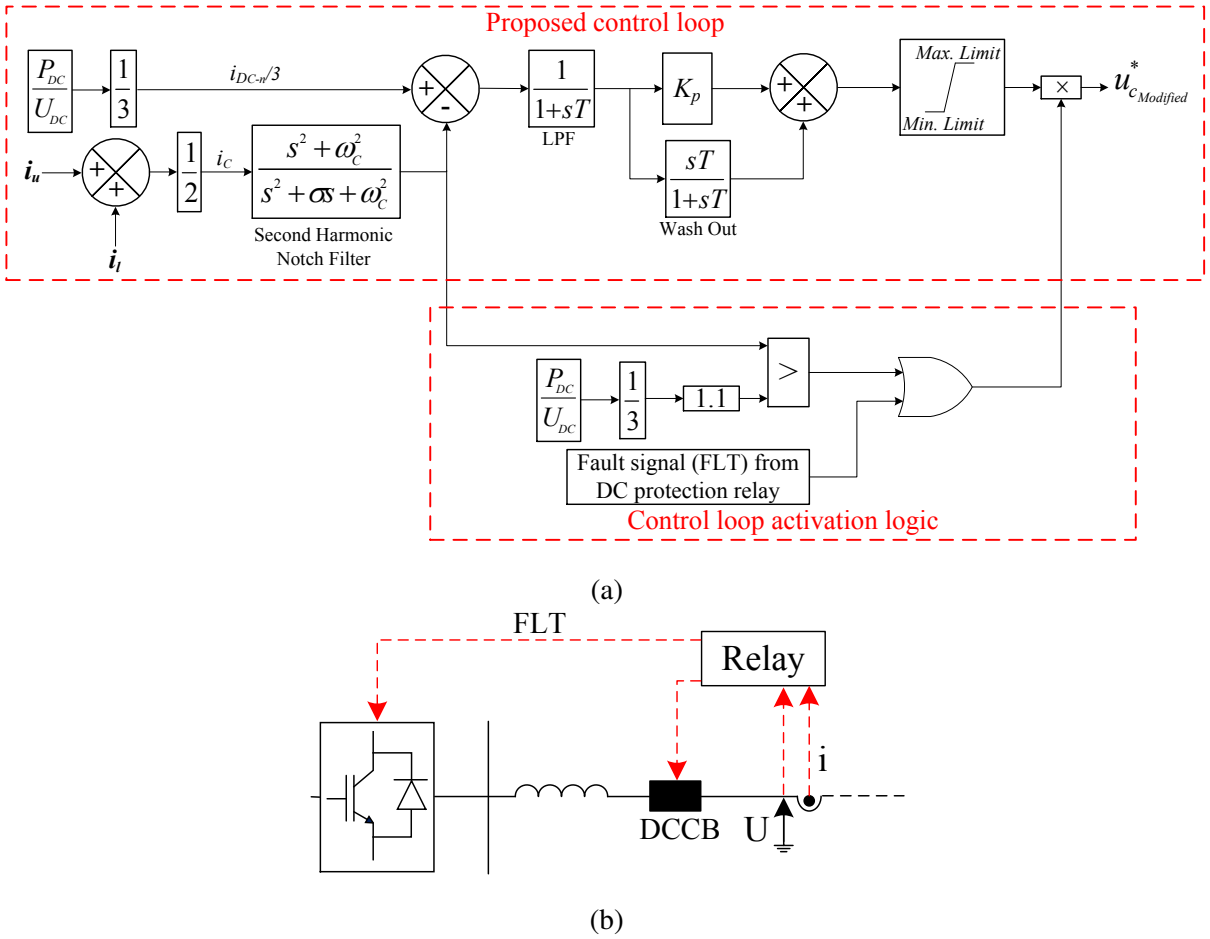


Fig. 2: (a) The structure of the proposed DC fault current reduction controller, (b) communicated signals between DC protection relay and converter station.

The arm current error, which is mainly composed of a transient DC current, is fed into a washout filter to get fast controller action immediately after the DC fault is detected. The derivative term will have no contribution during steady-state.

A proportional part with a small gain K_P is also used in parallel with the washout filter to achieve effective control action over a range of few milliseconds (Fig. 2).

The output of the DC fault current reduction controller is added to the output of the standard circulating current controller.

Activation of the DC fault current reduction controller

The DC fault reduction controller is activated only when a DC fault is detected or the fault current is above the nominal DC current. This is achieved by the fault detection signal received from the relevant

protection relay or when the DC current exceeds the threshold value set as indicated in Fig. 2.

Selection of the parameters of the proposed controller

The control parameters and limits of the proposed controller are selected considering the operational limitations of the MMCs, in order to facilitate an effective reduction of the DC fault currents while maintaining system stability.

The closed loop bandwidth of the DC fault current reduction controller is selected to be close to the bandwidth of the output current controller, as these two controllers operate in parallel and in order to guarantee stability [15].

The selection of the control parameters is performed considering operational constraints such as: (i) the converter arm over-current current limits, and (ii) modulation index limits of the converter. The modulation index m is defined as the ratio of the converter AC voltage to the DC voltage as described in (9).

$$m = \frac{\pi}{4}\frac{u_s}{u_d} \tag{9}$$

Depending on the type of carrier based PWM used, the maximum modulation index M_{max} can vary from $M_{max} = \frac{2}{\sqrt{3}}$ with third harmonic injection [16] to $M_{max} = 1.0$ without third harmonic injection. The converter should be operated with a modulation index which falls below the maximum modulation index under normal operations. If the DC voltage reduces too much during transients, it can cause temporary over-modulation. Prolonged over-modulation may lead to loss of controlability of the converters and needs to be avoided.

Upon the occurrence of a pole-to-pole DC fault on a symmetric monopole HVDC system, the DC voltage collapses at the fault location and reaches the DC terminal of the MMCs following the travelling wave behaviour. The decrease in the DC voltage causes an over-modulation, if the AC voltage remains unchanged. However, the large increment in the arm currents during the DC fault causes a large reactive power drop in the converter transformer and the arm inductances, and this in turn leads to a reduction in the AC voltage as well.

Depending on how the DC and AC voltages change relative to each other, the converter might take some time before it reaches over-modulation, hence giving time for the control actions during the start of the DC fault.

Furthermore, a scheme following the structure shown in Fig. 3 is also introduced to reduce the reactive current order of the MMC during the DC fault in order to give more margin to the active current order which can act on the DC current. This is analogous to the concept of AC voltage ride through for AC faults, which aims at reducing the active current order to increase the reactive current margin. But this scheme is relevant if the converter was operating at a non zero reactive power order before the DC fault.

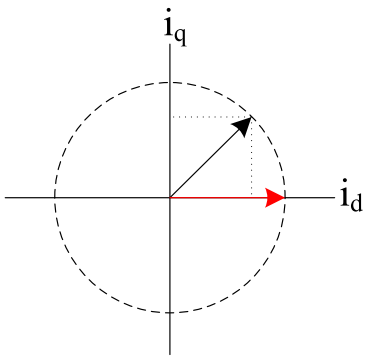


Fig. 3: Active current order margin extension of the MMC under DC fault.

In Fig. 3, the reactive q-component current order is set to zero during the DC fault to extend the active

current order limit of the d-component, shown by the red arrow, to be equal to the maximum arm current limit of the MMC indicated by the dashed circle.

Validation of the proposed controller and simulation results

The validation of the DC fault current reduction controller is performed on a symmetrical monopole HVDC grid test system shown in Fig. 4. During steady-state, MMC1 and MMC2 inject 500 *MW* to the HVDC grid excluding the converter station and DC line losses, while MMC3 injects 1000 *MW* to the AC system it is connected to.

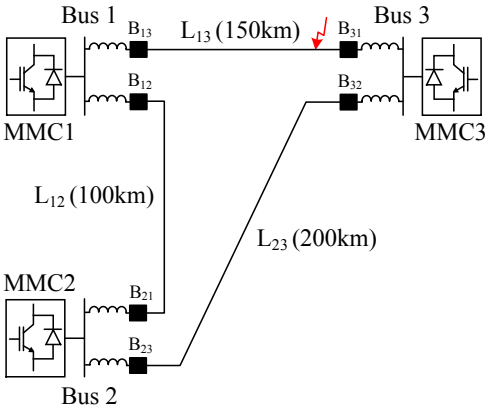


Fig. 4: HVDC grid test system.

The MMC model is based on the CIGRE B4-57 working group developed models downloaded from the PSCAD support website [17], whose arm representation is also described in [18]. The parameters of the converters are listed in Table I.

The control system of each MMC consists of an inner current controller, a DQ-type standard circulating current controller and outer control loops. Converter MMC3 is equipped with DC voltage droop controller, which controls the DC voltage, and a reactive power controller. The outer controllers for MMC1 and MMC2 control the AC side active and reactive power exchanges.

The lines in the HVDC grid are 320 *kV* XLPE cables. Each cable is formed from 3 conducting layers; a conducting core, a lead sheath and a steel armor. The PSCAD frequency dependent phase domain model is used to model the cables.

The HVDC grid is protected selectively using hybrid DC circuit breakers with 2 *ms* opening time. A DC line inductor (100 *mH*) is connected in series with the DC circuit breaker to limit the rate of rise of the fault current.

The proposed control structure is implemented, and is activated only during DC fault conditions. A solid pole-to-pole DC fault is applied on cable L_{13} at a distance of 150 *km* from Bus 1. The fault is detected within 100 μs after the traveling wave arrives at the terminal [14], which is cleared by opening DCCBs $'B_{13}'$ and $'B_{31}'$ at both ends of cable L_{13} before the internal protection system of the converter is triggered.

Three cases are compared to identify the influence of the proposed controller on the DCCB requirements and on the submodule voltages:

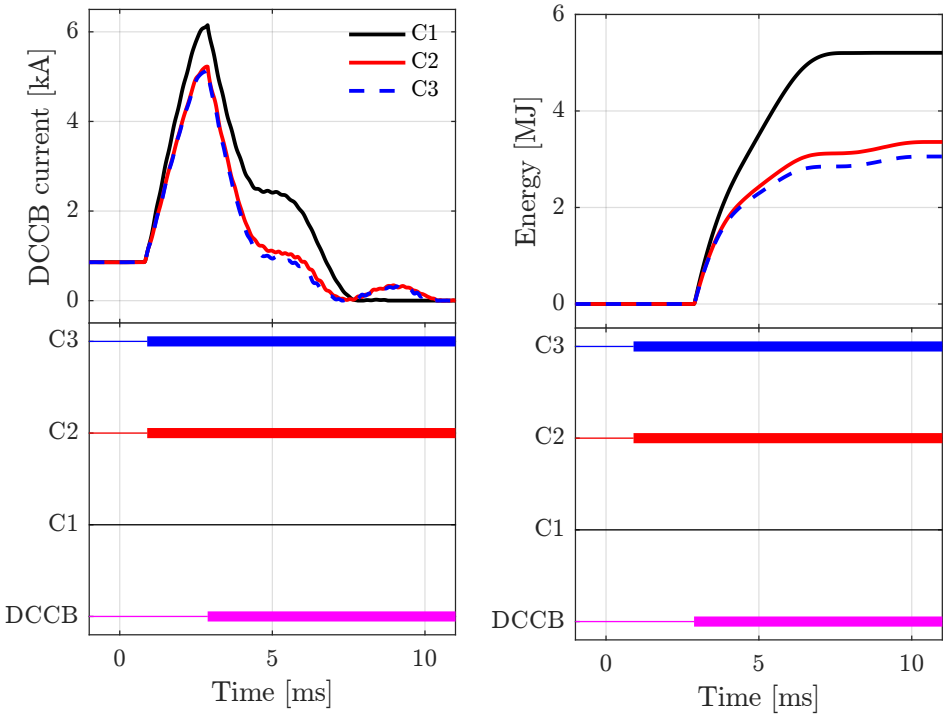
- C1: The proposed control loop is not activated during DC fault conditions.
- C2: The proposed control loop is activated during DC fault conditions.
- C3: The proposed control loop is activated and the reference point of the q-component in the inner current control loop is set to zero during DC fault conditions.

Table I: Parameters of HVDC grid test system shown in Fig. 4.

Parameters & settings	MMC1	MMC2	MMC3
DC voltage [kV]	±320	±320	±320
Converter capacity [MVA]	1000	1000	1000
Number of submodules per arm	80	80	80
AC system short circuit power [MVA]	5000	5000	5000
Transformer primary voltage [kV]	400	400	400
Transformer secondary voltage [kV]	320	320	320
Transformer leakage reactance [pu]	15%	15%	15%
Transformer series resistance [pu]	0.6%	0.6%	0.6%
MMC arm reactance [mH]	80	80	80
Control mode	P-Q mode	P-Q mode	$U_{dc} - droop$
Converter protection settings		$i_{th} = 1.75 i_{arm}$ [1]	

[1] i_{th}: Over-current threshold, i_{arm}: Maximum peak of arm current.

The proposed control loop decreases the interrupted current and absorbed energy in the DCCB. In Fig. 5, the comparison of the current and absorbed energy in B_{13} for the three cases (C1, C2 and C3) is presented. The signals in the lower sub-figures of Fig. 5 illustrate the control loop activation and DCCB tripping signals. In the simulated cases, it is observed that activating the control loop when the fault is detected leads to 15% reduction in the DCCB current and about 35%-41% reduction in the absorbed energy. Furthermore, cases C2 and C3 have almost the same fault current, however, case C3 has slightly lower energy absorption.



(a) DC current in the positive pole DCCB B_{13}

(b) Absorbed energy in DCCB B_{13}.

Fig. 5: Simulation results of the DC fault current and energy absorption in DCCB B_{13} of Fig. 4 .

The summation of the arm submodule voltages on the upper arms of each phase of MMC1 are presented in Fig. 6. It can be observed that the summation of the arm voltages shown in cases C2 and C3 are much higher during the pole-to-pole DC fault compared with C1. This validates that the reduction con-

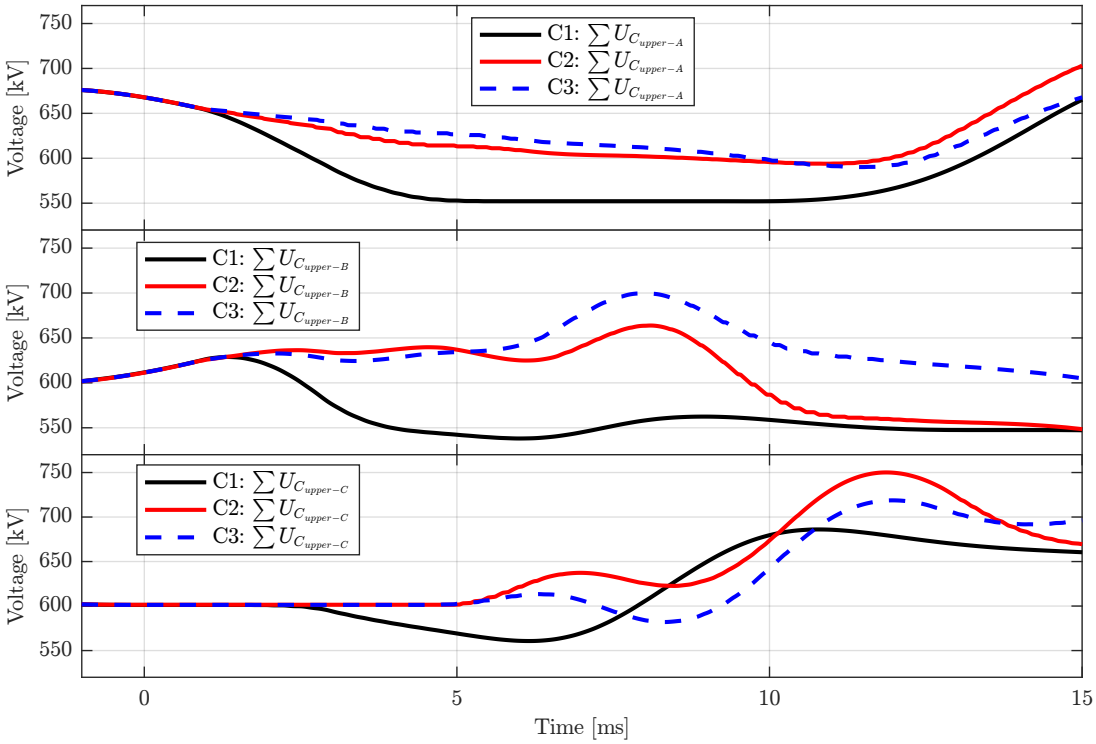


Fig. 6: The summation of submodules voltages of the upper arms of MMC1.

troller bypasses a significant number of the submodules when it is activated, preventing the submodule capacitors from discharging during the DC fault conditions, and hence reducing the DC fault current and absorbed energy in the DCCB.

The transients associated with the DCCB opening can lead to a slightly altered behaviour of the sum of the arm voltages as shown in phases B and C in Fig. 6.

Conclusion

This paper has introduced a control scheme that reduces a DC fault current in an MMC based HVDC grid guaranteeing continuous operating of the healthy converters during DC fault conditions. The parameters of the proposed control scheme were chosen considering the operational limits of the MMC converters.

The performance of the proposed controller was validated in a three terminal meshed DC grid. The DC fault reduction controller was observed to help reduce the initial rate of rise of the DC fault current by up to 15% of the peak value compared with the fault current case without the proposed controller activation. This translates into a reduction of the DC circuit breaker energy dissipation requirements as well.

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