Modelling of Hybrid DC Circuit Breaker Based on Phase-Control Thyristors

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***Abstract*—This paper presents model of hybrid direct current (DC) circuit breaker (CB) based on phase-control thyristors. The design aspects are shown and the CB parameters are calculated for a 120kV and 1.5kA DC CB assuming 10kA interrupting current. An internal control system for opening and closing is presented. The DC CB is modelled at system level in PSCAD. Simulations are used to evaluate the DC CB performance under different operating conditions such as opening and closing. The model represents well DC CB including main internal subsystems and can be employed for DC grid protection studies. It is also concluded that the thyristor-based hybrid DC CB potentially benefits in higher fault current interruption compared IGBT-based hybrid DC CB. However on the downside, simulations indicate that extinction time of phase-control thyristors results in DC CB longer opening time.**

***Index Terms*—DC grids, Protection, Hybrid DC circuit breaker.**

I. INTRODUCTION

High voltage DC Circuit Breakers have recently been developed and prototype tested at voltages around 100kV [1]-[5]. There are three main groups of DC CB; mechanical DC CBs [2], [3], IGBT-based hybrid DC CBs [4], and thyristor based hybrid DC CB [5],[6].

The mechanical DC CBs provide very small contact resistance (a few μΩs) but with relatively long fault current interruption time (around 10 ms) [2], [3]. The mechanical DC CB has been modeled in [7], and simulation results have shown good model accuracy.

The IGBT-based DC CB provides fast fault interruption time (2-3 ms) with current limiting capability [4]. The IGBT hybrid DC CB model is reported in [8], and the model has proven to be adequate for DC grid development studies in [9].

The fault interruption time with thyristor-based DC CB can vary in wider range (2.5-12 ms) depending on the DC CB design and fault current level. The thyristor-based DC CB can potentially withstand much higher fault current compared to the IGBT-based DC CB because of smaller ON resistance and higher non-repetitive surge current rating of the thyristors.

The model for hybrid thyristor-based DC CB has not been reported yet.

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Thyristor-based DC CB has similar normal current branch as in IGBT-based DC CB, but the main breaker branch uses thyristors with substantially different and more complex operating principle [5],[6]. In particular, the circuit design should ensure thyristors completely turn off by providing adequate reverse recovery duration. Also the capacitors should be discharged in anticipation of the closing/opening cycle.

This paper aims developing suitable model for hybrid DC CB employing phase-control thyristors. The model is primarily aimed at DC grid protection studies.

II. DESCRIPTION OF THYRISTOR-BASED HYBRID DC CB

Fig. 1 shows the structure of thyristor-based DC CB [5]. It consists of normal current branch, main breaker branch and energy absorption branch. The normal current branch conducts the current in normal operation and consists of a load commutation switch (LCS) T_1 with a parallel surge arrester SA_{T1} and an ultra-fast disconnector (UFD) S_1.

The main breaker branch is composed of the first and second time delaying and arming sub-branches. The first time-delaying branch includes thyristor valves T_{r1} and T_{r11}, surge arrester SA_{11}, capacitor C_{11} and discharging resistor R_{11}. It conducts the fault current from the time the LCS T_1 is opened until the contacts of UFD S_1 have separated (but not necessarily reached their full dielectric withstand capability). The main function of this sub-branch is to keep the voltage across UFD S_1 low enough while it is opening. and to start building up the transient interruption voltage (TIV).

The second time-delaying branch ($T_{r12,}$ SA_{12}, C_{12} and R_{12}) conducts the fault current for the period the contacts of the switch S_1 are opening until they reach their full dielectric withstand capability. This branch builds up partially the transient interruption voltage (TIV).

The arming sub-branch ($T_{r2,}$ SA, C_2 and R_2) starts to conduct the fault current when the switch S_1 is fully opened. The current will then be transferred to the main surge arrester SA in the energy absorption branch and will finally be extinguished because of the counter voltage of SA.

III. Design Principles

The test system has the rated voltage of 120kV and rated current of 1.5kA. The peak interrupting current is 10kA.

A. Normal Current Branch

The current rating of the LCS T_1 should be higher than 1.5kA. The voltage rating for valve T_1 should be higher than the conduction voltage of first time-delaying sub-branch when S_1 is still closed. One suitable IGBT module for valve T_1 could be the ABB StackPak 5SNA 2000K450300 (4500V and 2000A). Usually a matrix configuration of 3x3 IGBTs is used in T_1 to reduce the power loss and to increase both current and voltage ratings. Therefore, the ratings of T_1 would be 6 kA and 13.5 kV. Each IGBT module has internal driver-level protection which indiscriminately trips IGBT if current is close to destruction level.

The surge arrester SA_{T1} is required to keep the voltage across T_1 well below its rated value. Therefore, the clamping voltage of SA_{T1} should be less than the voltage rating of LCS T_1 and it is selected asV_{SAT1_clamp}=12 kV.

The UFD S_1 is selected with residual chopping current I_{res}=10 A and mechanical time delay T_{mec}=2ms.

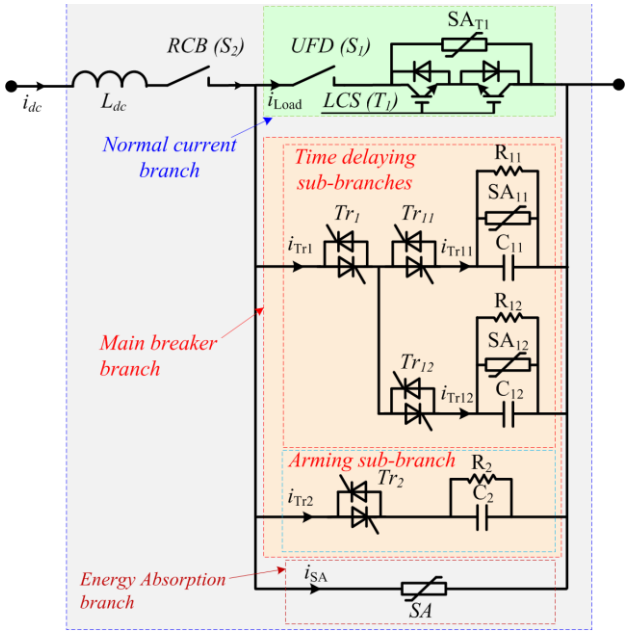

Fig. 1. Structure of thyristor-based hybrid DC CB

B. First Time-Delaying Branch

Thyristor module ABB 5STP 48Y7200 (7200V and 4800A) is adopted for this DC CB. This switch has over 50kA non-repetitive peak current capability on 10ms half-sine cycle. Since thyristor conduction time is quite short (around 5ms) this surge capability is relevant for the design and indicates potential DC CB design with much higher interrupting current capability. In this design 10kA peak current is assumed and this determines capacitor sizing.

The thyristor valves Tr_1 and Tr_{11} should withstand 1.5 time of the maximum TIV which is 1.5*120 kV. Therefore, each of the valves Tr_1 and Tr_{11} should be composed of 19 series thyristors.

A minimum value of the capacitance C_{11} can be determined based on the voltage dielectric breakdown strength of switch S_1. If UFD S_1 opens fully in 2 ms and withstands 50% overvoltage of the DC nominal voltage, the voltage slope across the contacts of S_1 is 90,000 kV/s and therefore the dv_{C11}/dt should be lower than 90V/μs.

Considering the parallel circuit C_{11}, R_{11} and SA_{11}, the maximum dv_{C11}/dt happens when v_{C11}=0; i.e. current through R_{11} and SA_{11} is zero. Assuming the trip happens at fault current i_{Tr11}=5 kA,

$$\frac{dv_{C11}}{dt}=\frac{i_{Tr11}}{C_{11}}=\frac{4kA}{C_{11}}<90,000kV/s\Rightarrow C_{11}>55\mu F \qquad (1)$$

The above current magnitude is justified considering that at the end of interruption the current will reach rated 10kA. It is recommended to design the DC CB in a way that the conduction time of the first time-delaying sub-branches is around $T_{mec}/2$. Considering that the conduction time is composed of charging time of C_{11} and conduction time of SA_{11}, capacitance C_{11} is usually selected larger to have longer charging time for C_{11}. This shortens conduction time of SA_{11} and reduces dissipated energy in the surge arrester.

Assuming that the charging time of capacitor C_{11} should be no longer than 1 ms for any fault current, a maximum capacitance of C_{11}=450 μF is obtained for a minimum fault trip level i_{Tr11}=3 kA (2pu). Considering the maximum and minimum of values for C_{11} and without doing detailed study, a value C_{11}=300 μF is selected.

The voltage rating of capacitor C_{11} should be higher than the clamping voltage of the surge arrester SA_{11}. Therefore, V_{C11_rated}=1.5*V_{SA11_clamp} is selected. The voltage rating of the surge arrester SA_{11} should be lower than the rating of SA_{T1}, therefore, V_{SA11_calmp}=7 kV.

The resistor R_{11} discharges capacitor C_{11} and prepares it for the next opening sequence. A maximum value of R_{11} can be determined based on the minimum time between two successive opening sequences.

There is also a minimum value for R_{11} based on the minimum load current that the DC CB should trip. When the DC CB is tripping low load current, capacitor C_{11} should keep charging as long as the sub-branch is conducting. This happens if the sum currents in R_{11} and SA_{11} is less than the minimum load current in the sub-branch. Considering the equivalent circuit of this sub-branch and assuming that C_{11} is charged up to K_{SA}*V_{SA11_clamp} (K_{SA}<1), R_{11} should satisfies

$$I_L=\frac{V_{dc}-K_{SA}V_{C11\_clamp}}{R_L}>\frac{K_{SA}V_{C11\_clamp}}{R_{11}}+i_{SA11} \qquad (2)$$

where R_L represents the equivalent load resistance.

The coefficient K_{SA} should be sufficiently low to enable DC CB to trip low load current. Considering the

characteristics of the surge arresters, K_{SA}=0.8 is selected which limits $i_{SA} \leq 0.01$ kA and enables the DC CB to interrupt load currents around I_L=0.1 kA. Also considering adequate margin and the results for R_{12} and R_2, a resistance R_{11}=15 kΩ is selected. This resistor discharges C_{11} in around 18 s. Therefore the fastest next opening sequence could be in 18 s.

C. Second Time-Delaying Branch

The valve Tr_{12} is similarly composed of 19 series thyristor modules ABB 5STP 48Y7200.

By triggering the valve Tr_{12}, the thyristor valve Tr_{11} undergoes reverse recovery process. The valve Tr_{11} becomes fully off if $V_{c12}<V_{c11}$ for $t>t_q$, where t_q is the extinction time which is t_q=700 μs for the selected thyristor. Assuming fault current i_{Tr12}=8 kA (at the instant of firing T_{r12}), and $V_{c11}=V_{SA11\_calmp}$=7kV (ignoring voltage drop of V_{c11} for t_q):

$$\frac{dv_{C12}}{dt} = \frac{i_{Tr12}}{C_{12}} \Rightarrow C_{12} = \frac{i_{Tr12}}{\Delta v_{C12}} \Delta t > \frac{i_{Tr12}}{v_{C11}} t_q = 800 \mu F \quad (3)$$

Assuming adequate margin, C_{12}=1000 μF is selected.

The voltage rating of the surge arrester SA_{12} is selected between the voltage rating of SA_{11} and the main surge arresters, therefore V_{SA12_clamp}=60 kV is selected.

The resistance R_{12}=4.5 kΩ is similarly selected.

D. Arming Branch and main Surge Arrester

The valve Tr_2 is similarly composed of 38 series thyristor modules ABB 5STP 48Y7200.

The capacitance C_2 is calculated similarly based on reverse recovery time of valve Tr_{12} and C_2=180 μF is selected.

The voltage rating of the main surge arrester SA is selected to have its clamping voltage around 1.5 times the DC line voltage level. Therefore, V_{SA_clamp}=1.5*120kV=180 kV.

The resistance R_2=25 kΩ is similarly selected.

E. Switch S_2 and series inductor L_{dc}

The residual current breaking (RCB) S_2 is a switch with residual chopping current I_{res}=10 A and time delay T_{res}=30 ms.

The series inductor L_{dc} is used to limit the rate of rise of fault current. Considering the worst case scenario, R_f=0 and ignoring the valves ON resistance, and also assuming that the fault current will reach I_{fpk}=10 kA from the nominal current I_{dcN}=1.5kA during the fault interruption time $T_{int} \geq 7$ ms, L_{dc} is:

$$V_{dc} = L_{dc} \frac{di_f}{dt} \Rightarrow L_{dc} = \frac{V_{dc}}{\left(\Delta i_f / \Delta t\right)} > \frac{V_{dc}}{\left(\left(i_{fpk} - i_{dcN}\right)/T_{\text{int}}\right)} > 99mH \quad (4)$$

Assuming adequate margin, L_{dc}=150 mH is selected.

IV. Hybrid DC CB Controller

A. Opening Sequence

The opening sequence starts when the DC CB is in normal operation (LCS T_1 and UFD S_1 are closed), all capacitors in the main breaker branch are discharged and a trip order is received. The opening sequence is summarized in Table I. The T_{Tr11} is the conduction time of the first time-delaying branch.

Table I
Opening sequence of thyristor-based hybrid DC CB

	Inputs	Action
1	(Is trip order received?) & (All capacitors are discharged?)	Open LCS T_1
2	Is LCS T_1 opened?	Trigger Tr_1 & Tr_{11}
3	(Is LCS T_1 opened?) & ($i_{Load} < I_{res}$?)	Open UFD S_1
4	($V_{C11} > K_{SA} * V_{SA11\_calmp}$?) & ($T_{Tr11} \geq T_{mec}/2$)	Trigger Tr_1 & Tr_{12}
5	(Is S_1 fully opened?) & ($V_{C12} > K_{SA} * V_{SA12\_calmp}$?)	Trigger Tr_2
6	Is $i_{dc} < I_{res}$?	Open RCB S_2

B. Closing Sequence

The closing sequence starts when the DC CB is in open state (LCS and UFD are open) and the capacitors C_{12} and C_2 are discharged. Note that there is no need for capacitor C_{11} to be discharged as the valves Tr_1 and Tr_{11} can be turned on even if C_{11} is fully charged.

The closing sequence is summarized in Table II. Note that UFD S_1 can be closed as soon as V_{C11} is partially charged. The first time-delaying branch includes capacitor charging time and SA conduction time and it must conducts until UFD S_1 is fully closed.

Table II
Closing sequence of thyristor-based hybrid DC CB

	Inputs	Action
1	(Is closing order received) & (Are C_{12} & C_2 discharged?)?	Close RCB S_2
2	Is S_2 fully closed?	Trigger Tr_1 & Tr_{11}
3	(Is $V_{C11} > 0.5 * V_{SA11\_calmp}$?)	Close UFD S_1
4	(Is S_1 fully closed?)	Close LCS T_1

C. Thermal model

Fig. 2 shows the block diagram of model of the junction temperature of each IGBT/thyristor, which is required to be monitored in order to prevent overload.

The thermal impedance between junction and case (Z_{thJC}) is sum of four first order filters. The gain (R_i) and time constant (τ_i) of filters are given in datasheets for switches.

The parameter K_{CH} represents the case-heatsink thermal impedance which is respectively equal to 1.25 and 1.0 for IGBT valve T_1 and thyristor valves. The IGBT valve T1 conducts steady-state load current and the case-heatsink thermal impedance of the IGBT should be taken into account which is 25% of its junction-case thermal impedance. The thyristor valves conduct short transient fault current and there will be minimal thermal conduction between the case and heatsink during this very short time.

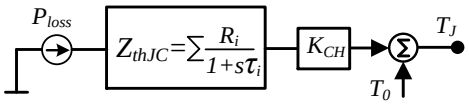

Fig. 2. Thermal model an IGBT/thyristor module

The environment temperature is represented by T_0. It is selected 40 ºC for IGBT valve with water cooling system and 35 ºC for thyristor valves with air cooling system.

The power P_{loss} for IGBTs and thyristors is calculated as

$$P_{loss\_IGBT}(t) = V_{CE0\_IGBT} \cdot i_{IGBT}(t) + R_{ON\_IGBT} \cdot i^2_{IGBT}(t)$$
$$P_{loss\_Th}(t) = V_{CE0\_Th} \cdot i_{Th}(t) + R_{ON\_Th} \cdot i^2_{Th}(t) \quad (5)$$

where R_{on} is the ON resistance of each IGBT/thyristor and V_{CE0} is the forward drop voltage of each IGBT/thyristor.

V. Simulation Results

A. Test system

A simple test system including a fixed DC voltage *120kV*, a DC CB and a load 80 Ω is developed in PSCAD. The system parameters are given in Table III and Table IV.

The following tests are simulated to evaluate the performance of the DC CB:

- Case 1: Opening on grid order at various currents,
- Case 2: Closing on grid order

The monitored signals are currents, voltages, temperatures and switching status. However, only some of the above tests results are shown here for brevity.

Table III
Main parameters of thyristor-based hybrid DCCB

Parameters	Value
Voltage rating	120 kV
Current rating	1.5 kA
Peak interrupting current	10 kA
IGBT module	ABB 5SNA 2000K450300 (4500V, 2000A)
Thyristor module	ABB 5STP 48Y7200 (7200V, 4840A, t_q=700µs)

Table IV
Design parameters of thyristor-based hybrid DCCB

Branch	valves	V_{SA_clamp}	Capacitor	Resistor
Main	3x3 IGBT (T_1)	12 kV	---	---
First	19 series thyristors (Tr_{11}) 19 series thyristors (Tr_1)	7 kV	300 µF (10.5 kV)	15 kΩ
Second	19 series thyristors (Tr_{12})	60 kV	1000 µF (90 kV)	4.5 kΩ
Arming	38 series thyristors (Tr_2)	180 kV	180 µF (240 kV)	25 kΩ
Series inductor and Switches	L_{dc}=0.15H	UFD S_1: (T_{mec}=2 ms, I_{res}=0.01 kA) RCB S_2: (T_{mec}=30 ms, I_{res}=0.01 kA)		

B. Opening on grid order

Fig. 3 and Fig. 4 show the switching states and currents of the DC CB on receiving grid trip order after a fault at 0.5 s. It is seen that the fault interruption time is around 11 ms. This long interruption time is result of large capacitors in the time-delaying and arming branches which are required considering extinction time of the selected thyristor. This time can be reduced if thyristors with smaller extinction time are selected.

Fig. 5 shows the voltages of the DC CB for the same fault in Fig. 4. It is seen that the capacitors voltages (v_{C11} and v_{C12}) rise up to their threshold limit (K_{SA}*V_{SA11_clamp} and K_{SA} *V_{SA12_clamp}) and discharge into their resistor when the fault current commutates to the next sub-branch. The capacitor voltage v_{C2} and the breaker voltage v_{DCCB} rise up to V_{SA_clamp}. The breaker voltage v_{DCCB} drops to V_{dcN} (120kV) when the DC CB current becomes zero.

Fig. 6 shows the junction temperature of an IGBT module of valve T_1, and each thyristor module of valves Tr_1 and Tr_2. It is seen that the temperatures are well below the limit 120 ºC. This implies that the thyristor-based DC CB can interrupt much higher fault current from the switches junction temperature point of view.

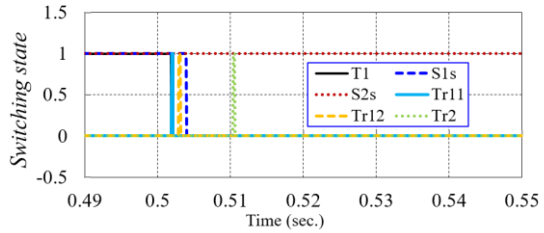

Fig. 3. Switching states (Opening on grid order)

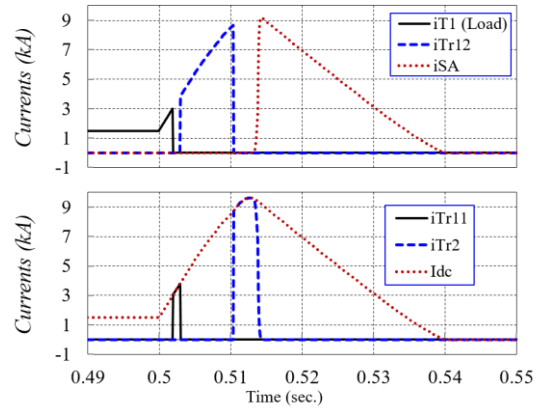

Fig. 4. Branches currents (Opening on grid order)

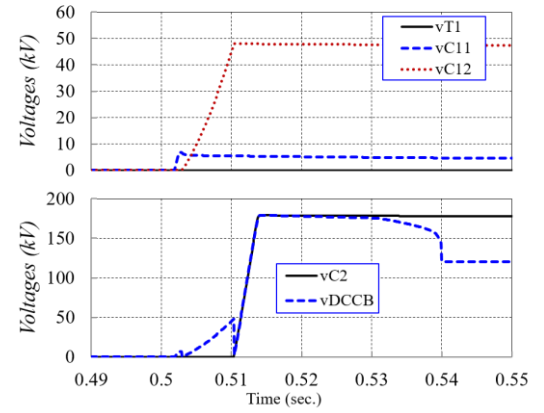

Fig. 5. Capacitors and DC CB Voltages (Opening on grid order)

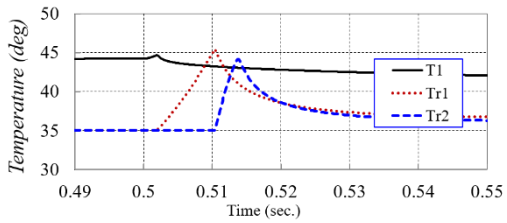

Fig. 6. Junction temperature (Opening on grid order)

C. Closing on grid order

A closing order in normal operating condition (fault cleared) is issued at t=1 s, and Fig. 7 show the DC CB switching states, while Fig. 8 shows currents and voltages. It is seen that capacitor C11 takes load current and voltage v_{C11} builds up until it reaches SA_{11} clipping voltage (7kV). This low voltage enables closing S1 at zero current while T1 is exposed to acceptable voltage stress. Once S_1 is closed (after 2ms) T_1 is closed and normal current branch takes full load current.

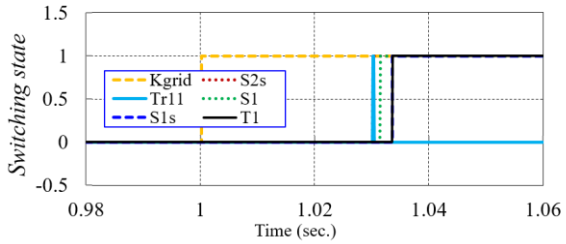

Fig. 7. Switching states (Closing on grid order)

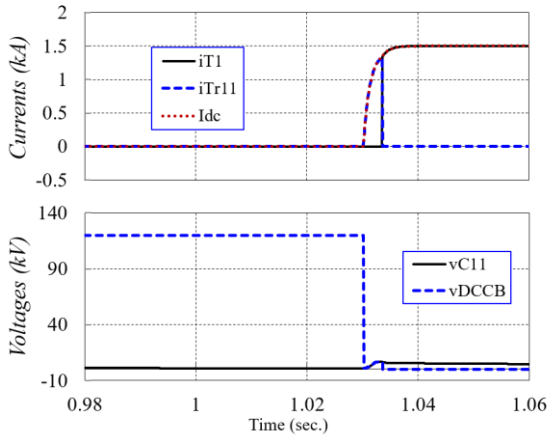

Fig. 8. DC CB Currents and voltages (Closing on grid order)

VI. Conclusion

A 120kV, 1.5kA thyristor-based hybrid DC CB design is investigated and DC CB is modelled in PSCAD. The breaker system level model is suitable for DC grid protection development and transient studies involving DC faults.

It is concluded that the parameters of DC CB depend on the voltage and current rating, but also on the properties of selected semiconductors, like extinction time of thyristors.

Simulation results conclude that the model shows good responses for both, trip and close commands. It is also concluded that the thyristor-based DC CB has the potential of much higher current rating thanks to higher non-repetitive surge current rating and lower ON resistance of phase-control thyristors. The interrupting current rating is limited by the capacitor sizes. An issue with this thyristor-based DC CB is the long fault interruption time, which is consequence of extinction time for phase-control thyristors.

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