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Mechanical DC circuit breaker model for real time simulations

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ABSTRACT

The main goal of the paper is the modeling of the mechanical circuit breaker (MCB) that can replicate the breaker characteristics in real time environment. The proposed MCB with active current injection is modelled for a system level, which provides adequate representation of the circuit breakers for system analysis studies. External current-voltage characteristics of the proposed MCB models replicate the ones of the devices in the real world. It is well known that the DC circuit breaker (DCCB) needs to interrupt DC faults very quickly in order to avoid converter damages. The total current interruption time consists of fault detection time, time needed for the DC protection to provide command to the DCCB, and DCCB arc clearing time. Thus, it is necessary to demonstrate the system performance of associated protective devices through real time simulation, before these devices can be implemented and commissioned in practice. This paper presents a detailed modeling of the mechanical DCCB in real time simulation environment based on RTDS. The performance of the model is verified by the simulations based on PSCAD and meaningful conclusions are drawn.

1. Introduction

The growth of renewable energy sources changes the existing transmission systems. Significant progress has been made toward the development of Voltage Source Converter (VSC) based HVDC in the last few years, which enable meshed HVDC grid to provide a promising technological solution for the connection of offshore wind farms. In order to utilize the potential of offshore resources, meshed networks are urgently studied. There have been several point-to-point VSC HVDC networks in operation, connecting offshore wind resource to mainland. Meshed HVDC offshore grids will provide additional flexibility, security and sustainability to energy supply assets. The development of meshed HVDC offshore grids is hindered by a few technical barriers. One of the main barriers is the lack of reliable, fast, low loss and cost effective HVDC circuit breakers, which can allow the isolation of faulted segments from the HVDC grid and keep the healthy areas operating continuously [1].

The development of HVDC circuit breakers (CBs) is different from that of AC CBs. DC faults are not easy to interrupt because of the absence of a natural current zero. An artificial current zero is needed to be created by adding an active current injection circuit. Due to the absence of practical testing platform for HVDC CBs [2], the related transients are investigated based on the simulations conducted in RTDS environment.

Several mechanical DCCB models have been presented in the literature [3–7]. The complexity level of such models changes according to their applications. More simplistic models, like the one presented in [3–5], are conceived to be applied in system-level studies. Models proposed in [6,7] are used to clarify the physical performance as well as the interactions and stresses between internal components. Also in our previous work on Mechanical DCCB [8], a system-level model has been developed in PSCAD with the consideration of high fault current interruption and energy dissipation.

In [4], an EMTP (electromagnetic transient program) based model of the mechanical DCCB for transmission applications is presented. The model includes the main hardware components (ideal switches with delay, resonant circuit, surge arrester), the control logic and interlocks between sub-components, and self-protection feature in case of failures of the DC protection scheme. The model is proved to be robust for a large range of operating conditions (DC fault clearing, reclosing operation, self-protection, reclosing into a DC fault). Despite being a valuable starting point for developing a system level model of the mechanical DCCB with active current injection, the model is regarded too detailed for system-level studies and it is not compatible for RTDS based modelling as it would require a very fast time sampling.

All these models mentioned above are realized by making use of different software packages that do not operate in real time. However, in the future studies, one of the main issues will be the time

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requirement of DC fault current elimination. In order to avoid the damage of the DC equipment, this time should be kept as short as possible, even below 10 ms. This fault current elimination consists of fault current detection, time of protection operation, and the time that the DC CB needs to interrupt the fault current. In order to test future protective solutions, RTDS based simulations and tests will be necessary. Thus, those possible protective algorithms can be checked upon robustness, speed and sensitivity.

In this paper, a robust model of the mechanical DCCB in real time environment is presented and demonstrated based on RTDS simulations. The paper is organized as follows: Section 2 provides general information about the proposed mechanical DCCB. Section 3 describes the details of how the model can be realized in RTDS, and the verification of the model by the comparisons with an existing PSCAD model. Section 4 shows the robustness of the model and its application in Multi Terminal DC network. Finally, conclusions are addressed in Section 5.

2. Mechanical circuit breaker modelling

2.1. The structure of mechanical DCCB

The general structure of the mechanical HVDC CB with active current injection is shown in Fig. 1. In addition to the DC inductance L_{dc}, the breaker consists of three branches:

- Main branch, including a high speed mechanical vacuum interrupter (S_1), a residual current switch (S_2).
- Current injection branch, including switchable parallel resonant branches (L_p, C_{p_a}, S_{3_a}).
- Energy absorption branch, including a surge arrester which is connected in parallel with the capacitor (C_{p_a}) to limit overvoltage and absorb energy.

2.2. Mechanical DCCB components

(1) High speed vacuum interrupter

The main interrupter (S_1) contacts must separate a sufficient distance to ensure an adequate dielectric strength before Transient Interruption Voltage (TIV) can be applied. In this paper for system level DCCB model, S_1 is modelled by resistive breakers, with values of $1x10^{12}$ Ω and $1x10^{-4}$ Ω when the states are open and close respectively. It needs to be pointed out that the resistance of close state is in the order of several tens of micro ohms in practice [10]. However, the minimum resistance of the breaker in RTDS small time step is limited to $1x10^{-4}$ Ω due to RTDS operational principle.

(2) Current injection circuit

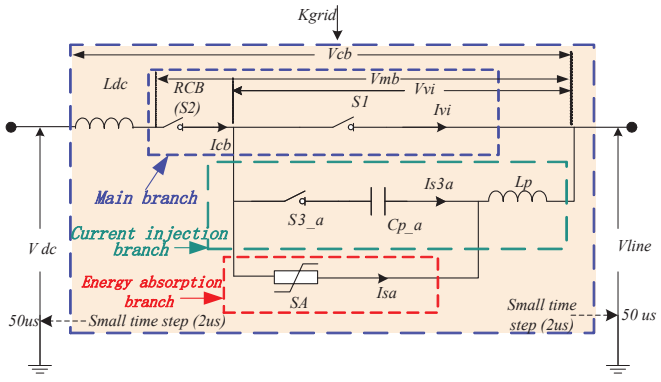


Fig. 1. General structure of the mechanical DCCB with current injection.

In Fig. 1, the resonant circuit, when it is closed by closing S_{3_a}, generates an oscillating current through the main interrupter (S_1). With a sufficient magnitude, a current zero will be generated in the interrupter.

The circuit topology is shown in Fig. 1. The current in the interrupter (I_{vi}) is given by (1). The prospective current in the resonant circuit after S_3 is closed (that is the current if the interrupter were to remain closed), is given by (2). The resonant circuit must be capable of generating a current pulse which is equal to the DC breaker current, as given by (3). However, it is common that the prospective current magnitude exceeds this by some margin to ensure that multiple current zeros are created in case the interrupter does not succeed at the first time.

$$I_{vi} = I_{cb} - I_{s3a} \tag{1}$$

$$I_{s3a} = V_{c(0)}\sqrt{\frac{C_p}{L_{s3a}}}\,sin(\omega t) \tag{2}$$

$$V_{c(0)}\sqrt{\frac{C_{pa}}{L_{s3a}}} \geq I_{cb} \tag{3}$$

$$\omega = \frac{1}{\sqrt{C_{pa}L_{s3a}}} \tag{4}$$

The balance of frequency, current magnitude and component sizes must be traded off against one another to optimize the circuit breaker functionality and costs. A higher frequency is desirable as it reduces the costs and the volume of the components in the resonant circuit. However, it also places additional stress on the vacuum interrupter (VI) in the form of a higher di/dt. This will make it challenging for the VI to interrupt successfully upon a current zero.

The capacitance and the inductance in the resonant circuit as well as the pre-charged voltage affect the profile of the discharge current for both magnitude and frequency. In the proposed DCCB model, the capacitor is pre-charged to the nominal line voltage. To achieve the required current pulse, the values of L_p and C_{p_a} must be adjusted carefully.

(3) Surge arrester

The voltage generated across the DCCB is determined by the characteristic of the Metal Oxide Surge Arrester (MOSA) placed in parallel with a resonant circuit capacitor C_{p_a}. When the current is commutated from the resonant circuit into the MOSA, the voltage rapidly rises to a level determined by the MOSA characteristic. In order to dissipate the interruption energy stored in the system, sufficient number of MOSA elements are added in parallel to absorb the required energy, which influences the clamping voltage of the DCCB. The MOSA current-voltage (I-V) characteristics are given in Fig. 2. These I-V curves are aggregated based on a number of parallel columns, with a clamping voltage of approximately 1.5pu nominal dc voltage at 16kA. The MOSA characteristics in PSCAD is described as a nonlinear resistor. However, the MOSA characteristics in small time step RTDS model is described as an Eq. (5).

$$V = V_d * (\frac{I}{I_d})^{1/N} \tag{5}$$

The characteristics of the MOSA in RTDS model and the characteristics in PSCAD are different due to the limitation of MOSA models in RTDS. The comparisons of MOSA characteristics can be seen from Fig. 2. The MOSA characteristic in PSCAD has been fitted by equation (5) and adopted in RTDS with the critical constants (N = 23, V_d = 507 kV and I_d = 8.51 kA). The representations of both curves show good matching. Table 1 shows the point list characteristic of the MOSA in PSCAD.

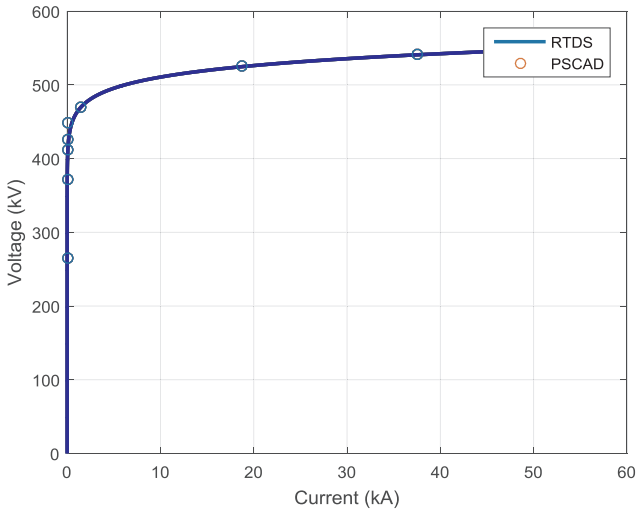


Fig. 2. Aggregated MOSA current-voltage characteristics.

Table 1
MOSA characteristics in PSCAD.

Voltage (kV)	Current (kA)
265.6	4.5e−6
371.2	1.5e−5
412.8	7.5E−5
425.6	1.5E−3
448.0	1.5E−2
470.4	1.47
524.8	18.8
540.8	37.5

(4) Residual switch

When the current through the breaker falls below a lower threshold, the MOSA conducts only leakage current. This results in an oscillation between the system inductance and the circuit breaker capacitance. The residual current switch (S_2) clears this when a current zero is created. For this situation, a standard AC breaker with a low chopping current can be used. S_2 is modelled by a resistive breaker in the simulation, with values of $1 \times 10^{12}\,\Omega$ and $0.01\,\Omega$ when it opens and closes respectively.

2.3. Principles of operation and time sequence

Each switch, e.g. S_1, S_2, S_{3_a} in Fig. 1, is modelled by some critical parameters of mechanical delays and chopping currents. The main interrupter (S_1) begins in the closed state normally and the trip signal is provided by the grid protection as an external parameter. A logic "0" represents that the protection system detects a fault and sends to the DCCB 2 ms after the fault is applied. For the switch states, a logic "0" means the switch is open and a logic "1" means the switch is closed. After a trip signal is given, a mechanical delay is added and the interrupter starts to open. The chopping current represents the minimum current through the interrupter for an arc to be sustained. Above this current, the switch remains in closed (low impedance) state. When the current goes below the chopping current value, the switch changes in an open state (high impedance).

Based on Fig. 3 [8], the basic control logic and time sequence can be observed, and relevant voltages in the circuit breaker and the switching states of the switches. V_{vi} is the voltage across the main interrupter (S1). V_{mb} is the voltage across the main interrupter (S1) and the residual current switch (S2). U_{sys} is the system voltage whilst V_{cb} is the voltage across the inductor L_{dc}, residual current switch (S2) and main interrupter (S1). During fault current interruption, when the current (I_{cb})

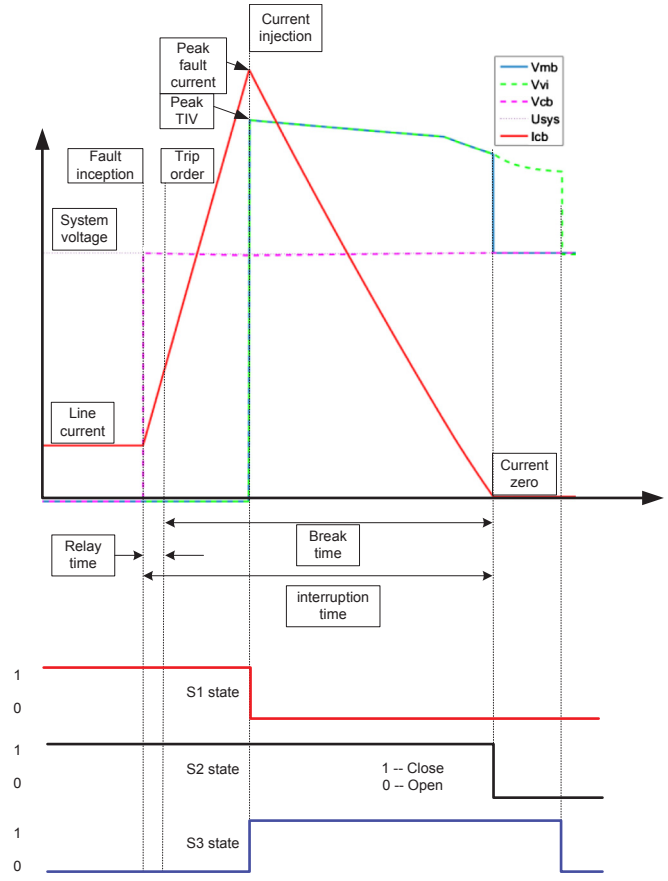


Fig. 3. Control and time sequence.

rises to its peak value, high-speed making switch (S3) closes and injects a counter current in the main interrupter (S1) that eliminates the current in the main interrupter. At the same instant, S1 changes its state from closed to open. Voltages V_{mb} and V_{vi} rise and reach their peak values. The current through the residual current switch (S2) is absorbed by the surge arrester (SA) and gradually decreases toward zero. When the current reaches zero, the state of the residual current interrupter S2 changes from closed to open. At that instant, the voltage V_{mb} drops to the value of the system voltage. The voltage across the main interrupter V_{vi} gradually decreases and at the instant when S3 changes its state from closed to open, Vvi drops to the system voltage. Based on trip signals open/close receiving from grid protection, the whole DCCB executes open/close operations in a pre-set timing sequence, which can be seen from Fig. 3. It needs to be pointed out that the time delay changes with the operating mechanism of the mechanical breakers and the system parameters, and the parameters in this paper are shown in chapter III.

3. Implementation and verification of DCCB model in RTDS environment

3.1. Test system

Fig. 4 shows the test system developed in RTDS environment to verify the performance of the DCCB model. A resistive DC source connects to the load R_{load} through a cable. The cable sections are modelled using simple T-line model in RTDS. The DCCB is connected to the output of the DC source and the other side is connected to the cable. The fault occurs at 10 km to CB and 100 km to the load R_{load}. Table 2 shows the main parameters in the CB and test circuit.

Many tests are simulated to evaluate the performance of the

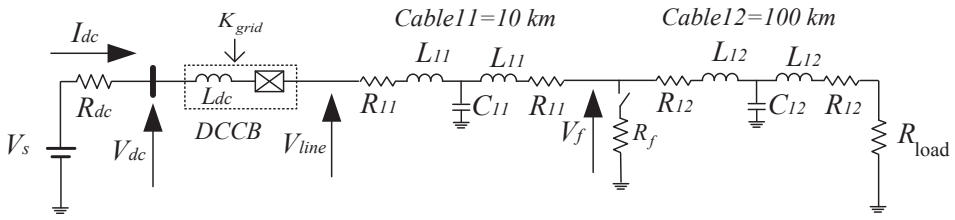


Fig. 4. DCCB test system in RTDS.

Table 2
Test circuit parameters.

Parameter	Value	Parameter	Value
Vdc	320 kV	Capacitor pre-charge voltage	V_{dcN} kV
Rdc	0.1 Ω	Clamping voltage of MOSA	480 kV
DC cable 1	10 km	Pre-charge capacitor $C_{p_a/b}$	3 μF
DC cable 2	100 km	Injection inductance L_p	1100 μH
R_{cable} (Resistance of T-line)	0.0095 Ω/km	I_{res12} (residual current for S_1 and S_2)	0.01 kA
L_{cable} (Inductance of T-line)	2.112 mH/km	I_{res3} (residual current for S_3)	0.03 kA
C_{cable} (Capacitance of T-line)	0.1906 μF/km	T_{O12} (S_1, S_2 and S_3 open mechanical delay)	8 ms
I_{dcN} (Rated DC current)	2.0 kA	T_{C12} (S_1 and S_2 close mechanical delay)	50 ms
I_{pk} (Rated interrupting current)	16 kA	T_{O3} (S_3 open mechanical delay)	30 ms
L_{dc} (DC series inductor)	0.22 H	T_{C3} (S_3 close mechanical delay)	8 ms
R_{load}	160 Ω		
R_f	0.1 Ω		

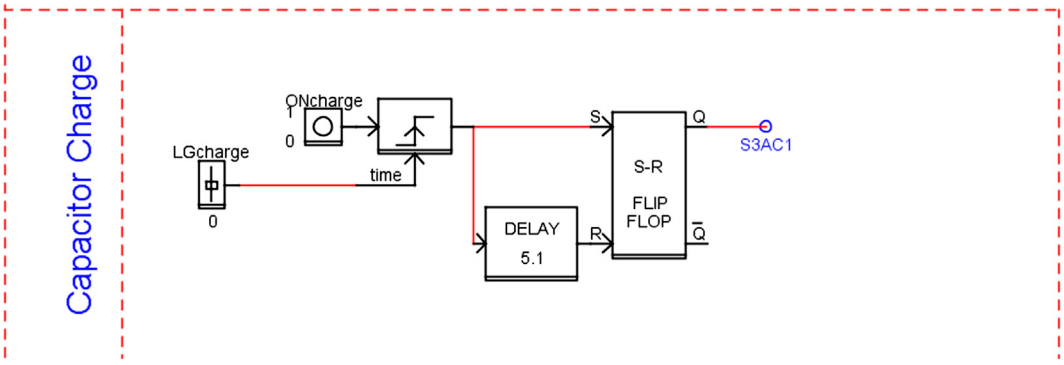


Fig. 5. RTDS Capacitor charge logic.

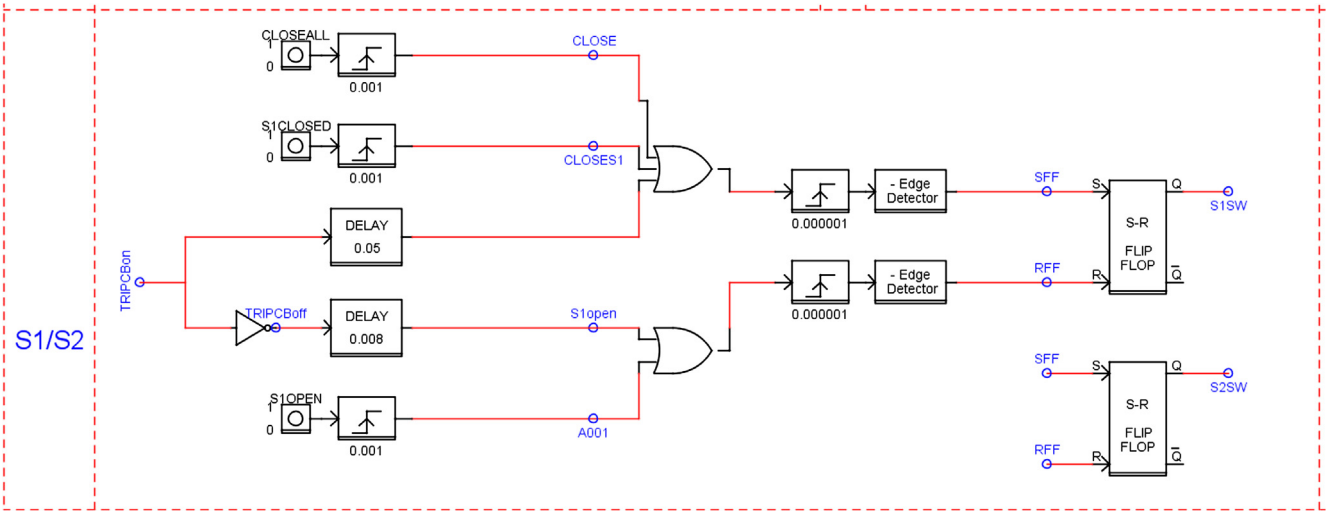


Fig. 6. RTDS S_1 and S_2 switch controls.

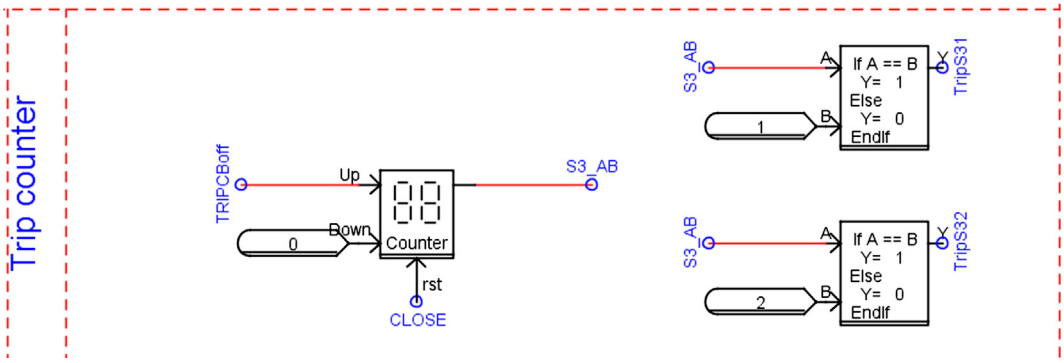


Fig. 7. RTDS Counter block for S_{3_a} and S_{3_b} close and open commands.

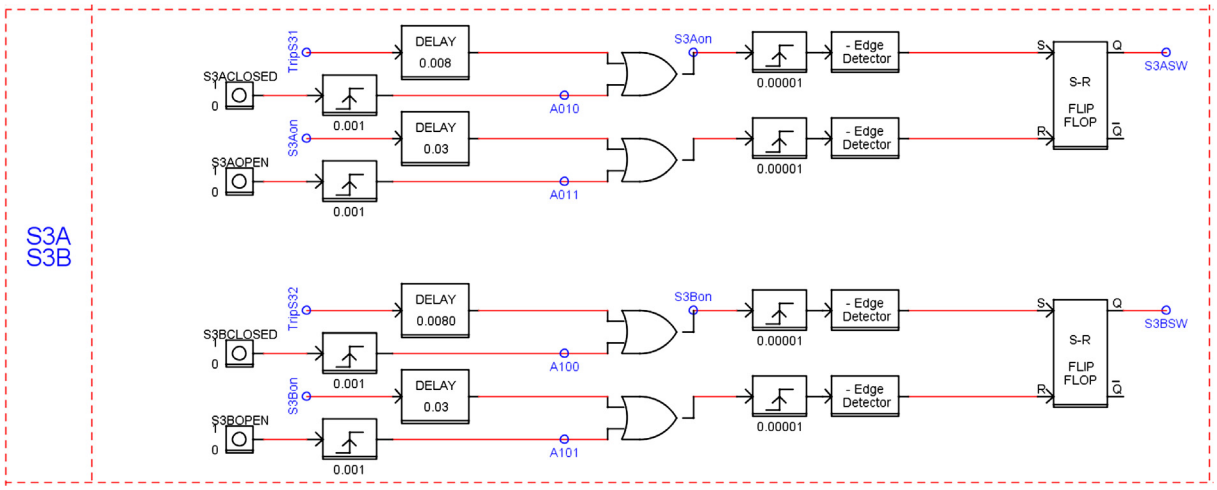


Fig. 8. RTDS S_{3_a} and S_{3_b} switch controls.

mechanical DCCB in RTDS. Only reprehensive cases and results are shown in this paper:

- Interrupting short circuit current,
- Interrupting reverse short circuit current,
- Closing into rated load current

3.2. Modelling of DCCB control in RTDS

In the draft file of RTDS, the DCCB control logic is allocated in the hierarchical box. The logic for the switches S_1, S_2, S_{3_a} and the control to charge the capacitors are enclosed. In order to have a fully charged capacitor in the resonance circuit, after starting the simulation in RTDS, it is necessary to charge the capacitors for 5 s to ensure the full charge. The related logic can be seen in Fig. 5, a flip-flop element is used with input signals from the charging button and duration.

During the normal operation state, the original positions of S_1 and S_2 are close, and the positions of S_{3_a} is open. After a fault occurs, the trip signal (i.e. TripCBon in Fig. 6) is sent to S_1 and S_2 with a 8 ms delay. Together with this open command and by the counter shown in Fig. 7, a close command is sent to S_{3_a}. This sequence provides the correct DCCB close/open commands and completes the trip actions. At this time, the positions of S_1 and S_2 are changed to open; and S_{3_a} is close. The close command in S_{3_a} (TripS31 in Fig. 7) remains for 30 ms and after this time the DCCB is ready to reclose S_1 and S_2 switches. Once the reclose command is provided by the trip signal and after 50 ms delay, S_1 and S_2 close and the status of the switches becomes equal to the initial positions.

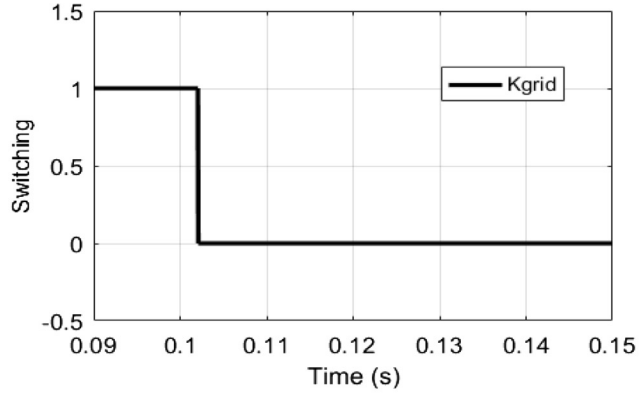
In RTDS modelling, the reclosing logic has been considered and designed, which will be realized by a second charging branch and related control logic, e.g. S_{3_b} and TripS32 related control blocks and control signals in Fig. 7 and Fig. 8. The reclosing related investigation and analysis will be presented in another paper.

3.3. Case studies and verifications

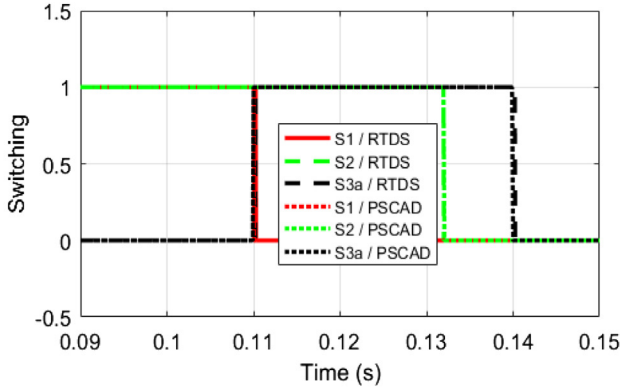
In this paper, the RTDS model is verified by an existing DCCB PSCAD model. The simulation results of the DCCB based on RTDS are drawn in solid lines whilst the results from PSCAD are in dashed/dotted lines.

(1) Short circuit current interruption

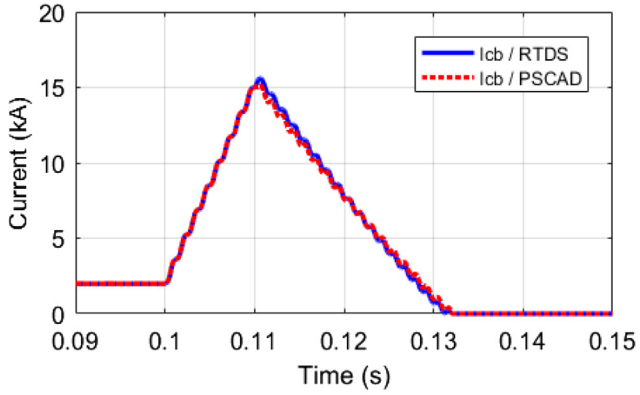
A high current (low impedance $R_f = 0.1\,\Omega$) fault is applied at t = 0.1 s and the grid protection sends trip order at t = 0.102 s. The switching signals can be seen in Fig. 9a. The K_{grid} is the trip signal from the grid protection. It changes the state from close (1) to open (0) at 0.102 s. Fig. 9b shows the breaker status. S_1, S_2 and S_{3a} change their status at the required moments both in RTDS and PSCAD. The comparison of circuit breaker current I_{cb} is shown in Fig. 9c. The I_{cb} rises after the fault and reaches the peak value at 16kA, then drops to zero after the current injection induces energy dissipation. There are very tiny differences on the decreasing parts of the current waveforms from RTDS and PSCAD resulting from the different MOSA modelling methods in RTDS and PSCAD. The comparisons of the vacuum interrupter current I_{vi}, the surge arrester current I_{sa} and the injection current I_{s3a} are shown in Fig. 9d and Fig. 9e. The I_{vi} rises with I_{cb} and reaches the peak value at 16kA, then it is interrupted by the injection current. After this interruption, the commutation current flows through the surge arrester branch. As the DCCB voltage reaches surge arrester's clamping voltage,



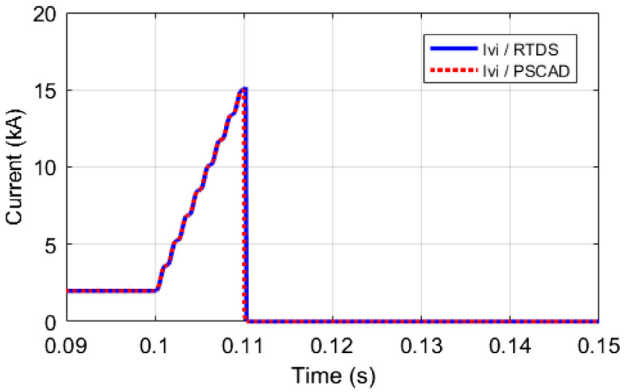
(a) Trip command from the grid



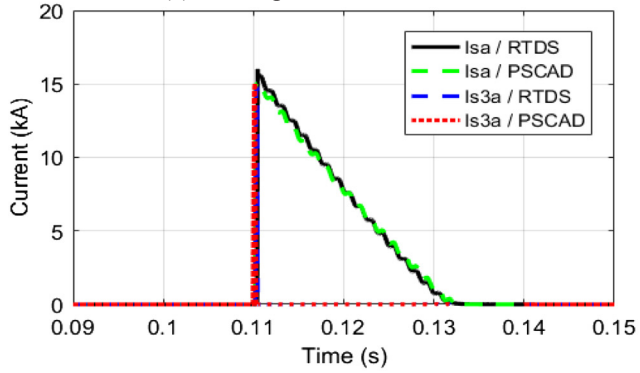
(b) Breaker status comparison RTDS versus PSCAD



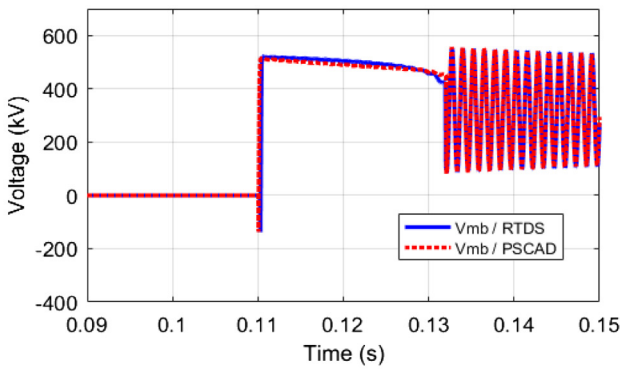
(c) I_{cb} comparison RTDS versus PSCAD



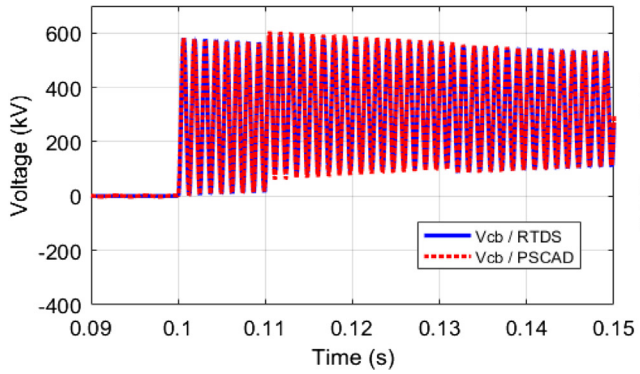
(d) I_{vi} comparison RTDS versus PSCAD



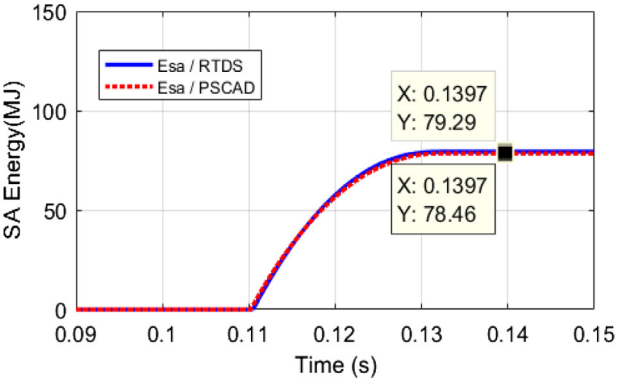
(e) I_{sa} and I_{s3a} comparison RTDS versus PSCAD



(f) V_{mb} comparison RTDS versus PSCAD

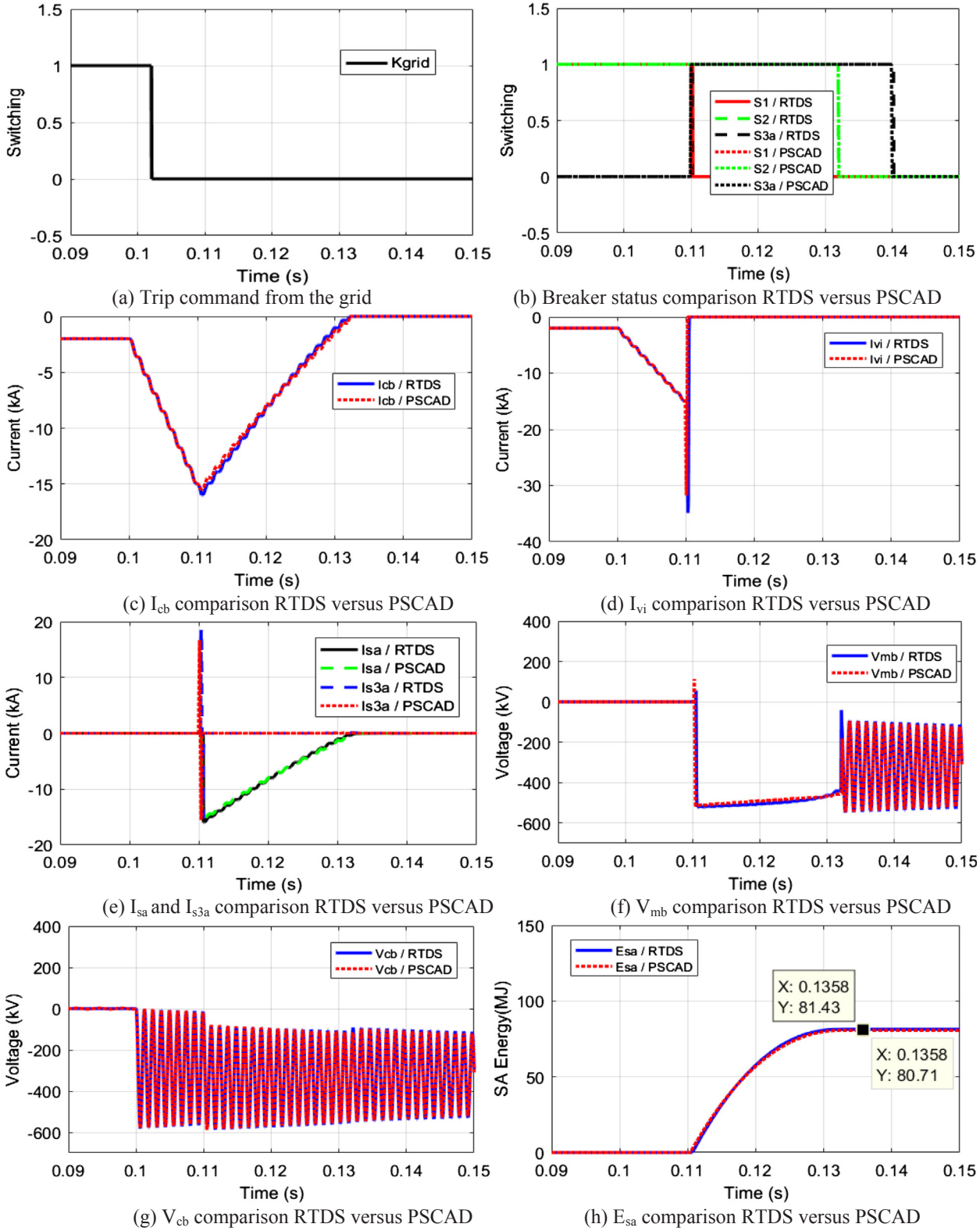


(g) V_{cb} comparison RTDS versus PSCAD



(h) E_{sa} comparison RTDS versus PSCAD

Fig. 9. The comparison on short circuit current interruption results.



(a) Trip command from the grid

(b) Breaker status comparison RTDS versus PSCAD

(c) I_{cb} comparison RTDS versus PSCAD

(d) I_{vi} comparison RTDS versus PSCAD

(e) I_{sa} and I_{s3a} comparison RTDS versus PSCAD

(f) V_{mb} comparison RTDS versus PSCAD

(g) V_{cb} comparison RTDS versus PSCAD

(h) E_{sa} comparison RTDS versus PSCAD

Fig. 10. The comparison on reverse short circuit current interruption results.

the I_{sa} rises and energy dissipates. These waveforms are matched very well, which is the reason that S_1, S_2 and S_{3a} can change their status at some required moments in Fig. 9b.

Two breaker voltages of V_{mb} are shown in Fig. 9f. The V_{mb} rises to the clamping voltage of MOSA 480 kV as soon as S_1 opens. It should be noted that at the instant of current injection, prior to the voltage rise, a negative spike could be observed. This results from the fact that at the instant of current injection, vacuum interrupter is in parallel with the C_{p_a}, the voltage is the pre-charged capacitor voltage that is negative. There is only slight difference when the voltage starts oscillating and the rest matches well. After the fault occurs, V_{cb} increases immediately and experiences a slowly damped oscillation; then the DCCB interrupts

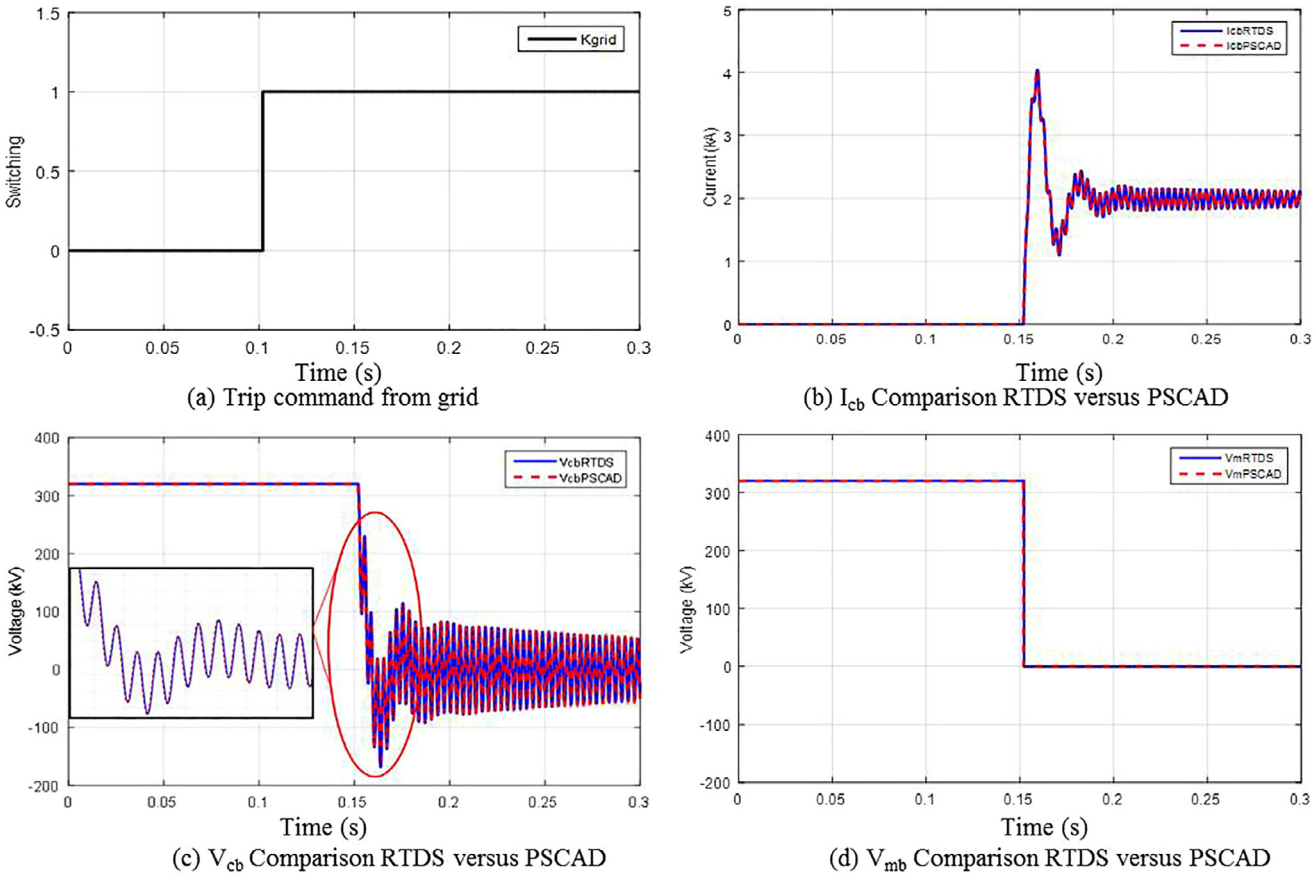


Fig. 11. Closing on receiving grid order under normal condition (Mechanical DCCB).

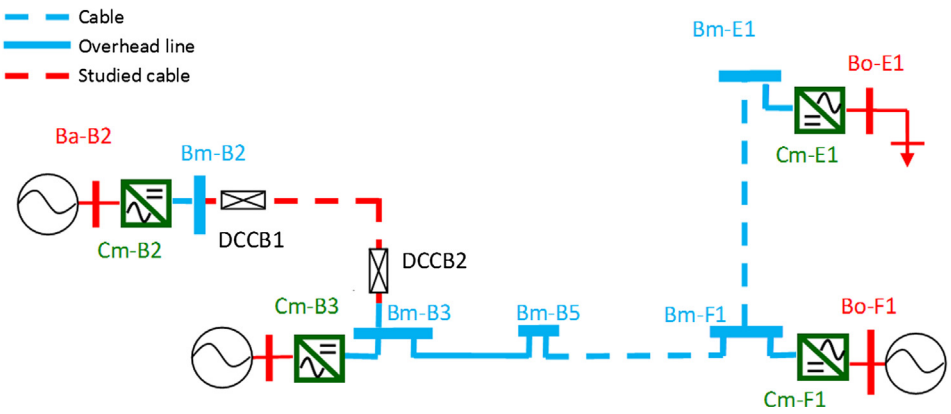


Fig. 12. Configuration of studied 4 terminal HVDC system.

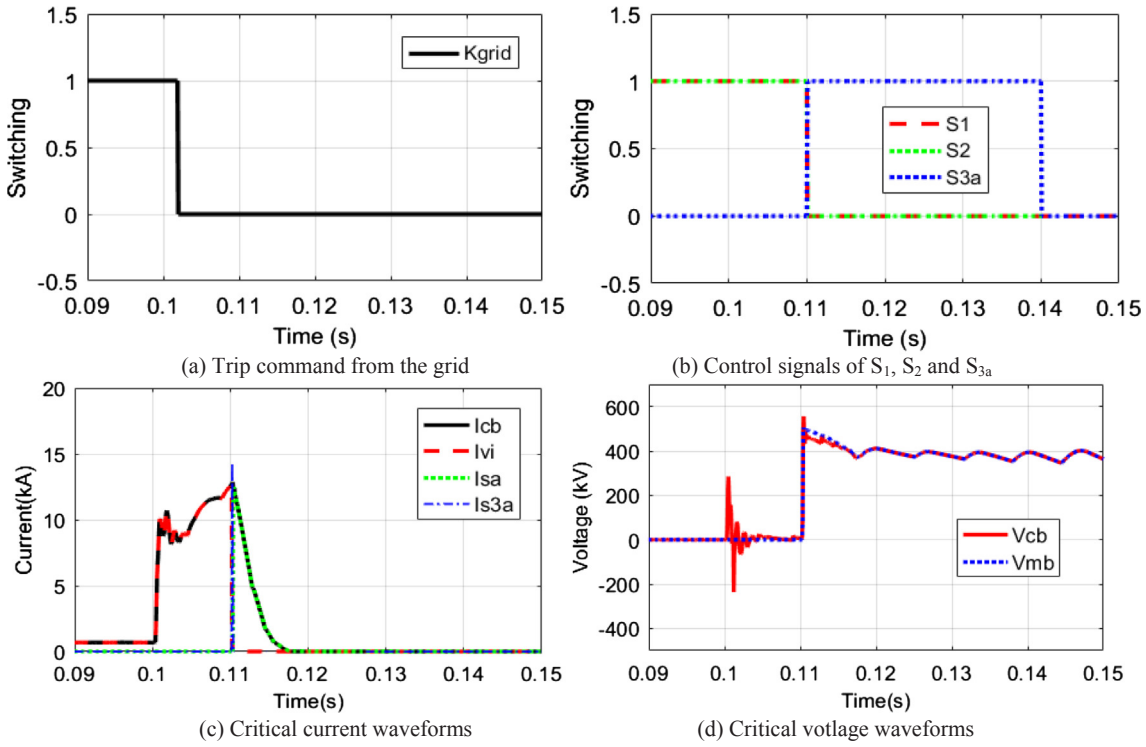
the fault and withstands the oscillation around the system voltage V_{dc}, which can be seen in Fig. 9g. The damped oscillation of V_{cb} and V_{mb} are caused by the oscillation of T-line cable model and the power source.

Fig. 9h shows the dissipated energy E_{sa} in the energy absorption branch. The absorption process starts at 0.11 s and ends at 0.134 s. The final value of the energy absorption is denoted on the graph and it can be seen that results match quite well. We have to point out again that this figure is only significant to compare the modelling in RTDS with that in PSCAD, and no conclusion can be made regarding energy absorption in practice. The results are valid only for the studied case.

(2) Reverse short current interruption

This simulation case demonstrates the circuit breaker performance when interrupting a reverse fault current in RTDS environment. The DCCB is connected in an opposite side and the measured signals are provided in the same way as in the previous models. A same high current fault (low impedance $R_f = 0.1\ \Omega$) is applied at t = 0.1 s and the grid sends a trip order at t = 0.102 s.

Fig. 10 shows the results of this case compared to PSCAD simulations. In this case, after the switch S_3 closes, the injection current I_{s3a} and main interrupter current I_{vi} flow in same direction in the beginning, which results in a current peak in the main interrupter (I_{vi}) in the order of 30kA. The natural oscillation of the current injection circuit causes a current zero half a cycle later here. At this point of current zero, the breaker interrupts the fault current in the typical manner; commutating the current in the surge arrester. However, counter-voltage (TIV) generation is of the opposite polarity.



(a) Trip command from the grid

(b) Control signals of S_1, S_2 and S_{3a}

(c) Critical current waveforms

(d) Critical votlage waveforms

Fig. 13. High current interruption results on receiving grid order in MT HVDC system network.

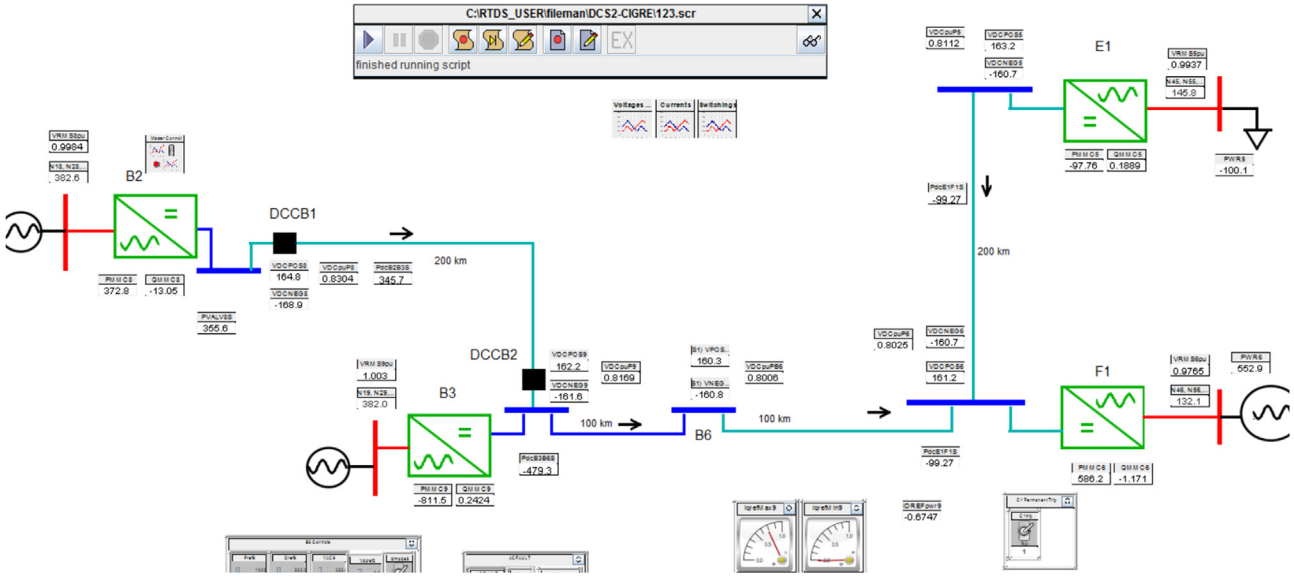


Fig. 14. Runtime platform for DCCB testing with Multi Terminal HVDC DCS2 test system.

The breaker states for all switches match well and the ability of the MOSA models represent the dissipating energy in RTDS and PSCAD environment. The similar difference in V_{mb} in Fig. 10f can be observed when the current is interrupted, and the small differences on the peak values of I_{vi} and I_{s3a} can be seen as well due to the default parasitic capacitors in the RTDS switch models. In Fig. 10h, the dissipated energies are plotted and the results are again very close to each other.

(3) Closing operation under normal condition

The simulation results of the mechanical DCCB on receiving grid close order are shown in Fig. 11. No fault is applied in the system, and the close signal is sent to the CB at t = 0.102 ms. The main current rises to 2kA which is the steady state rated current. Fig. 11a shows the switching signals. The K_{grid} is the close signal from the grid protection. A logic "0" represents that the protection system sends a close order to DCCB, afterwards the S1 and S2 take 50 ms to close. Simulated currents are shown in Fig. 11b. The CB current I_{cb} and the vacuum interrupter current I_{vi} are the same in this case, firstly they rise and experience a damped oscillation decreasing to the rated current of 2kA. In Fig. 11c the voltages are shown and in this case, the main breaker voltage V_{cb} drops to zero after a short oscillation. There are no reactions on surge arrester and capacitor branch in this case.

4. The DCCB application in MTDC grid

In order to have an efficient and reliable integration of new renewable generation, electrification of oil- and gas-platforms from onshore grids, HVDC technology has been considered as a new demanding power transmission solution. Although Multi Terminal HVDC systems have been applied in some research projects, there are very few such schemes operating in service. In this paper, the modified DCS2 test system has been adopted to testify the proposed DCCB model. DCS2, which belongs to one of the CIGRE_B4_DC_GRID_TEST_SYSTEM [9], is a 4-terminal symmetric monopole HVDC system (± 200 kV). It connects the offshore wind power plant at F1 and the offshore oil & gas platform at E1 to the onshore node B3 and extends further inland to a load centre B2 as shown in Fig. 12. This system consists of overhead lines and cables in series, to be able to capture possible interactions of those different line types (wave reflections, etc.).

In this case, the proposed DCCB models have been applied at the ends of the cables connecting DC buses Bm-B2 and Bm-B3. The DC voltages in this part of HVDC system models have been modified to (± 320 kV), which is matched with the nominal voltage level 320 kV used in the former DCCB test cases when a pole to pole DC fault is conducted. The fault occurs on the cables 50 km to the bus Bm-B2 at 0.1 s, the grid sends trip order at t = 0.102 s. The related switching signals, currents and voltages can be observed in Fig. 13.

Similarly, Fig. 13a and b shows the switching signals. The switching signals of DCCB1 are with same denotations used in the former cases based on the small test system in Fig. 4. From Fig. 13c, the CB current I_{cb} rises after the fault occurrence and reaches the peak value at 12.68kA, then drops to zero after the current injection and energy dissipation. The vacuum interrupter current I_{vi}, the surge arrester current I_{sa} and the capacitor injection current I_{s3a} also performs well. However, with this complex test system, the currents increase with more oscillations. In Fig. 13d, the differences are that more transients can be observed in the voltage waveforms when the fault occurs, and more time is required for the voltages to get stable after opening of DCCB.

In this case, the Multi Terminal HVDC DCS2 test system together with the DCCB models have been simulated by two RTDS racks with 10PB5 Processor Cards, whilst 4 VSC_Bridge blocks in RTDS library have been built for models in 2us small time steps. The runtime sib file in RSCAD provides a center control platform to run this case in real time, which can be seen in Fig. 14. Based on all above simulations and analysis, the simulation based on RTDS can give good results with enough accuracy. Compared with the real time simulation operations in RTDS, PSCAD/EMTDC approximately takes several minutes for 1 s simulation time for this case. Besides, the powerful interfaces with diverse commutation standards associated with RTDS can provide very strong and reliable Hardware-In-the-Loop (HIL) working environment, which is significant for the testing and validating of protection and control devices in the power sector, e.g. DCCB breaker prototyping testing, and HVDC protection testing, etc. The relevant HIL testing studies will be presented and discussed in our future work.

5. Conclusion

The paper presents a robust system level model of mechanical DCCB implemented in RTDS environment. The DCCB was modelled in small time step in order to obtain simulation of the switching actions of the DCCB. The comparative analysis in study cases has been given between the RTDS model and the PSCAD model. It shows that control logic signals match well with the PSCAD signals. The current signals through S1 and S2 simulated by PSCAD and RTDS are in good agreement. Slight differences can be seen in main breaker voltages, the surge arrester currents and energy absorption values due to the different way of modelling of the SA and different performance of the switches in small time steps in RSCAD environment. Moreover, the application of the proposed DCCB has been shown for an interruption of the DC fault in an MTDC grid of CIGRE B4 benchmark model. Based on the results, it can be concluded that this DCCB model can be used to test the performance of future protection schemes effectively and successfully in real time, as the most efficient way to see how particular protective solution can be implemented with respect to elimination of DC faults in future DC networks.

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