DC Chopper Based Test Circuit for High Voltage DC Circuit Breakers

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Abstract

High voltage DC circuit breakers (DC CB) are essential components for the future DC transmission grid. One of the challenges after manufacturing the DC CB is testing it and confirming the working of the DC CB under different conditions. In this paper, a 320kV, 1.5kA test circuit is proposed for testing DC CB in conditions very close to real DC transmission systems. In the proposed circuit topology a chopper is used to regulate the DC voltage. A DC capacitor bank is used to provide the energy required during the fault replication. In the test circuit the initial DC voltage is boosted by *12%* which results in a DC voltage drop of *88%* at the end of discharge period. The test circuit keeps the voltage at nominal level as soon as the fault is cleared to enable testing dielectric stress. The proposed test circuit is modelled using PSCAD and the simulation results are shown which confirm the working principle of the proposed test circuit.

1 INTRODUCTION

The use of high-voltage direct current (HVDC) transmission has been increasing because of many changes in power industry like use of remote renewable sources, increasing need for interconnections and increasing use of cable systems. There has been significant advance in HVDC technologies which have increased performance but reduced losses, costs and harmonics [1]-[3].

The DC grid is very promising concept where multiple HVDC are required, however, many challenges need to be addressed before a complete DC grid can be realized. Until recently, one of the most important challenges was the protection of the DC grid [2]-[4]. In the last 5 years several manufacturers have announced high-voltage DC Circuit Breaker prototypes and some are commercially available [5]-[8]. These devices have very fast operating time and minimal on-state losses, at the expense of high complexity and use of combination of technologies (mechanical switchgear, high voltage electronic valves and surge arresters).

An important challenge is testing the DC CB in order to confirm the working of the CB in real conditions. Different DC CB testing configurations have been proposed in literature. In [5] charged capacitors, which have enough energy to inject the required peak current, are used. In this method as the capacitors are discharged, the voltage decreases hence the DC CB is not stressed with rated voltage. Additionally, testing reclosing is not possible in this method. In [6] two different frequencies are used to generate the nominal voltage and the peak current. In this method the voltage drops in a quarter cycle of 50Hz which is 5ms. However dielectric strength testing is required for longer duration. A current source is used in [7] which cannot provide adequate voltage stress. The authors of [8] propose a method which uses a 50Hz sinewave and the authors in [9] use 16.7Hz sine wave to stress the DC CB. With this method the voltage falls to zero from peak in about 15ms. This is still too short interval since the total interruption process of the DC CB may last about 10-15ms. Additionally, testing the DC CB in high-impedance fault condition is not possible with the above circuits.

The test circuit should contain significant energy storage with fast discharge capability, since high energy pulses cannot be drawn directly from the network. The peak current stress and dielectric stress on DC CB should correspond to the conditions in the actual DC grid. A challenge with capacitive energy storage is that voltage reduces as the energy is released and this implies incorrect (lower) dielectric stress on the DC CB. Because of requirements for DC CB re-closure and repeated operations within
200-500ms cycle, the test circuit should be capable of fast recharging.

2 DC CHOPPER BASED TEST CIRCUIT

Fig. 1 shows the proposed DC CB test circuit, and all the parameters are given considering a *320kV* DC CB unit with *16kA* peak interrupting capability. The front end diode bridge rectifier (D_1-D_6) and the chopper active switch (T_{ch}) are rated for nominal current (*1.5kA*). The energy storage capacitor bank (C_s) is large and therefore its voltage cannot change rapidly. For this reason the chopper discharge diode (D_s) is placed in series with the capacitor banks, rather than in parallel as it is in the case with normal buck converters. This series connection ensures that chopper can rapidly "top up" capacitor voltage to ensure adequate DC test voltage. Since fast recovery diodes do not have good overcurrent capability, a parallel thyristor (Ts) is added to relieve diode from high (up to 15kA) discharge current. The test circuit operates either

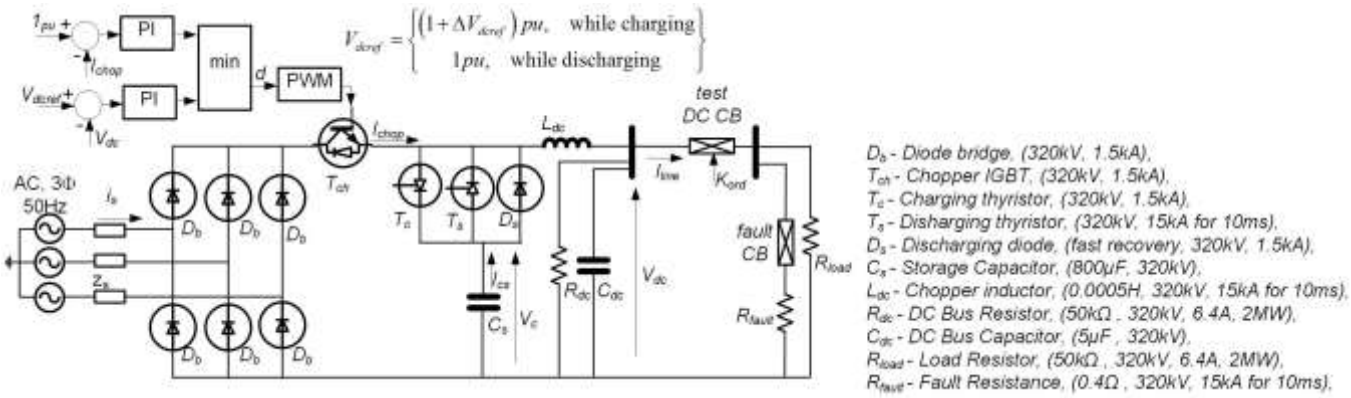

Fig. 1 320kV, 16kA, DC CB testing circuit.

in charging mode or in discharging mode. The charging mode itself has two modes. First, charging both the storage capacitor bank C_s and the DC bus capacitor C_{dc} (T_c activated). Second, charging only the dc bus capacitor (T_c deactivated). This mode is activated just after the fault is cleared to keep the DC voltage at nominal voltage as fast as possible. Hence when full dielectric stress is required, the storage capacitor bank Cs (which has a large capacity and takes longer to charge) is out of circuit.

The components C_{dc} and R_{dc} ensure stable DC voltage at the test DC CB. R_{load} is designed to provide initial current before the test is applied. Ideally the initial current should be similar to nominal current (*1.5kA*) but this may not be always feasible because of excessive heat dissipation (in case of *500MW*). Hence a 2MW load is used to partially load the system.

During the charging if the line current, I_{line}, exceeds a threshold current, the controller moves to discharging mode and remains in discharging mode for a preset time (*25ms*). Fast recovery diode D_s enables current commutation as required by *1.5kHz* operating frequency. Thyristor T_s cannot provide such fast recovery on its own. The controller block diagram is also shown in Fig. 1. There are two controller loops, the V_{dc} PI feedback control and I_{chop} PI control. These two controllers compete to get minimum duty ratio for the active switch. The current control is normally inactive but it will override DC voltage control when current magnitude is high. The fault CB is used to initiate a fault. A conventional *320kV* rated AC CB can be used since AC CBs have no technical difficulties in making large DC currents.

3 DIMENSIONING THE CAPACITOR BANK

When a fault is applied to the circuit. The capacitor bank voltage drops from V_1 to V_2. During the discharge of the capacitor bank C_s, the energy released is:

$$E_s = C_s \frac{V_1^2 - V_2^2}{2} \qquad (1)$$

There is clearly a tradeoff between voltage deviation and the capacitor size. To avoid very low final DC voltage and large capacitor, it is proposed to increase the initial test voltage. Assuming that the nominal voltage is V_{dcn}, the initial and final DC voltages can be expressed as:

$$V_1 = V_{dcn} + \Delta V_{dc}; \quad V_2 = V_{dcn} - \Delta V_{dc}; \qquad (2)$$

where ΔV_{dc} is the allowed voltage deviation. Substituting (2) into (1) results in:

$$E_s = 2\, C_s\, V_{dcn}\, \Delta V_{dc} \qquad (3)$$

The required energy release (E_s) can be determined from simulation tests with an infinite DC bus which represents ideal test circuit. Then, knowing E_s, (3) can be used to evaluate required storage size for assumed allowed DC voltage deviation (ΔV_{dc}) during the discharge test. For the test system E_s*=19.6MJ*, and with V_{dc}*=320kv*, Fig. 2 shows the capacitor size versus ΔV_{dc} in per-unit.

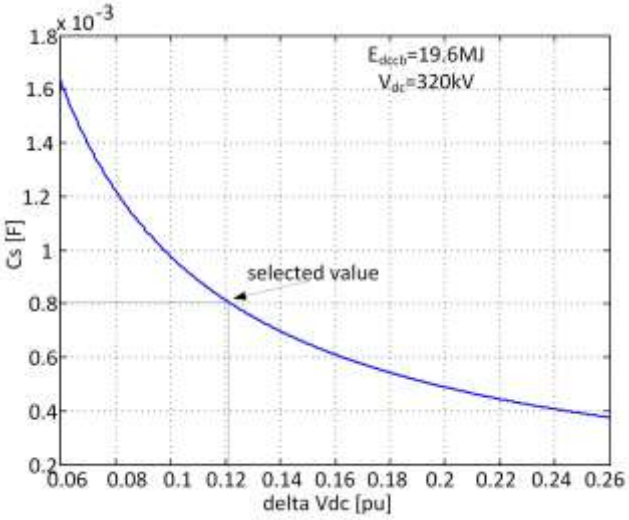

Fig. 2 Storage capacitance versus voltage deviation (±ΔVdcref) during the test.

A capacitance of 800μF is selected, requiring 12% higher initial test voltage and generating 88% DC voltage at the end of discharge period. Note that the ΔV_{dc} in Fig. 2 is in per-unit with V_{dcn} considered as a base voltage.

4 SIMULATION VERIFICATION

4.1 Single peak interrupting current test

A PSCAD model is developed for the test circuit shown in Fig. 1. The model for hybrid DC CB model is adopted from [8] and the model parameters are similar; L_{cb}*=100mH*, ultrafast disconnector time delay is *2ms*, while residual disconnector delay is *10ms*. The default arrester V-I curve in per-unit from PSCAD library is used.

Fig. 3 shows the simulation of testing the test circuit with DC CB for single interruption at peak current. The self-protection is set to trip DC CB at DC current level which, for a given L_{cb}, V_{dc} and opening time for ultrafast disconnector ensures that peak interrupting current is $0.9I_{pk}$*=14.4kA*. This calculated trip level is *8kA* for the test system. It is observed that adequate DC CB current stress is achieved at *14.4kA*. The DC CB voltage is initially (point A) around *12%* above nominal, and it reduces to *88%* of nominal by the time the arrester current is brought close to zero, (point D). After point D, although capacitor voltage V_c remains at *88%*, the chopper ensures that DC CB voltage stress V_{dc} is raised to nominal voltage V_{dcn}, this is done by deactivating the T_c. The interval DE is important for testing thermal stability of surge arresters, since in this interval the arrester temperature is at highest. After point E, nominal voltage is important for dielectric tests of residual switch. None of the test circuits given in the introduction can represent correctly voltage stress after point D.

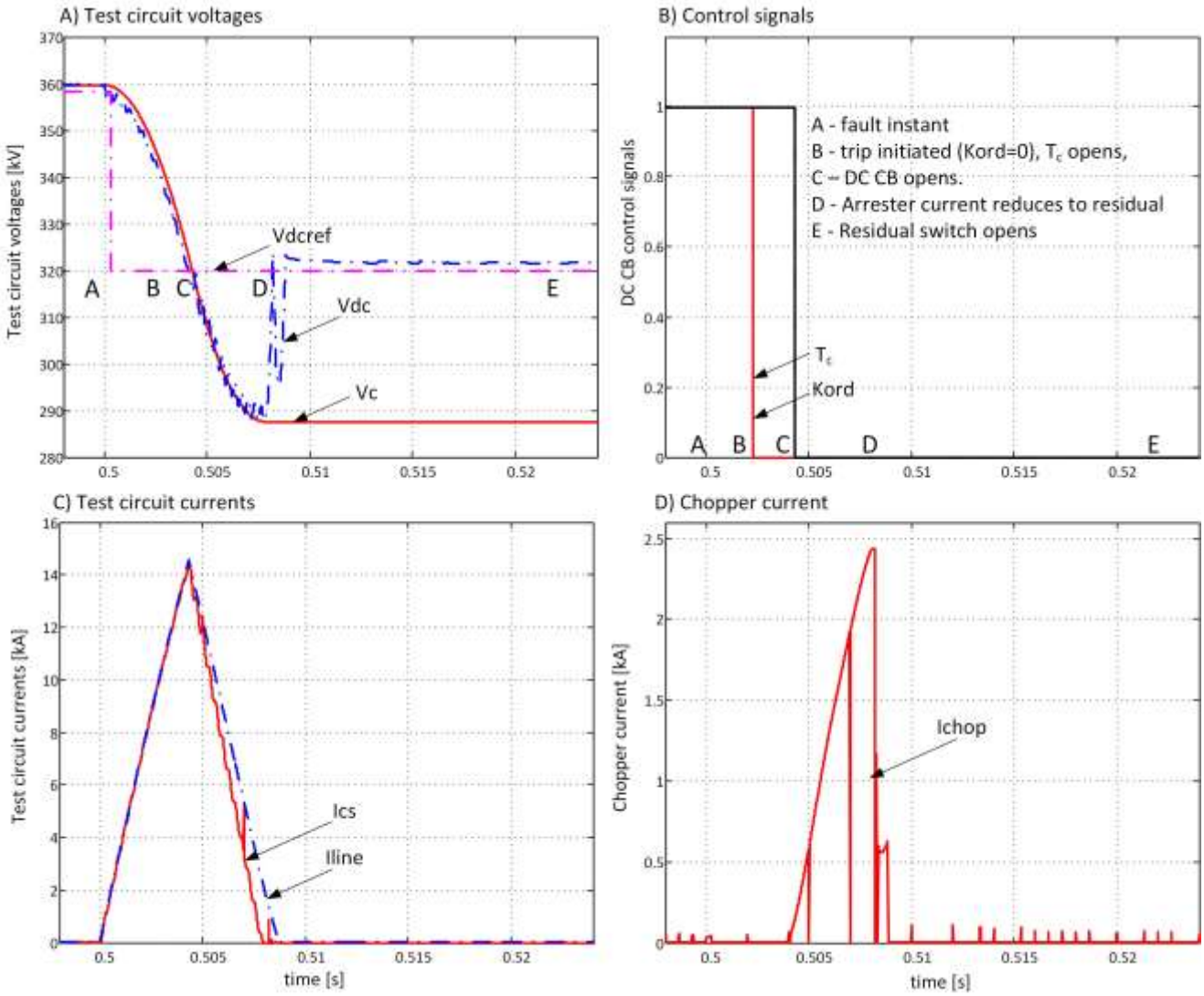

Fig. 3 Test circuit and variables for peak current test.

Fig. 3(A) illustrates that voltage reference for DC chopper is $V_{dcn}+\Delta V_{dc}$ in the pre-fault region (up to point A) and reduces to V_{dcn} during the fault condition. During the period where the Note that the standards regarding testing DC CB currently do not exist but AC CB tests specify that rated voltage should be applied immediately following current interruption [11], [12]. Similar requirements will likely exists in the case of DC CB and it can be seen that the test circuit can replicate correctly this requirement. Fig. 3(B) shows the control signals of the DC CB and the thyristor T_c. The trip signal, Kord=0, is generated as the CB current passes 8kA. At this time the switch T_c is deactivated.

Fig. 3(C) shows the DC CB current I_{line} and the capacitor bank current I_{cs}. It can be observed that the most of the fault current is fed from the capacitor banks. The difference between these two is the chopper current which is shown in Fig. 3(D). Fig. 3(D) shows that chopper current stays below rated value, which prevents any large current transfer to the diode bridge and the network.

voltage reference is V_{dcn} the thyristor T_c is deactivated to enable fast voltage recovery after the fault is cleared.

4.2 Reclosure and multiple operation

The reclosure testing capability of the test circuit is essential. System protection errors during reclosure (into permanent DC faults) might lead to particularly high stresses and fast transients, which require fast, local trip decisions. Reference [10] incorporates model for DC CB self-protection, where two decisions are employed: 1) high current threshold to prevent fast thermal overload, and energy I^2t threshold to prevent thermal overload of the CB switches.

Fig. 4 shows the tests with 3 reclosure attempts. Each time DC CB closes into a permanent DC fault and current increases until self-protection trips DC CB (no external trip signal K_{ord}). The self-protection logic is configured to attempt 2 reclosures *70ms* after each trip signal.

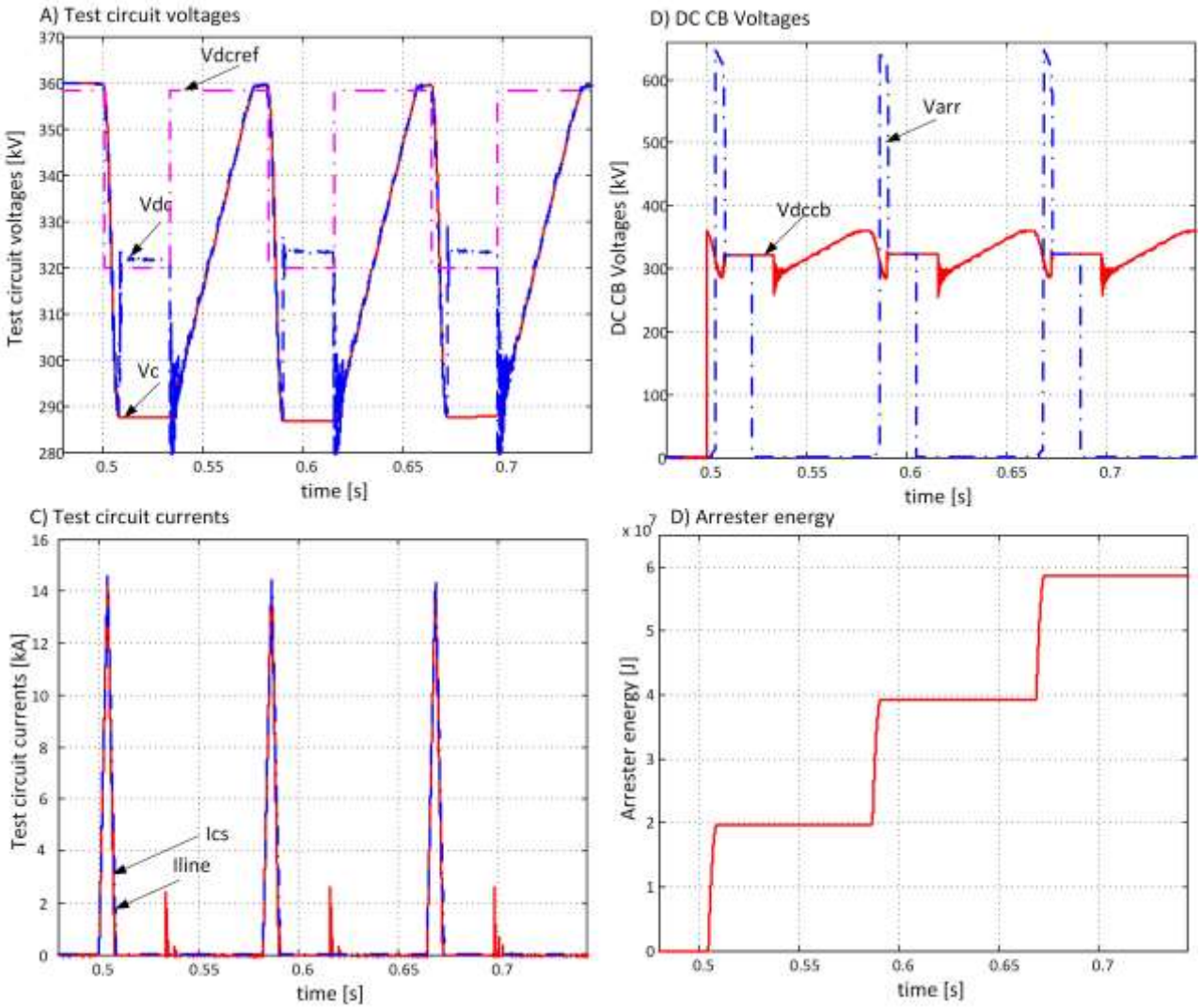

Fig. 4 Test circuit and DC CB variables for multiple reclosure test.

The test circuit is configured to recharge *25ms* after discharge signal is received. Fig. 4(B) shows the voltages across the CB and the surge arrester. It can be observed that although the voltage across the voltage reference V_{dcref}, the DC voltage V_{dc} and the capacitor bank voltage V_c are shown in Fig. 4(A). It can be observed that after fault is cleared the test circuit keeps the voltage at nominal voltage for 25ms. This duration should be sufficient to stress the DC CB after opening. Then the test circuit charges the capacitor banks and make the system ready for the next reclosure. In this test three reclosures are simulated, however practically there is no limitations for the number of reclosure from test circuit side. The DC CB is around the voltage rating, the internal components such as surge arresters voltage can go up to two per-unit. Fig. 4(C) shows the CB current and the capacitor bank current. It can be seen that these two currents are almost the same and the test circuit is not drawing high current pulses from the grid. Fig. 4(D) depicts the surge arrester energy, assuming that there is no cooling effect between each reclosures. It is seen that the arrester energy in the first interruption is *19.6MJ*, which is identical as with the infinite DC bus, and that total energy accumulates to *58MJ* after 3 interruption events. This is very important for the operation of the DC CB in reclosure mode. The DC CB surge arrester must be designed such that at the end of the reclosures total energy dissipated in the arrester do not exceed the rating of the arrester.

4.3 High impedance faults

Fig. 5 shows the testing results of the test circuit and the CB with a high-impedance fault. Self-protection of the CB is configured to trip the CB for I^2t thermal overload of the CB switches at a specified energy threshold. It takes over *20ms* of overcurrent to initiate the trip. This test requires rated voltage and current of somewhat higher than rated for a long time interval, which may not be feasible test condition with any of the test circuits mentioned in the introduction. Fig. 5(a) shows the reference voltage, DC voltage, capacitor bank voltage, and arrester voltage. The fault is initiated at 0.5s and takes more than 20ms to be detected by the protection. During this period the voltage reduces and currents goes up. As this duration is long it is difficult to be replicated by other testing circuit method. However, the CB current is interrupted at around 2.5kA, shown in Fig. 5(b), it can be seen that the arrestor voltage increases to about two per-unit.

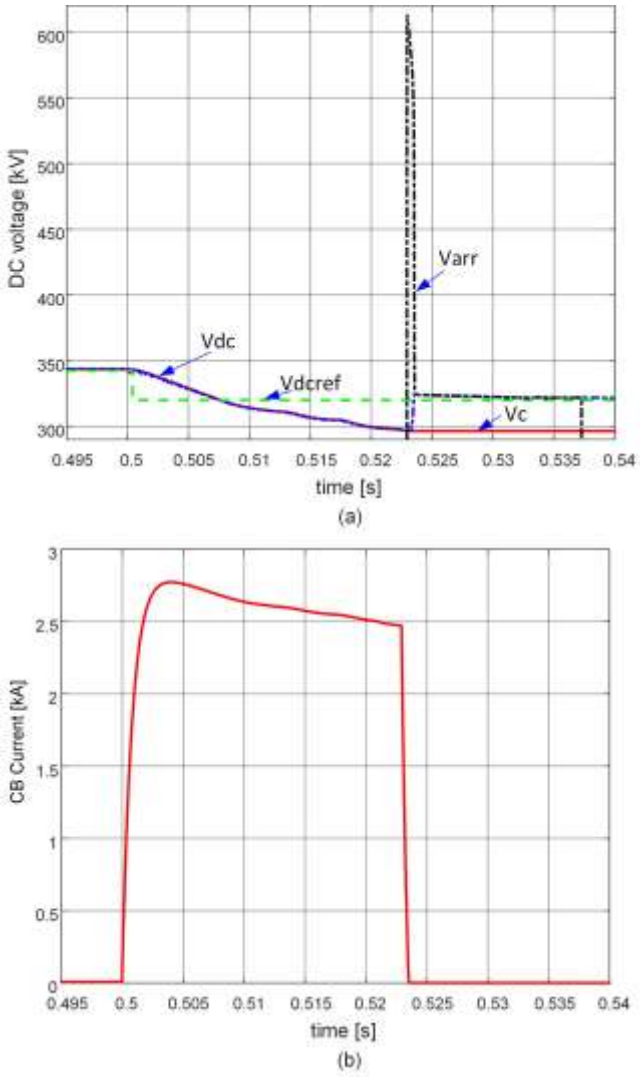

Fig. 5 Testing with high-impedance fault.

5 Conclusion

A new DC chopper-based test circuit, for testing DC CB, is proposed that largely replicates all important stress conditions on the DC CB. The test circuit employs capacitive storage banks to avoid high current pulse transfer to the network. The test circuit simulation results confirm that accurate stresses are applied on a *320kV, 16kA* DC CB test unit. Further test indicate accurate replication of stresses for multiple reclosure attempts. The fast acting chopper maintains required DC CB voltage stress through the tests. The high-impedance tests show that the test circuit can sustain overcurrent for longer period with adequate timing for voltage stress.

6 Acknowledgements

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