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Mechanical Circuit Breaker Modelling for System-level, Real-time Protection System Simulations

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SUMMARY

The mechanical dc circuit breaker (DCCB), with active current injection, has been developed to protect against dc side faults in HVDC multi-terminal systems. To reduce its cost, volume and weight, as well as operate in a short period, the natural frequency of current injection is high (typically several kilohertz). As such, a number of fast transients occur whilst commutating current between various branches within the circuit breaker.

Real-time simulation platforms can be used to assess protection strategies of multi-terminal HVDC networks (MTDC). To do so, suitable models of all major components of the MTDC are required, which are compatible with such platforms. Specifically, to facilitate real-time operations, the minimum time-step threshold must be considered. This limitation makes it challenging to implement a detailed model of the mechanical circuit breaker, where transients take place in very short time-periods. Therefore, it is desirable to reduce the complexity of the circuit breaker model to allow implementation within a real-time environment.

From a system-level design perspective, it is important that the circuit breaker model replicate key system-level quantities accurately, such as current, voltage and energy dissipation. However, it is not critical to reproduce internal stresses (such as those inside the vacuum interrupter, for example) as accurately, which would typically require detailed modelling and the small simulation time-step associated.

In this paper a simplified model for the mechanical dc breaker is introduced, for the purposes of system-level studies on a real-time platform. The loss of accuracy between detailed and simplified models is assessed and justified by comparing simulation results produced with a detailed model on EMTP-type software (which allows a wide-range of time-steps to be used). Finally, a simplified model is then implemented and demonstrated on the RTDS platform, in both normal and small time-step.

KEYWORDS

HVDC, DCCB, RTDS, Mechanical Circuit Breaker

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Introduction

DC Circuit breakers are one of the key technologies to enable the access to integrated, offshore energy via meshed dc grids. They must operate in a co-ordinated fashion, together with the rest of the protection system, to isolate faults in as shorter-space of time as possible and allow the system to return to normal operation. Transients in dc systems can be much faster than those typically found within ac, and fault propagation times are often shown to be in the order of tens of milliseconds. The fast dynamics associated with the overall dc grid's operation lends itself to small time-step transient simulations.

It is common practise to use real-time environment to validate control and protection equipment to validate previous off-line simulation work. This requires all main electrical circuits (that are not represented in hardware) to be modelled in a way that is suitable for real-time simulations, including the mechanical circuit. Typical mechanical DCCB models [1] replicate the fast transients within the circuit breaker. However, to replicate the fastest phenomena reliably, a time-step in sub-microsecond range can be required in some cases, depending on DCCB parameters. As such, it can potentially be challenging to utilise typical models, and reproduce all transients, on a real-time platform.

To allow simulations within a real-time environment the mechanical breaker model should provide the correct level of accuracy along with a time-step compatible with the MTDC grid within which it will be placed and the hardware limitations.

Mechanical DC Circuit Breaker with Active Current Injection

DC Circuit breakers must force current to zero, unlike their ac equivalents – which interrupt current on the naturally occurring current zeros. To do this, dc breakers must generate a counter voltage, which produces a negative di/dt and thus a current zero. A number of topologies have been proposed, and some of these have been prototyped at high-voltage [2-4]. To fulfil the fast operation requirements typical of HVDC systems, the mechanical breaker with Active Current Injection (referred to within this paper simply as the mechanical breaker) has been developed [5, 6].

The main circuit diagram of the mechanical breaker is shown in Figure 1(a) [4, 5]. In the closed-state, the device exhibits a very low loss path (similar to that of a typical ac breaker). This reduces losses, which is a key factor for HVDC multi-terminal system and circuit breaker development. The mechanical construction results in high-current interruption capability (16 kA [6]), making it suitable for operation within VSC–based HVDC systems. The current injection circuit allows the breaker to force a current zero within the main interrupter – with the first current zero occurring within a quarter-cycle. Key operating principles are described below.

Stage 1: Pre-Trip

During this period, the circuit breaker has not been activated (S_1 and S_2 are closed, S_3 open). If a fault has occurred, the current may be rapidly rising. However, this is not a strict necessity, as the circuit breaker may also function whilst current is within normal range for the line (i.e. switching-out a line, rather than breaking a fault).

Stage 2: Contact Separation and Arcing

This period begins when the circuit breaker receives the trip signal. The actuator then beings moving. When the contacts separate, an arc is drawn.

Stage 3: Current Injection

When the contacts have reached a sufficient separation distance the making-switch S_3 is closed, which causes current to be injected into, and circulated through, the main interrupter S_1. The time duration (to achieve a current zero) depends on several factors: current direction

positive or negative); magnitude of current to be interrupted; frequency of injected current; prospective magnitude of peak current. This time is in the order of tens to hundreds microseconds, based on a frequency of several kilohertz.

Stage 4: Voltage Rise

At the end of Stage 3, a current zero has been generated in the main interrupter S_1. At this point, it can be considered as open-circuit (open-state), all current must pass through the parallel (energy absorption and current injection) branches.

Stage 5: Energy Dissipation

During this period, the surge arrester clamps the voltage across the main interrupter to the desired level. The voltage generated across the DCCB is termed the Transient Interruption Voltage (TIV). Energy stored in any system inductance, and contributed from other sources (such as converters), will be dissipated in the DCCB as current decreases. The end of this stage is marked by the circuit breaker current passing through zero, and the end of energy dissipation.

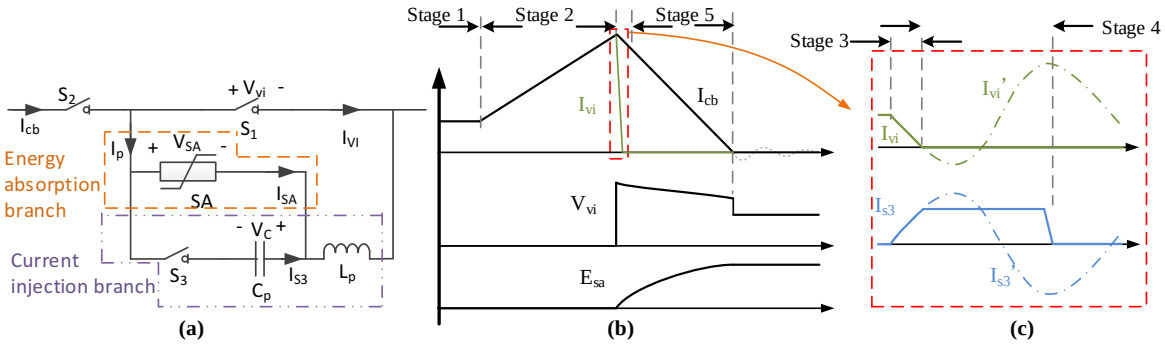

Figure 1: Mechanical circuit breaker topology and key waveforms during interruption. Dashed lines represent prospective currents (i.e. if no interruption occurred)

Current-zero Interruption Capability

The volume, weight and cost of the active current injection branch components is strongly related to the passive component values. These, in turn, govern both the natural frequency and peak current of the prospective current injection. The peak current generated by the current injection branch is determined by the passive components. Ignoring any damping effects, the peak prospective current (i.e. without interruption) is given by (1). The capacitor pre-charge voltage V_{c_I} is typically the same as the dc-line voltage and, thus, assumed fixed. Therefore, the ratio of capacitance C_p to inductance L_p may be adjusted to influence the current magnitude. In practice, it is common to over-rate the current injection magnitude (i.e. the prospective current is larger than the rated current) to allow for a number of items, such as damping and reverse current operation. In this paper, a 30% margin is assumed in the simulation results given.

$$|I_p| = V_{c\_I}\sqrt{\frac{C_p}{L_p}} \qquad (1)$$

To reduce the values of both L_p and C_p it is desirable to increase the frequency, which is given by (2). The rate-of-change of current at the point of current-zero crossing is determined by the natural frequency of the circuit $|I_p|$ (1) and ω_n (2), as shown in Figure 2. A higher di/dt places a larger stress on the interrupter; limiting its interruption performance [5, 6]. Therefore, there is a trade-off between higher frequency and required interruption current. Due to this, the natural frequency of the current injection circuit is typically less than 10 kHz.

$$\omega_n = \frac{1}{\sqrt{C_p \cdot L_p}} \qquad (2)$$

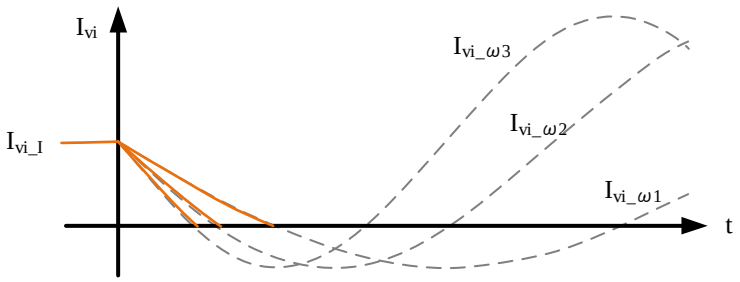

Figure 2: Influence of natural frequency on current-zero profile

Initial Transient Interruption Voltage Stress

The main interrupter is subjected to severe stress during interruption, in particular at current-zero and during the TIV phase. At the point of current-zero creation the main branch forms an open circuit. Ignoring effects of damping, the instantaneous capacitor voltage $V_{c,}$ as expressed in (3). The time-period for current to reach zero ΔT_{i0} can be estimated by (4), where I_{vi_I} is the interrupted current. At this point, the capacitor voltage V_{vi_0} is applied across the main interrupter S_1, which can be can be approximated by (5). This demonstrates that the ratio of I_{cb_0} to $|I_p|$ is inversely related to the applied voltage; i.e. interrupting smaller currents results in a higher applied voltage. Figure 3 shows this effect, for a range of interrupted current magnitudes.

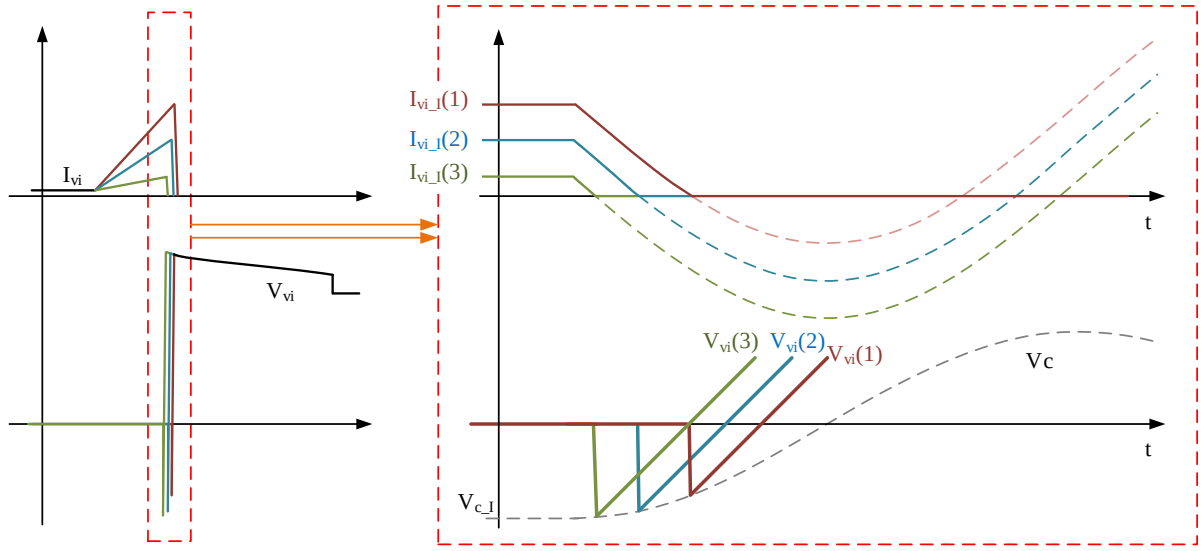

Figure 3: Influence of interrupted current on main interrupter initial TIV stress. Dashed lines represent the prospective current and voltage profiles if interruption does not occur

After current interruption, the capacitor voltage will rapidly increase. The rate of increase is proportional to C_p and I_{cb_I}. The current will continue to increase until the surge arrester begins to conduct, clamping the voltage and commutating current away from the capacitor.

$$|V_c| = \cos(\omega_n \cdot \Delta T_{i\_0}) \tag{3}$$

$$\Delta T_{i\_0} = \frac{1}{\omega_n} \sin^{-1}\left(\frac{I_{vi\_I}}{|I_p|}\right) \tag{4}$$

$$|V_{vi\_0}| = \cos\left(\sin^{-1}\left(\frac{I_{vi\_I}}{|I_p|}\right)\right) \quad (5)$$

This initial transient across the main interrupter is particularly fast. Sample simulation results are shown in Figure 4 , which demonstrate the fine time-step required to capture the initial [negative] TIV. In the cases performed, if the time-step was increased beyond 20µs the simulation failed to commutate current out of the main interrupter, and thus did not interrupt. This limitation depends on a number of factors, including the interrupted current and the resonant frequency of the commutation circuit. In the case given here, 5 kHz was assumed. For higher frequencies, the maximum time-step must be reduced accordingly. The feasible range for which this type of model can be used directly within a real-time system is therefore constrained.

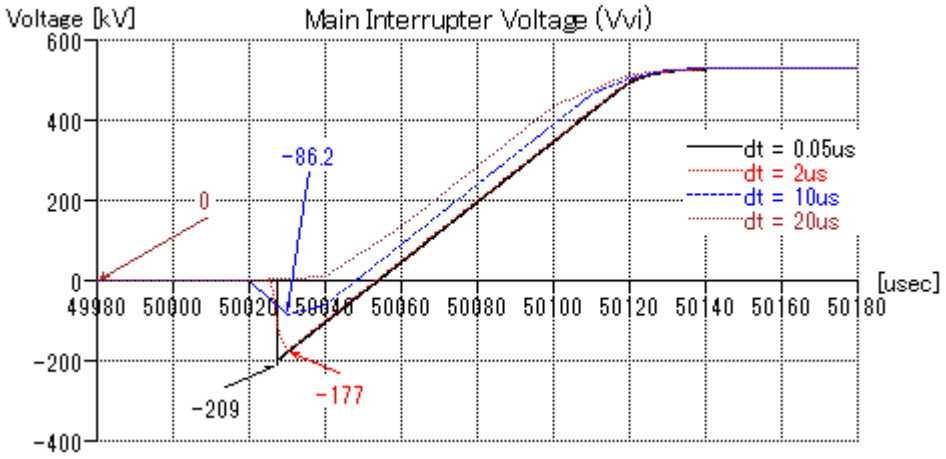

Figure 4: Simulation results of the initial transient interruption voltage across the main interrupter, performed with EMTP software. Simulation cases with various time-steps have been shown to illustrate the difficulty in accurately capturing the transient.

RTDS Model for System Studies

To verify the operation of the overall protection and control system of the HVDC network, suitable models of all major components must be available – this includes the DCCB. Operation at real-time requires that all computations can take place - continuously - within the time-step associated with the simulation. Lower limits on the time-step are governed by the hardware available. To achieve reasonable accuracy and interpolate between data points, it is desirable to have a time-step in an order of magnitude smaller than the highest frequency of interest. Due to the high frequency of the current injection circuit, the mechanical circuit breaker intrinsically generates very fast transients and capturing all information in real-time is challenging. In this section, RTDS model simulation results of the dc breaker are compared against those using a typical model (shown in Figure 1), simulated on an EMTP platform with fine-resolution time-step. It should be noted that the simulation results given have been simulated using a simplified test circuit, and do not therefore represent full system studies. As such, energy dissipation is not directly proportional to that expected in a multi-terminal network.

Key Phenomena

Given the constrained of modelling on a real-time platform, the desired phenomena which are required for measurement and observation should be assessed. For system-level simulations it is important that Stages 1, 2 and 5 (Pre-Trip; Contact Separation and Arcing;

and Energy Dissipation) are replicated with a reasonable degree of accuracy. The time-duration of each of these is in the order of several milliseconds and, thus, they can be readily simulated on a real-time platform.

As it has been shown in the previous sections, Stages 3 (Current Injection) and 4 (Voltage Rise) represent critical stresses within the circuit breaker – in particular, on the vacuum interrupter. However, for the purposes of system-level simulations, they are relatively redundant. For system-level simulations, the circuit breaker model is typically ideal – i.e. it breaks current on demand – and it does not include statistical or detailed physical representation of arc phenomena. This means that the additional data given in Stages 3 and 4 is not utilised within system-level analysis. Moreover, these detailed phenomena are assessed separately during the design and optimisation phase of the circuit breaker, using EMTP-type software with the ability to use very-small time-steps.

Real-time Mechanical Circuit Breaker Model (or RTDS Model)

The proposed RTDS model is a simplification of the standard model, and it is shown in Figure 5. The current injection circuit is reduced, with the making switch and inductance being removed. The capacitor is also not pre-charged. Interruption capability is determined by setting the chopping current of the main interrupter, S_1 (e.g. for 16 kA interruption capability, the chopping current is set to 16 kA).

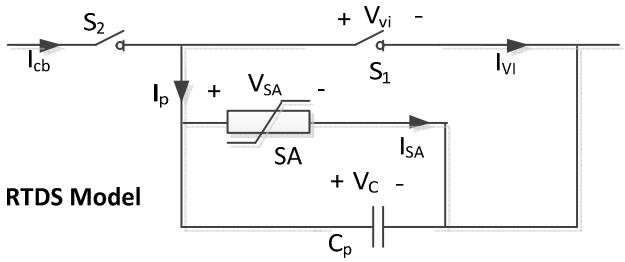

Figure 5: Real-time Mechanical Circuit Breaker Model, implemented in both small and normal time-step..

As shown in Figure 3 the rate-of rise of voltage across the interrupter is related to the initial voltage at the point where current commutates from the main interrupter to the capacitor branch. In the case of the RTDS model, the capacitor voltage starts at 0 V. Therefore, it rises to the clamping voltage slightly faster than in the case the full model is used, and it produces a negative di_{cb}/dt slightly earlier. This can result in discrepancies in energy, peak voltage and current.

Small time-step RTDS Model Simulation Results

RTDS has the facility for both small and normal time-step models. In general, because of fast transients, VSC systems are typically simulated in real time simulation platforms using small time-step models. A small time-step model of the mechanical breaker has been developed. Figure 6 shows simulation results comparing the small time-step RTDS model with a standard model (developed in EMPT-based software, allowing fine time-steps to be used). The results show that main system-level properties – current, energy, and voltage – are replicated accurately in the RTDS model.

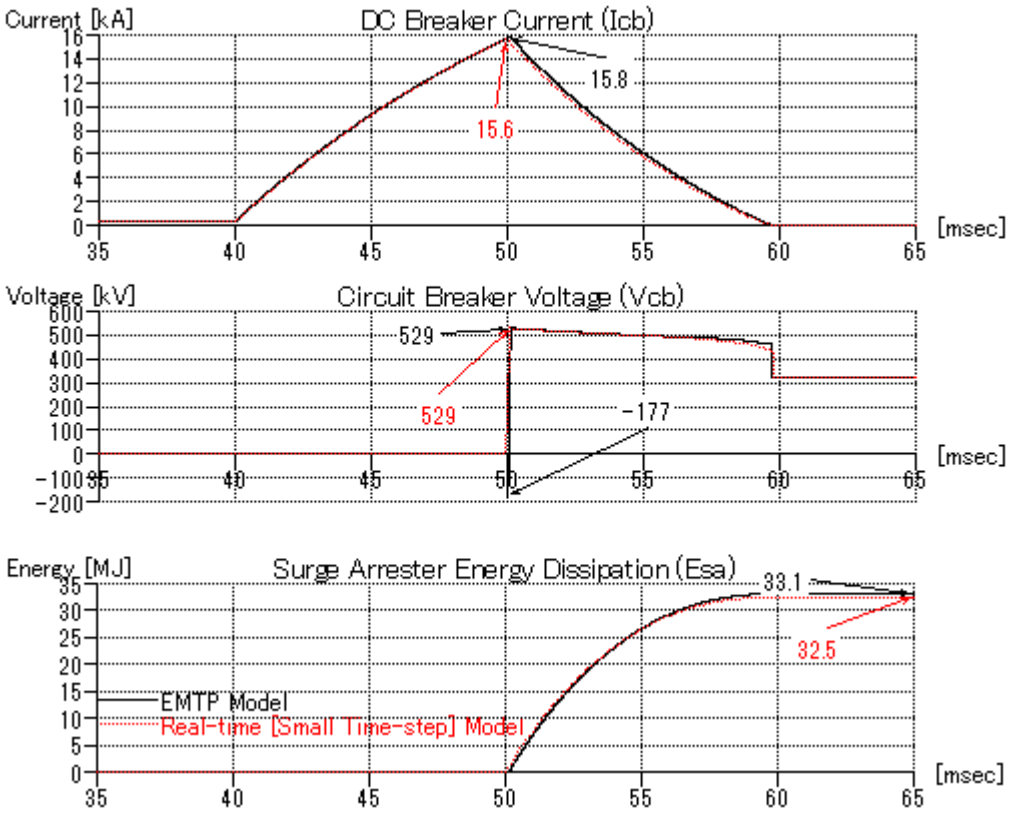

Figure 6: Comparison of Mechanical DC Circuit Breaker PSCAD and Small Time-step RTDS Model

Normal Time-step RTDS Model Simulation Results

It is conceivable that in large, future real-time simulations, there may be cases where circuit breakers are separated from converter stations via long lengths of cable. For this purpose, long time-step models may be feasible and indeed desirable to reduce computational burden. A normal time-step model of the breaker has also been implemented for this situation.

Figure 7 shows simulation results comparing the normal time-step model and the EMPT model. In the case of a normal time-step model, there are a significantly reduced number of samplings for a given period. As the rate-of-rise of voltage in Stage 4 rise is very rapid, current commutation from capacitor to surge arrester can lead to numerical errors, which typically results in erroneous voltage spikes as shown in the Figure 7.

By increasing the capacitance, the rate-of-rise of voltage is decreased significantly, which can introduce errors in peak current and voltage. However, it should be noted that this results in additional energy is also transferred to the capacitance, which would have otherwise have been transferred to the surge arrester. Therefore, the change in capacitance must be chosen with care.

Conclusion

Key phenomena of the mechanical circuit breaker have been described, and those of interest have been highlighted. Both small and normal time-step real-time models of the breaker have been developed to enable system studies. These models were demonstrated to be able to replicate key phenomena required for system studies, such as TIV, current and surge arrester energy within a reasonable accuracy. It has been shown that some information is lost in the RTDS model (namely, the initial, negative TIV). It has been demonstrated that the margin of error introduced by ignoring this region is small, and the model valid for the range of simulations to be performed.

A long time-step model has also been demonstrated, where increased capacitance has been used to slow the rate-of-rise of voltage. This results in an increased margin of error, compared to the small time-step model. However, it significantly increases the ability to simulate very large networks in the future.

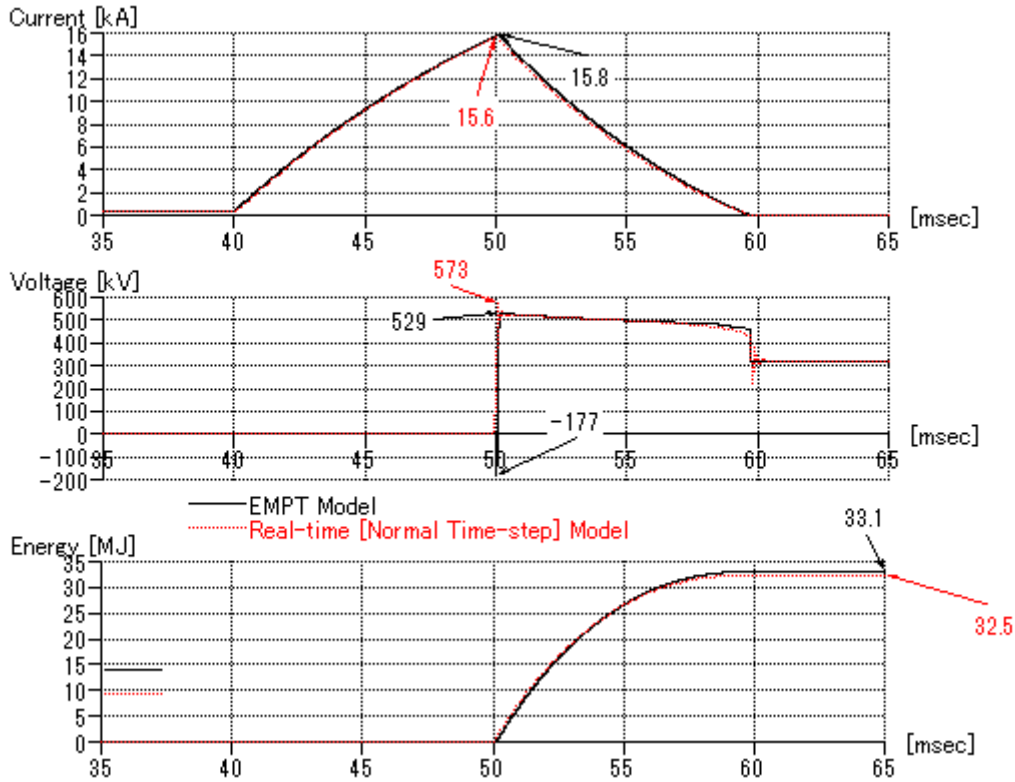

Figure 7: Comparison of Mechanical DC Circuit Breaker PSCAD and Normal Time-step RTDS models

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BIBLIOGRAPHY

[1] Lin, Weixing, et al. "Modelling of high power mechanical DC circuit breaker." Power and Energy Engineering Conference (APPEEC), 2015 IEEE PES Asia-Pacific. IEEE, 2015.
[2] Lee, A., et al. "The development of a HVDC SF6 breaker." IEEE transactions on power apparatus and systems 10 (1985): 2721-2729.
[3] Ito, H et al. "Instability of DC arc in SF6 circuit breaker" IEEE transactions on power delivery 1997.
[4] Greenwood, A. N., and T. H. Lee. "Theory and application of the commutation principle for HVDC circuit breakers." IEEE Transactions on Power Apparatus and Systems 4 (1972).
[5] Tokoyoda, S., et al. "Interruption characteristics of vacuum circuit breaker and the application to DCCB." (2017): 29-5.
[6] Tokoyoda, S., et al. "High frequency interruption characteristics of VCB and its application to high voltage DC circuit breaker." Electric Power Equipment–Switching Technology (ICEPE-ST), 2015 3rd International Conference on. IEEE, 2015.