

Fault Current Control Methods for Multi-Terminal DC Systems based on Fault Blocking Converters

P. Ruffing*, C. Brantl*, C. Petino*, A. Schnettler*

*Institute for High Voltage Technology, RWTH Aachen University, Schinkelstr. 2, 52056 Aachen, Germany
ruffing@ifht.rwth-aachen.de

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Abstract

Within the framework of modernisation of the European electricity grid, multi-terminal HVDC offshore grids shall be integrated in future transmission systems. An essential aspect of multi-terminal HVDC systems is fast and selective DC-side fault handling and the separation of faulty lines. This paper investigates the applicability of different control methods relying on full-bridge based converters in combination with high speed switches for a fast and selective separation of faulty line segments in a multi-terminal HVDC cable system in symmetrical monopole configuration. It is shown, that the proposed line current control method can significantly reduce the separation time of a faulty line compared to standard fault control methods. The analysis is based on simulations in PSCAD|EMTDC™ with a converter model based on the CIGRÉ WG B4.57, which is enhanced for the use of full-bridge converters with fault current control schemes.

1. Introduction

The world's increasing integration of renewable energy sources into existing energy supply systems leads to enlarged distances between production and consumption of the electrical energy. Voltage Source Conversion (VSC) based High Voltage Direct Current (HVDC) networks enable flexible and efficient bulk power transmission over long distances. Thus, multi-terminal HVDC onshore and offshore grids will be used for the expansion of future transmission systems. A critical aspect for the integration of these systems is the DC-side fault handling. To minimise the downtime of DC networks, which might transmit several gigawatts of electrical power, while protecting the expensive converter stations, fault currents in DC systems must be interrupted quickly and reliably. In addition, the faulty line must be isolated from the grid as fast as possible. Several concepts have been proposed to comply with these requirements of fast fault separation in HVDC grids, most relying on either DC circuit breakers or fault-blocking converters.

This paper investigates a concept based on converters with DC fault current blocking and controlling capability – in this case full-bridge based modular multilevel converters (FB-MMC).

Protection strategies for MTDC systems based on converters with DC fault-blocking capability and disconnectors have been elaborated in the past [1]. After fault detection, all converters are blocked and the grid discharges via the fault. Using a fault localisation method, the switches, which separate the faulty line segment from the healthy network, are identified. The isolation of the faulty line can be realised with fast disconnectors with residual current breaking capability, so called high speed switches (HSS) [1]. Once the current through the HSSs is reduced and stays within a predefined current threshold (defined by the current interruption capability of the HSS) the selected HSSs open. After the line is successfully isolated from the grid, the converters deblock and the grid restoration takes place. Nevertheless, the methods neglect the ability of FB-MMCs to control the DC voltage and the fault current. To enhance the speed of the protection concept, the fault current can be actively controlled by FB-MMCs [2, 3, 4]. Thereby, a faster discharge of the grid capacity is achieved and consequently the current through the HSS can be reduced below its interruption threshold faster. An additional advantage of this approach is the continuous supply of ancillary services to the connected AC systems as no blocking occurs.

Within this paper, a comparison of converter blocking and fault current control concepts concerning the isolation time of faulty lines is conducted and novel fault control methods are proposed. The investigations are based on a minimal meshed MTDC offshore network used within the European Horizon 2020 project PROMOTioN. The network and the location of the HSSs are illustrated in Figure 1. The simulations are carried out in the software PSCAD|EMTDC™ with a converter model based on the CIGRÉ WG B4.57, which was modified within the PROMOTioN project.

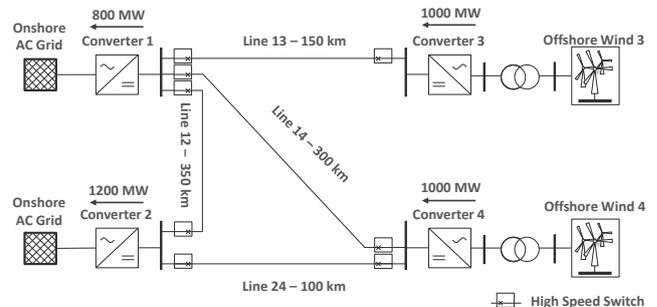


Figure 1: Minimally meshed MVDC network used in the PROMOTioN project

2. Technical Considerations

2.1. Fault Handling Requirements for MTDC Systems

Future multi-terminal HVDC systems will have several requirements to fulfil during fault operation. Among others a requirement is that the DC protection system has to ensure that the system's components are not stressed beyond their limits. This includes the limitation of the voltage stress on cables and converters. Moreover, it has to be ensured, that the power electronic devices remain in their safe operating area [5]. To guarantee a stable operation of the AC grids surrounding the DC system, the impact of DC faults on these systems shall be minimised and a high availability of the DC system is required. Therefore, HVDC grids necessitate fast, selective, reliable and robust protection strategies. DC line faults must be cleared selectively to reduce the loss of power transmission capacity [5].

2.2. Converter technology

Nowadays, voltage source converters for HVDC grids are half-bridge (HB) or full-bridge (FB) Modular Multilevel Converters (MMC). An MMC consists of six arms, which comprise a serial connection of n_{SM} identical submodules (SM) and a reactor L_{Arm} , as depicted in Figure 2. Within this contribution the converter is operated as symmetrical monopole, with a positive (P) and negative (N) pole.

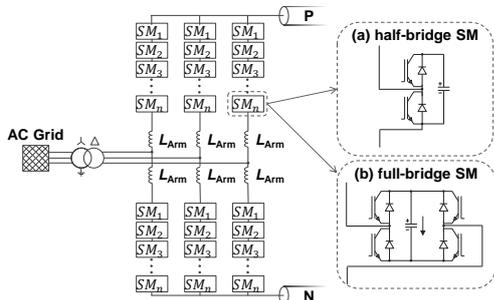


Figure 2: Schematic design of a monopolar MMC station with (a) half-bridge and (b) full-bridge submodules

Since half-bridge submodules consist of two IGBTs, they are not able to block negative voltages and interrupt DC fault currents. Therefore, blocked half-bridge based converters behave like a diode rectifier during DC faults. To fulfil the requirements defined in section 2.1, half-bridge based converters can be operated in combination with DC circuit breakers or current limiting devices. On the contrary, full-bridge submodules consist of four IGBTs, as shown in Figure 2. Thus, the submodules' capacitors can be inserted with negative polarity and the converter can interrupt fault currents. Moreover, the DC pole voltage of the converter can be controlled over the full range of $\pm V_{DC,max}$ [6]. This is utilised in fault control concepts (cf. section 2.4).

2.3. Converter Control

The converter is controlled with a cascaded vector control, which has a good stability and dynamic performance [7]. The control is separated in three functional levels: the lower, upper

and dispatch control level. An overview of the control structure is presented in Figure 3.

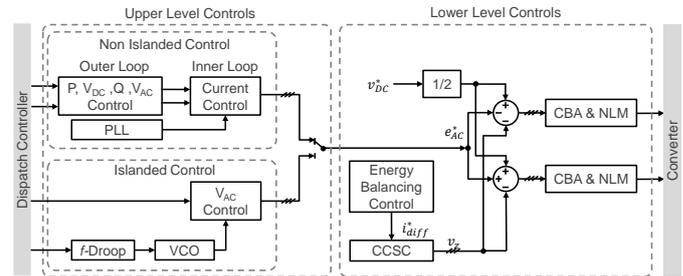


Figure 3: Control Scheme

Dispatch Control

The dispatch or station controller defines the operating set points (P , V_{DC} , Q , V_{AC}) and the control modes of a converter (e.g. islanded or non-islanded) to fulfil the requirements of the AC and DC systems [7]. Moreover, the ramps rates of droop functions are defined in this level. The outputs of the dispatch control are mainly forwarded to the outer loop of the upper level controls. The orders for the dispatch control come from the system operator [7].

Upper Level Control

Based on the orders from the dispatch control, the upper level control generates the reference AC voltage of the converter. If the converter is connected to an AC system with active synchronous generation or an offshore AC system with WPPs as feeders, the upper level control is set to *non-islanded mode* or *islanded mode* respectively. If the control operates in *non-islanded mode*, it utilises a decoupled current vector control as an inner loop and regulates the AC current's direct (d) and quadrature (q) component. The AC systems phase angle is tracked via a *phase locked loop* (PLL). The reference currents are generated by outer loop controllers for P , V_{DC} , Q and V_{AC} [7]. If the control operates in *islanded mode*, the d-component of the converter's AC voltage is directly controlled via a V_{AC} controller. The angle reference is generated by an oscillator controlling the system frequency [7]. To reduce the maximum arm voltage the reference arm voltages are lowered by a third harmonic injection [7].

Lower Level Control

For a stable operation the average AC and DC power have to be equal and voltages of the SM capacitors have to be constant over a period of the fundamental frequency f_{AC} . Therefore, the energy differences between the phases and between the upper and lower arms are minimised using an *energy balancing control* [8]. The energy balancing output is used as input of the *circulating current suppression control* (CCSC) [7]. The reference arm voltages are generated by a summation of the upper level voltage e_{AC}^* , the CCSC voltage v_Z^* and the reference DC voltage v_{DC}^* (cf. Figure 3). Based on the reference voltage, firing signals are generated for the power electronic switches by a *nearest level modulation* (NLM) method [9]. To guarantee an even capacitor voltage distribution across the converter arms a *capacitor balancing algorithm* (CBA) is used [7].

Converter Protection

To protect the converter's power electronic devices against overcurrents and thermal overload an *arm overcurrent protection* triggers the blocking of the SMs. The protection threshold is set to $I_{OCP} = 0.9$ p.u. of the repetitive peak current I_{RRM} of the IGBTs (cf. Table 1).

2.4. DC Fault handling with full-bridge converters

Within this section different DC fault handling methods for converter with DC fault blocking and controlling capability (usually FB-MMC) are presented. The methods *Submodule Blocking*, *Terminal Current Zero Control* and *Terminal Voltage Zero Control* are presented in recent literature [2, 3, 4]. The methods *Terminal Current & Voltage Zero Control*, *Line Current Zero Control* and *Terminal Voltage & Line Current Zero Control* are novel extensions of the previous methods developed within this paper.

(a) Submodule Blocking

The most basic option is the blocking of all submodules, once a fault is detected at a station. A major drawback of the concept is the loss of reactive power control to the AC system.

Since full-bridge based MMCs can control their DC-side output voltage v_{DC} freely over the full range of $\pm V_{DC,max}$, DC fault currents and the voltages at the terminals can be controlled by the converter. Within this publication, several fault current control methods are analysed regarding the opening times of the HSSs, which have to separate the faulty line, as shown in Figure 4. To stop the infeed of active power to the converter and the fault, the d-component of the outer loop is controlled to $P^* = 0$ by the *P-Control*. A positive aspect of controlling the DC fault is that the converter is continuously connected to the AC grid and thus can continuously control reactive power.

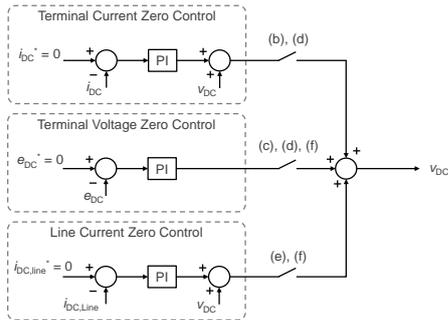


Figure 4: Fault Control

(b) Terminal Current Zero Control

The most common DC fault control technique is the zero current control at the DC terminals. In case of a DC fault, the DC terminal current i_{DC}^* is controlled to zero via a PI controller by adjusting the DC terminal voltage [2, 3, 4].

(c) Terminal Voltage Zero Control

In case of a DC fault, the DC reference voltage v_{DC}^* is controlled to zero via a PI controller to discharge the grid capacity as fast as possible [3].

(d) Terminal Current & Voltage Zero Control

A novel control strategy is the combination of both current and voltage zero control. Several multi-variable control concepts are possible. Within this paper, a simple parallel control approach of (b) and (c) is proposed.

(e) Line Current Zero Control

Since the currents through the line ends of a faulty line determine if the corresponding HSSs are able to interrupt and thereby clear the fault, this method uses exactly these currents as control input. After fault detection, the terminal current is used as input for the fault control (b). If a protection relay identifies, that a faulty line is directly connected to its busbar, its line current is used as input for the fault control. If no faulty line is connected to the busbar, the control remains in terminal current zero control.

(f) Terminal Voltage & Line Current Zero Control

Finally, a combination of the two previous methods is proposed within this paper. After fault detection method (d) is used to control the fault current. If the localisation method identifies a certain line, the terminal current control method (b) is switched to the line current control method (e).

After the fault is cleared, the converter controls are set back to their pre-fault values and the pre-fault control operation is resumed.

2.5. Line Fault Discrimination

DC fault discrimination is split into two main parts, fault detection and fault localisation. To ensure fast and robust detection of DC line faults, single ended methods, which do not require communication, are used within this paper. Thus, voltage and current values are evaluated at each end of the transmission line to detect DC line faults. As a transient protection method, a combination of voltage and current derivative protection is used. Both overcurrent and undervoltage relays are applied as backup protection [10]. For signal processing a time delay of $\Delta t_{det} = 0.5$ ms is assumed within the publication. Several methods for fault localisation are discussed in literature. Within this paper, the simple approach of a *longitudinal DC line current differential* protection is used for fault localisation. This method is based on the comparison of currents at each line end [10]. Thus, this method does not require series inductors at the line ends. However, the comparison of the currents requires communication. The communication velocity is set to $v_{com} = 150$ km/ms [1].

2.6. Fault Isolation

An identified faulty line needs to be separated fast and selectively from the healthy part of the transmission system. After the fault current at a selected line end is reduced to values close to zero, the corresponding HSS needs to open, interrupt a residual current and withstand a transient interruption voltage. Moreover, the HSSs need to withstand the rated DC voltage once the voltage in the healthy network is resorted. To

interrupt relatively low currents up to $I_{thres} = 100$ A vacuum interrupters with a radial axially symmetric magnetic field might be sufficient [11]. For the interruption of higher DC currents AC circuit breakers with artificial transition of the current through zero, so called *resonant circuit breakers* can be used. The current interruption capability and the speed of interruption can be adjusted by the parametrisation of the breaker's resonant circuit [11].

3. Fault Clearing Strategy

In this section, the fault clearing sequence for each individual converter is presented and visualised in Figure 5. After the occurrence of a DC line fault at the time t_F , travelling waves propagate through the system. The protection relay detects the fault at t_{Det} and triggers the fault limitation process of the converter (blocking or fault control, cf. section 2.4). Moreover, the fault detection triggers the fault localisation process. If a fault is localised on a line connected to the converters busbar, the relay selects the HSS corresponding to the faulty line. The HSS opens after the fault current flowing through the switch decays and remains within the specified current interruption threshold I_{Thres} of the HSS. Before the converter starts the grid recovery process, it has to be ensured that the HSS at the other line end is open as well. This can either be achieved via communication or a predefined safety time, in which fault clearing processes should be finished. If no fault is localised on a line connected to the converter's busbar the converter remains in the fault limitation mode until the fault is cleared by the related HSS. The grid recovery process is also triggered either by an external communication signal or a predefined safety time.

Since the focus of this work is the investigation of the effect of different fault current control methods on the decay of fault currents through HSSs, which separate the faulty line, grid restoration is not considered.

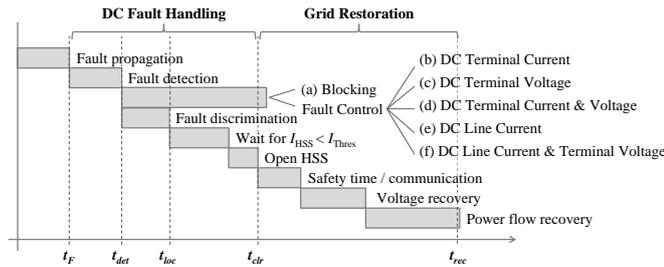


Figure 5: Fault clearing strategy

4. Investigated Transmission System

The influence of the fault clearing strategy for FB-MMCs is tested in a minimally meshed MTDC cable system with four converter terminals, as shown in Figure 1. Based on state-of-the-art DC offshore links, the test system is setup in symmetrical monopole configuration with high impedance grounding on the AC side of the converters. Two converters are connected to AC grids onshore, which are not connected to each other. The other two converters are connected to offshore AC grids fed by aggregated wind power plants (WPP) based on type 4 wind turbines. The model for the WPP is based on

the published standard IEC 61400-27-1 and is adjusted for DC fault stations [12]. Each WPP has a rated power of $P_{WPP,r} = 1200$ MW and is operated at $P_{WPP} = 1000$ MW. The onshore converter 1 is operated in V_{DC} -Control mode with $V_{C1}^* = 320$ kV and converter 2 is operated in P -Control mode with a target of $P_{C2} = 1200$ MW. Both onshore converters are operated in Q -Control with a target of $Q_{C1} = Q_{C2} = 400$ MVar.

The investigated fault locations are shown in Figure 6. For every fault location two types of faults are considered within this paper: P-to-ground (PG) and P-to-N-to-Ground (PNG) faults. The fault resistance between pole and ground is set to $R_{F,G} = 0.5 \Omega$ and the fault resistance between two poles is set to $R_{F,PN} = 0.1$ m Ω .

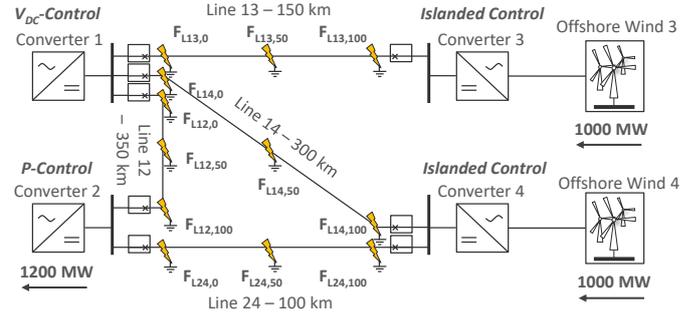


Figure 6: MTDC network: fault locations

4.1. Transmission Line Modelling

All transient simulations are carried out in PSCAD|EMTDC™ with a solution time step of $\Delta t = 10 \mu s$. The transmission lines are modelled using the *Frequency Dependent Line Model*. The cables are parametrised according to standard 320 kV XLPE submarine cables with metallic screen. The cables' metallic screens and the sheaths are grounded via a ground resistance of $R_{sheath} = 0.5 \Omega$ at each line end. Moreover, surge arresters with a nominal voltage of $v_{SA,r} = 560$ kV ($i_{SA} = 1$ kA) are placed at each line end and at the converter terminal (cf. Figure 6). In contrast to systems with DC circuit breakers, no line inductances are needed for fault current limitation and selectivity. The HSSs are modelled as ideal switches with a defined current chopping capability of I_{Thres} in parallel to a surge arrester with a rated voltage of $v_{SA,r} = 385$ kV ($i_{SA} = 1$ kA). The busbar configuration is shown in Figure 7.

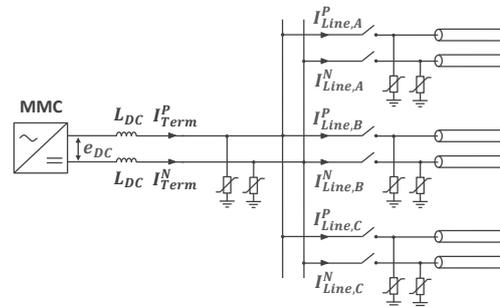


Figure 7: Busbar configuration

4.2. Converter Modelling

The converters are modelled as *Detailed Equivalent Circuit*

Model (Type 4). Since the individual submodule switching states and capacitor voltages of the converter are represented, the model is well suited for transient DC fault studies [7]. The converter station ratings are depicted in Table 1. The DC inductance is set to $L_{DC} = 25$ mH. This value is chosen in such a way that the internal converter overcurrent protection does not trigger in any fault scenario, if a fault detection delay of $\Delta t_{det} = 1$ ms is assumed.

Converter Station Parameter		Setting
Rated power	S_r	1265 MVA
Rated active power	P_r	1200 MW
Rated DC pole voltage	$V_{dc,r}$	± 320 kV
Rated DC current	$I_{dc,r}$	1.875 kA
Rated AC voltage onshore	$V_{ac,on}$	400 kV
Rated AC voltage offshore	$V_{ac,off}$	155 kV
Arm inductance	L_S	50 mH
Number of submodules per arm	n_{sm}	350
Rated submodule voltage	$V_{sm,r}$	1.9 kV
Submodule Capacitor	C_{sm}	8.8 mF
IGBT repetitive peak current	I_{RRM}	3.0 kA
Output converter inductance	L_S	25 mH

Table 1: Converter setting

5. Simulation results

Within this section the effects of the fault handling methods on the current through the HSSs, which have to separate a faulty line are analysed. Figure 8 depicts the current flowing through the HSSs on the faulty line, which have to separate the faulty line, for all fault handling methods presented in section 2.4, the fault types presented in section 4.1 and all fault locations

shown in Figure 6. In Figure 9 the maximum of the absolute current values of each method are presented for better comparison. After a fault occurs, it is successfully detected and localised in all cases. First, a transient surge current up to $I_{HSS,max} = 26$ kA occurs, which is caused by the discharge of the grid's cable capacitance into the fault. Afterwards, all methods are capable of limiting the fault current. It can be observed that *Submodule Blocking* (a) and *Terminal Current Zero Control* (b) have a similar effect on the DC currents flowing through the relevant HSSs. After the transient surge current, the HSS currents can be limited to values below $I_{HSS,Thres} = 100$ A, which is chosen due to the current interruption threshold of vacuum interrupters (c.f. section 2.6), in less than $\Delta t_{HSS,(a)} = 129$ ms and $\Delta t_{HSS,(b)} = 138$ ms in all scenarios. Nevertheless, controlling the terminal current to zero method (b) has the major advantage of continuous converter operation and therefore continuous reactive power support. The results for the *Terminal Voltage Zero Control* method (c) are presented in Figure 8 (c). Even though the fault current can be limited and the DC voltage is quickly controlled to zero, the time constants for current decaying to zero are relative high compared to the methods (a) and (b). Thus, it is concluded, that the purely voltage based methods is not suited for the proposed protection system. Therefore, method (c) is not considered in the analysis of the maximum current values in Figure 9. The combination of *Terminal Voltage & Current Zero Control* is depicted in Figure 8 (d). The transient behaviour after fault occurrence is similar to method (a) and (b). However, method (d) limits the fault currents to values close to zero faster than (a) and (b), due to the active discharge of the grid ($I_{HSS} < 100$ A in $\Delta t_{HSS,(d)} = 118$ ms). It is shown that the *Line Current Zero Control* (e) also can reduce the decay time of the fault current compared to method (a) and (b), with $I_{HSS} < 100$ A in $\Delta t_{HSS,(e)} = 88$ ms. Thus, the direct control of the relevant lines has a positive effect on the current to zero limitation as well.

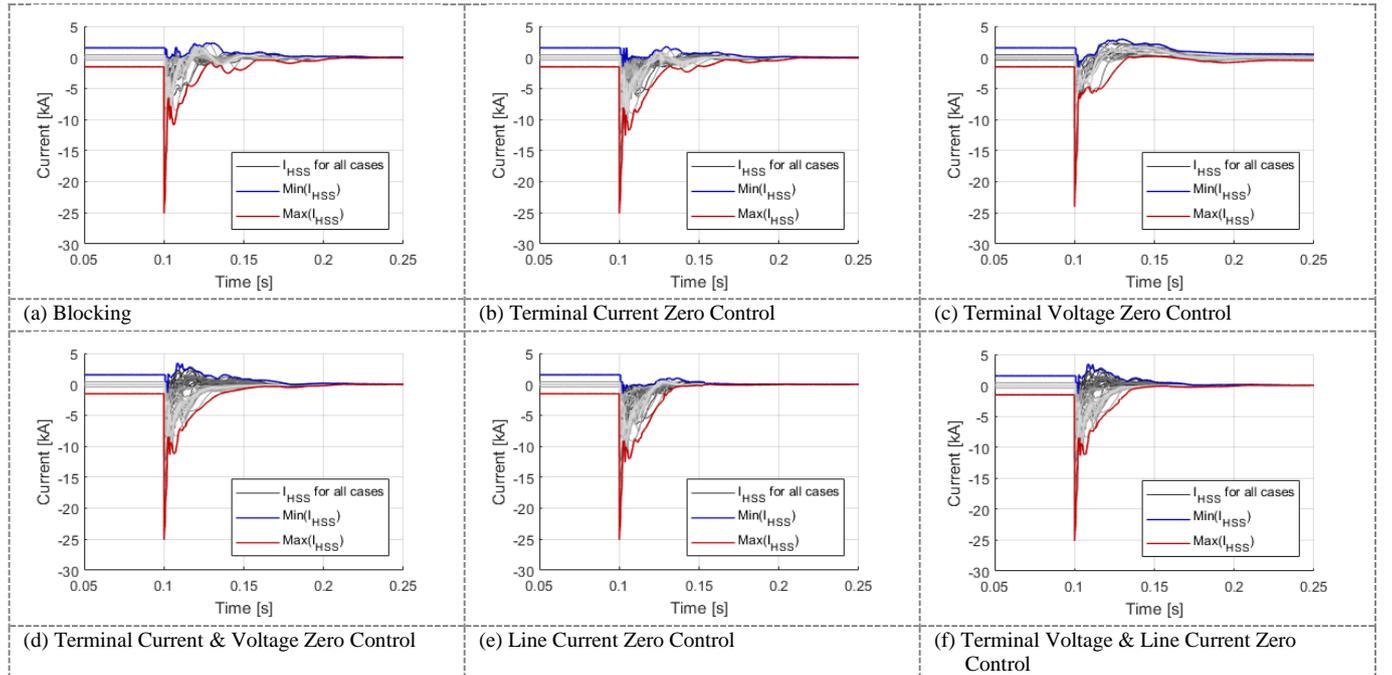


Figure 8: Current through relevant HSSs for all 24 test cases and all fault handling methods

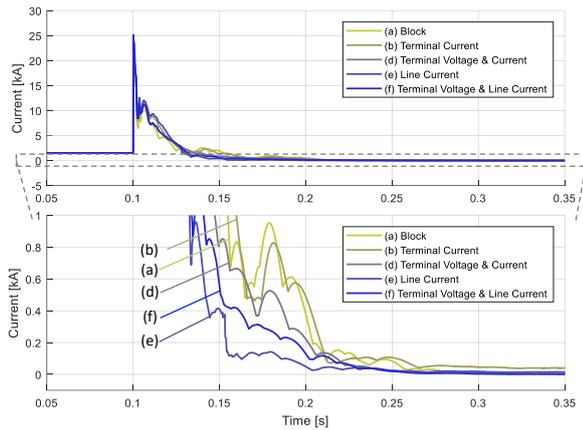


Figure 9: Maximum of the absolute current values through the relevant HSSs for all fault handling methods

The combination of *Terminal Voltage & Line Current Zero Control* (f) can also enhance the limitation of the fault currents flow through the affected HSSs. In the worst case situation ($I_{F13,0}$) the HSS current can be limited to $I_{HSS} < 100$ A in $\Delta t_{HSS,(f)} = 114$ ms. Nevertheless, if a voltage control is not needed, the *Line Current Zero Control* (e) shows better results within this test network.

6. Summary and Conclusion

Within this paper different fault handling methods for FB-MMC based multi-terminal HVDC cable systems in symmetrical monopole configuration are analysed. In such DC systems the separation of faulty lines is carried out by *High Speed Switches* instead of fast *DC circuit breakers*, which are normally used in combination with HB-MMCs. Focus of the investigation are the effects of the fault handling methods on the currents flowing through HSSs, since they will determine the required residual current interruption capability of the switches. It is shown that converter blocking and controlling the DC voltage can be used to limit the HSS currents to values close to zero. Thus, both methods are suitable for a selective line separation. In general, fault current control methods have the major advantage over blocking concepts that ancillary services such as reactive power control are not interrupted during fault operation. Moreover, it is shown that advanced control concepts, like the proposed *Line Current Zero Control* can significantly reduce the time until the current flowing through the relevant HSS is limited to a certain current interruption threshold. Therefore, the separation time of faulty line segments can be reduced significantly compared to converter blocking and proposed control concepts. Depending on the required fault separation and recovery time of the DC system, the current interruption capability of the HSSs can be defined and the switch can be designed accordingly. The influence of the HSS design on line separation has to be investigated in further contributions.

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