Test Circuits for HVDC Circuit Breakers

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***Abstract*—High voltage direct current circuit breakers (HVDC CBs) are necessary for reliable and safe operation of future multi-terminal meshed HVDC grids. So far no commercially mature products of such equipment exist. A few industrial concepts as a result of advances in power electronics have been proposed and prototypes have been built. However, performances of these concepts have never been demonstrated under realistic operation condition. Since these tests require construction of high power DC sources incurring significant investment costs, alternative test circuits providing equivalent stresses must be considered. In this paper various test methods and circuits used for testing HVDC CBs are investigated and their performance is evaluated against the stresses in a conceptual future HVDC grid. A novel method of testing an HVDC CB using existing installations in a high power ac test laboratory is proposed and its prospective fault current and voltage is experimentally demonstrated. It is concluded that adequate test circuits need to maintain the supply voltage not only up to the current zero in the main interrupter unit of the HVDC CB, but also during the entire energy dissipation phase of the interruption process.**

***Index Terms*—HVDC circuit breaker, power system transients, PSCAD, test circuit, test facilities, testing.**

I. Introduction

MULTI-TERMINAL, meshed high voltage direct current (MTDC) transmission is considered to be a viable solution for large scale integration of renewable energy sources such as offshore wind farms [1], [2]. For such application voltage source converter (VSC) based HVDC technology is superior to the traditional line commutated current source converter (LCC) because of its bi-directional and flexible power flow control, smaller footprint, ability to supply weak or even passive networks [3]. However, a few major technical challenges need to be addressed before such systems are realized [4], [5]. One of the main challenges is the lack of fast, low loss and reliable HVDC circuit breakers (CB) capable of clearing DC faults [6]. Because of the absence of current zero in DC systems, a HVDC CB need to create artificial current zero in its interrupter unit(s) while absorbing the magnetic energy stored in the system inductance.

Apart from two recently commissioned radial, MTDC grids [7], [8], so far all VSC HVDC projects are point-to-point interconnections. Although there is a plan to upgrade these grids with DC side protection employing HVDC CBs, at the moment of writing this paper, DC contingencies are handled via ac side protection in a similar way as in point-to-point interconnections [9]. This results in a temporary de-energization of the entire DC grid in case a DC fault is detected. However, as the size of DC grid increases, this technique becomes unacceptable. A protection system that isolates the faulty section without the collapse of the entire DC network is essential; this requires fast acting HVDC CBs.

Ever since the inception of HVDC transmission concept in the 50's, there has always been a desire to build MTDC grid; and hence, HVDC CBs have been the subject of significant research. Notably, in the 70's up to the late 90's considerable research and development has been conducted [10]-[29]. AC CBs with additional circuits for current zero creation and energy absorption have been thoroughly explored [10]-[13]. In order to enhance the performance of HVDC CBs various interruption media either as standalone or hybrid schemes consisting of series and parallel combination of CBs with different interruption media, have been experimentally investigated [13]-[18]. At the time the HVDC transmission technology under consideration was LCC HVDC in which the rate of rise and magnitude of fault current is not as critical as in the recently preferred technology for multi-terminal interconnection, the VSC HVDC technology [29]. In the former case the system fault current can be limited with control of firing angles of thyristor valves [10]. Besides, the system has inherent DC side reactors which significantly reduce the rate of rise of fault current. For this reason, the main focus of HVDC CB research was on the mechanism of current zero creation across the interruption unit(s) while the time to interrupt the fault current could be up to few hundred milliseconds.

The requirements of the test circuits used for the development of those breakers were also defined accordingly. For instance, low frequency charged capacitor-inductor (C-L) circuits with oscillation frequency in the range of 1-5 Hz were mostly used. Besides, a short-circuit generator running at frequency up to 10 Hz was used for testing the performance of the HVDC CBs [12], [18]. Moreover, a reactor with high quality factor charged by a low voltage battery also constitutes one of the test circuits used in the development of DC CBs [21]. In all of these test circuits the main objective is achieving (quasi-) DC current of required magnitude for a relatively longer duration, while the rate of rise of current and more importantly the magnitude of the driving voltage were not taken into account.

Nevertheless, issues such as sufficient energy in the test circuit have been identified as important part of the test procedure. With this regard two test procedures, one for current interruption capability and the other for energy

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absorption capability have been suggested [10] and separate tests have been carried out. For instance, a rectifier circuit along with a DC reactor is connected to a short-circuit generator to produce a DC current that can be used for testing current interruption capability [29]. In some cases, because of absence of test facilities with sufficient DC power, there are occasions where the HVDC CBs are tested in the field [22], [25], [30], but this results in the most expensive test and is not desirable from power system operation point view. Synthetic test circuits adopted from ac CB tests were also used for testing HVDC CBs [10], [19], [31], [32].

With the advent of VSC HVDC technology, new challenges arose. Especially, the future MTDC grids are likely to be supplied from modular multi-level converters (MMC) based on half bridge submodules. However, in such a system fault current cannot be controlled because of the freewheeling diodes associated with each IGBT in the submodules. Besides, due to the capacitive behavior of HVDC cables and overall low DC side impedance, the fault current rises rapidly to a large magnitude that can subsequently damage system components if not properly handled [33]. Thus, in a MTDC grid extremely fast HVDC CBs which can selectively clear the DC side fault before it propagates to the healthy part of the system are necessary.

In the past few years, a few industrial concepts as a result of advances in power electronics have been proposed and in some cases prototypes have been built [9], [34], [35]. Besides, the application of mechanical HVDC CBs based on active current injection principle has revived because of the developments in fast actuators, for instance, based on electromagnetic drives [36]-[39] and of high-voltage vacuum interrupters. As part of research and development at the respective laboratories, these industrial concepts have been tested using various test circuits primarily for their speed and maximum current breaking capability. The real performance of these concepts under expected MTDC grid operation condition is yet to be conducted.

Mostly, charged capacitor test circuits along with reactors, have been used [9], [34]. In addition, in order to take into account the load current just before the fault, synthetic test circuits built from superposition of two charged capacitor-inductor circuits are used [35]. The main challenge with the use of charged capacitor-inductor test circuit is that large values of capacitor must be used in order to produce sufficient stress at rated values. For instance, in order to tackle this challenge, a capacitor is charged to a voltage higher than the rated voltage for which the breaker is designed [40]. AC short-circuit generator at power frequency (50 Hz) has been used for testing the recently developed active current injection type HVDC CBs [36], [37].

In all these cases a test is deemed successful if the breaker interrupts the ac current at its peak well before its natural zero crossing. However, this method lacks sufficient voltage stress, as in service, during the energy absorption phase of the interruption process.

The optimal test circuit is indeed a full-scale converter connected to short-circuit generators having sufficient short circuit power. However, this incurs significant investment to build one at a test facility. Given the fact that no commercially mature products of such devices are available yet in the market, it is reasonable to look for other but equivalent alternatives.

The main aim of this paper is, therefore, the use of an existing high-power ac test facility to develop adequate test circuit for HVDC CBs. The paper describes and compares, via simulation, various test circuits that can potentially be considered for testing a HVDC CB. A method of using ac short-circuit generators with proper parameters is introduced. A simulation model of a HVDC CB is inserted in a low power-frequency test circuit that actually demonstrates experimentally the available test-capability with realistic parameters.

The remaining part of the paper is organized as follows. Section II describes the system model along with underlying assumptions for driving the requirements of a test circuit. A description of a generic model of an HVDC CB along with its operation principle is briefly provided in this section. In Section III a mathematical analysis of the current interruption process in a simplified DC system is presented. The candidate test circuits for HVDC CB are discussed in Section IV. The experimental result of the proposed test method using ac short-circuit generator is discussed along with the actual installation in a test laboratory. Simulation results of various test circuits are compared and discussed in Section V. Finally a conclusion based on the findings of the paper is drawn in Section VI.

II. Background and System Description

A test circuit must adequately represent the actual system in which a CB is to be installed. Thus, before designing a test circuit it is important to define the requirements of a test circuit based on practical system behavior under fault conditions. For this purpose, a DCS1 of CIGRÉ WG B4-57, a point-to-point symmetric monopole system with ±200 kV, VSC HVDC interconnection shown in Fig. 1, is used [41]. A half bridge 201 level MMC model of this system is developed in PSCAD based on detailed equivalent model (DEM) of a converter [42]. A few important modifications have been made to this system with the assumption of adequate DC side protection. First, in order not to lose controllability, a converter must not block, instead a fault current is entirely handled by HVDC CBs imbedded in the system (see Fig. 1). In the future MTDC grid with fast and reliable DC side protection, converter blocking may not be desirable in order not to disrupt power flow to the healthy part of the network.

Second, the model is originally developed with arm reactors dimensioned for achieving sufficient suppression of circulating current among converter legs while limiting the rate of rise of DC fault current within the blocking time (about 20 µs) of the converter IGBTs [43]. However, the state-of-the-art HVDC CB technologies are not purely power electronic and hence, require longer time for DC fault clearing. For this reason, further fault current suppression is necessary which can be achieved by additional DC side reactors (DCL) at each end of DC cables. Besides reducing the rate of rise of fault current, these reactors also limit the speed of voltage collapse at the converter terminal during fault. Several studies have been conducted on the need and impact of the DC side reactor in DC grids [37], [44]-[46]. In this paper DC current limiting

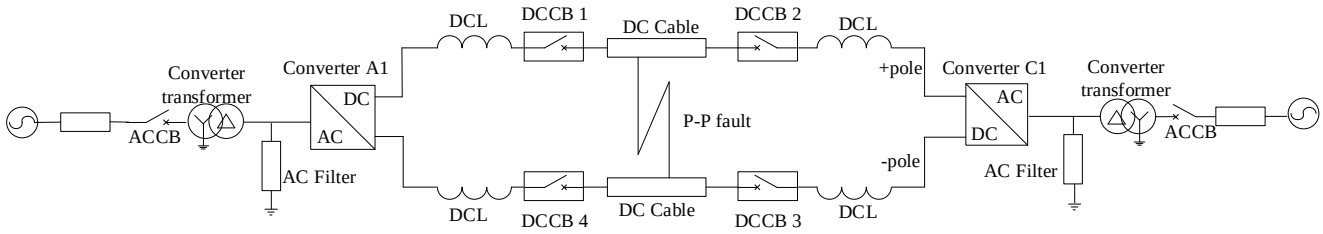

Fig. 1. System model CIGRÉ WG B4-57 (DCS1). Pole-to-pole fault in symmetric monopole configuration

reactors are dimensioned to limit the rate of rise of fault current to a maximum of 3 kA/ms

All fault clearing strategies by HVDC CBs that have been developed are based on creation of current zero through the nominal current path by employing several current paths as illustrated in Fig. 2.

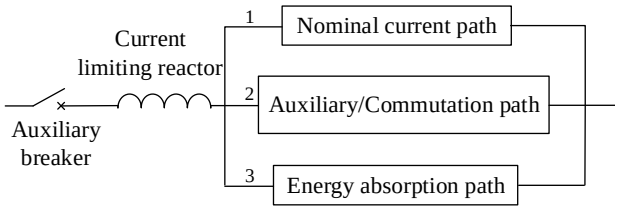

Fig. 2. Schematic block diagram of HVDC CB

Two principal candidate technologies for HVDC grid applications are considered.

A. *Active current injection type*

This consists of mechanical interrupter unit(s) in the nominal current path. The auxiliary branch consists of a pre-charged capacitor in series with a small inductor. During fault current breaking, the mechanical interrupter parts its contacts leading to arcing between the contacts. When the contact gap reaches sufficient dielectric distance to withstand the transient interruption voltage (TIV) at later stage, a counter current from a pre-charged capacitor is injected into an arcing gap to create current zero and interruption in the mechanical interrupter. From that instant on, the circuit current commutates first into the parallel L-C branch which causes the voltage to rise until a level is reached that will lead to commutation to a parallel metal oxide surge arrester (MOSA), in the energy absorption path in Fig. 2. The auxiliary breaker removes the residual current to protect the arrester banks against thermal overload [36], [37].

B. *Hybrid power electronic type*

This combines the positive features of mechanical switches with power electronic switches. The nominal current path consists of fast mechanical switch in series with few power electronic switches for bypassing the current into the parallel, main breaker unit (commutation path in Fig. 2) consisting of series connection of several power electronic switches. The main breaker (path 2) sustains the fault current until the fast mechanical disconnector reaches sufficient dielectric withstand to protect the power electronic switches in the nominal current path against subsequent overvoltage. Then, the main breaker interrupts the fault current and this is followed by a steep voltage rise across the breaker which is limited by MOSA serving the same purpose as in the active current injection type CB. A few hybrid power electronic HVDC CBs have been realized as a proto-type [9], [34], [35].

Since all of today's HVDC CB concepts basically apply the same principle of operation, the generic mode of operation of a HVDC CB is illustrated in Fig. 3 using the hybrid power electronic CB concept. For illustration purpose, a model of this CB is embedded in a point-to-point system as depicted in Fig. 1. A pole-to-pole fault is simulated on a line, 10 km away from the converter station C1.

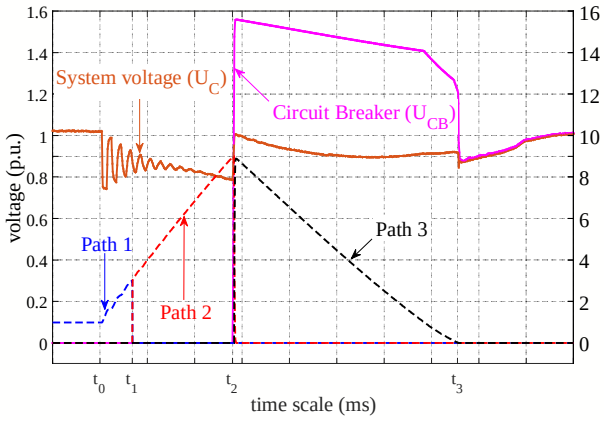

Fig. 3. Generic mode of operation of a hybrid power electronic HVDC CB. Dashed lines for current through various branches (right side scale), solid lines for voltage (left side scale). U_C is voltage at converter terminal; U_{CB} is voltage across circuit breaker terminals.

The fault current starts at t_0, then at t_1 current is interrupted in path 1 (see Fig. 3) and the fault current commutates into path 2 (the main breaker for hybrid type CB). Next, at t_2, the current is interrupted in path 2. This leads to a steep rise of voltage, until the surge arrester limits that voltage to about 1.5 p.u. as shown Fig. 3. This voltage is called transient interruption voltage (TIV). It is important to realize that, from this point on the system starts to recover, although the current in the fault location has not been interrupted yet. The faulted section is effectively separated from the healthy part of the system. From this point on, the counter-voltage (TIV) steadily reduces the current to zero; while the system's inductive energy is dissipated in the arrester of path 3. Current zero is then reached at t_3. A small residual current remains, which has to be interrupted by an additional switch, designated by

auxiliary breaker in Fig. 2 Similar illustration using active injection type HVDC CB model can be found in [45], [47].

III. Mathematical Description

Besides the current commutation inside a model of a CB, Fig. 3 shows the voltages across the circuit breaker (U_{CB}) and at the converter terminal (U_C) during interruption process. It can be seen that with the assumptions and modifications made in the preceding section, the system voltage remains within 80 % of the nominal value, which is acceptable for continued controlled operation of a converter [37]. From CB operation point of view, this results in the most onerous condition as it leads to high rate of rise of fault current. Assuming constant terminal voltage of a converter, mathematical analysis of system transients is provided in this section.

For mathematical simplicity, the analysis is split into two time intervals; fault current neutralization interval (t_0-t_2) and fault current suppression (energy absorption) interval (t_2-t_3). The time the voltage across the breaker rises to protection level is assumed to be negligible.

A. Fault current neutralization period

This is an interval from fault inception (t_0) until the time the counter voltage built up across the breaker equals (exceeds) system voltage (t_2, see Fig. 3). The fault current rises with its rate limited by equivalent inductance of the system (L) as,

$$\frac{di}{dt} = \frac{1}{L}\left(U_C - Ri\right) \tag{1}$$

where, i is the fault current, U_C is converter terminal voltage and R is resistance up to the fault location. Assuming initially steady state load current I_o, the solution of (1) is,

$$i(t) = \frac{U_C}{R}\left(1-\exp(-t/\tau)\right) + I_o \exp(-t/\tau) \tag{2}$$

where $\tau = L/R$ is the time constant of the system. From (2), it can be seen that current increases to a steady state value of U_C/R, if not interrupted by a CB.

B. Fault current suppression period

This is a time from the moment the voltage across the HVDC CB reaches the nominal voltage (t_2) till the system current ceases to flow or falls to a residual value (at t_3), see Fig. 3. For simplicity, the voltage across the CB is approximated as a constant value, U_{CB}, in this interval. With this assumption, the system equation during fault current suppression time becomes,

$$U_C - L\frac{di}{dt} - Ri - U_{CB} = 0 \tag{3}$$

If I_P represents the peak value of fault current, it decays and finally ceases to flow only if $U_{CB} > U_C$. This can be seen from the solution of (3) as,

$$i(t) = \frac{U_C - U_{CB}}{R}\left[1-\exp(-t/\tau)\right] + I_p \exp(-t/\tau) \tag{4}$$

Moreover, from (4), the time (t_s) required to suppress the fault current can be determined by setting $i(t)$ to the threshold value of the leakage current (zero). Accordingly, the fault clearing time t_s is,

$$t_s = \tau \ln\left[1+\frac{R}{U_{CB}-U_C} I_p\right] \tag{5}$$

From (5) it can be seen that the time required by an HVDC CB to suppress current I_p to a small leakage current (zero) is depending on the system time constant (τ) and the maximum protection level of a surge arrester in the breaker (U_{CB}). Increasing the counter voltage of a CB will reduce t_s; however, it has an impact on the dielectric strength of the other components of a CB as well as overall system insulation. Combining (2) and (5), the fault current suppression time t_s can be expressed as a function of system and CB parameters as follows:

$$t_s = \tau \ln\left[1+\frac{U_C}{U_{CB}-U_C}\left(\left(1-\exp(-t_2/\tau)\right)+I_o \exp(-t_2/\tau)\right)\right] \tag{6}$$

Important conclusions which can be drawn from the above mathematical analysis regarding the requirements of a test circuit are that a test circuit must:

1. Produce a fast rising current that increases to a value up to at least the rated interruption current I_p.
2. Have sufficient energy stored in its lumped reactor that corresponds to the magnetic energy stored in the system inductance.
3. Stress the HVDC CB with nominal and constant voltage during the energy dissipation phase of the interruption process and afterwards.

IV. Candidate Test Circuits for HVDC CB

Three types of test circuits supplied by different sources: namely, high-voltage charged capacitor banks, high-current charged reactor and variable frequency ac short-circuit generator are considered.

A. High-voltage charged capacitor banks

A capacitor charged to a given DC voltage (equivalent to system voltage) can be used as a current source for HVDC CB testing as shown in Fig. 4. In order to limit the rate of rise of current to within the design capabilities of an HVDC CB, a reactor (L) is connected as shown in Fig. 4.

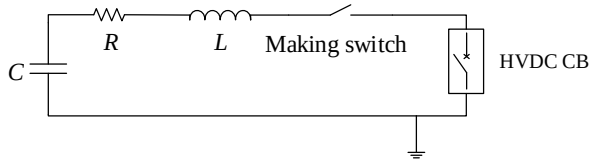

Fig. 4. Test circuit supplied by a charged capacitor

The main challenge with this method is that the voltage across the capacitor decays fast when the values of C and L are in a practical range. This makes the interruption process too easy for the circuit breaker since the difference between the counter voltage produced by the HVDC CB and the voltage across the capacitor banks is very large during the current suppression interval (refer to (5)).

B. High- current charged reactor

By discharging the magnetic energy stored in a current-charged reactor through a test object it is possible to produce quasi-DC current for the test duration. Various methods of charging a reactor have been discussed in [21], [48], [49]. Fig. 5 depicts a test circuit using the charged reactor method. Note, during testing the charging circuit designated by ac source is disconnected by the ac CB.

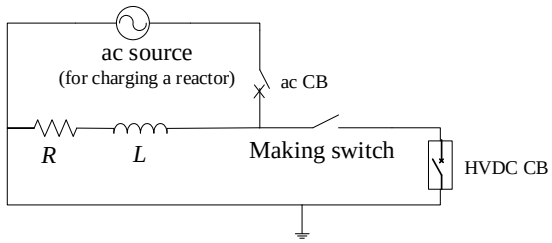

Fig. 5. Test circuit supplied by a charged reactor

This test circuit can produce pseudo-DC current required during the interruption process. However, it lacks an intrinsic voltage source during the interruption process as a result of which current is interrupted rapidly, making the test too light for the test object. This can be related to (5) where U_C is zero since there is no driving voltage in this case. Moreover, the current decay in such a circuit depends significantly on the circuit resistance and hence requires reactors with a very high quality factor.

C. Test circuits with variable frequency ac sources

As stated earlier, a HVDC CB must interrupt a fault current on its rising edge well before it reaches its steady state value. This justifies the fact that a steady state DC current is not necessary for testing the interruption performance of HVDC CBs. For this reason, test circuits supplied by ac short-circuit generators as shown in Fig. 6, especially running at low power-frequency, can be used.

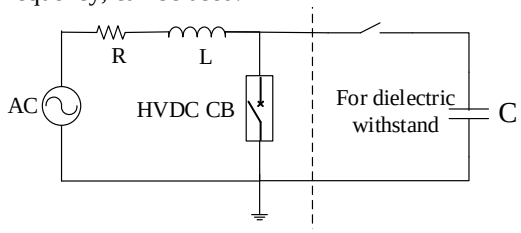

Fig. 6. Equivalent circuit of test circuit using ac generator(s)

The tests using short-circuit generator(s) discussed in the literature mainly focus on producing the maximum quasi–DC current for longer duration while the magnitude of driving voltage of the test circuit is not of prime concern in the studies. In those tests interruption is deemed as successful if the CB interrupts the peak ac current well before its natural current zero. However, when the ac current is at its peak, the driving voltage is zero and even changing its polarity afterwards (thus the generator starts absorbing system energy instead of providing energy), which makes the interruption duration much faster as can be justified in (5).

Therefore, a method to ensure sufficient energy contribution from a short-circuit generator, by maintaining its voltage magnitude within an acceptable range for the entire test duration, is introduced in this paper. It must be clear that the short-circuit generator must have sufficient power and must produce the ac voltage having a peak value equal to the rated system voltage for which the HVDC CB is designed. In such a way the requirements of a test circuit described in Section III can be achieved. In fact this can only be realized with careful choice of making angle (θ) for the ac voltage of the generator(s) as described in (7),

$$\frac{di}{dt} = \frac{E_m \sin(\omega t+\theta) - Ri}{L} \tag{7}$$

From (7), it can be seen that d*i*/d*t* follows the instantaneous value of the back emf of the generator ($E_m \sin(\omega t + \theta)$). The maximum d*i*/d*t* at a moment of short circuit is obtained when $\theta = 90^0$. However, in order to achieve a constant d*i*/d*t* during the fault neutralization interval, the short circuit must be made at $\theta < 90^0$. The other requirement is that it is necessary to maintain the driving voltage as constant as possible during the interruption process. This can be seen from (5) showing that the test object can be put under maximum stress if the driving voltage is at its peak during the fault current suppression period. This ensures a maximum energy contribution from the source.

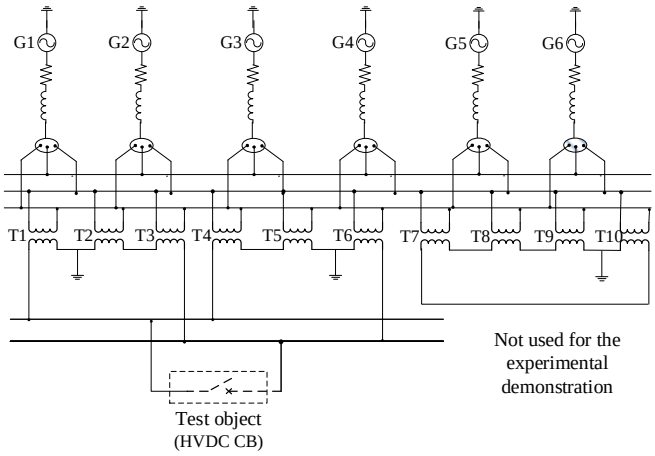

Fig. 7. Actual installation of four short circuit generators (G1-G4) and six transformers (T1-T6) for HVDC CB testing at KEMA high power laboratory. The additional two generators (G5-G6) and four transformers (T7-T10), shown on the right, are not used.

Thus, depending on the length of the fault neutralization period, the making angle θ becomes an optimization parameter for both sufficient rate of rise current and maximum energy contribution.

Fig. 7 shows the actual installation of short-circuit generators at KEMA laboratories. Six short-circuit generators with a total power of about 15 GVA (at 50 Hz) along with 10 step-up transformers are available for testing. However, the challenge when using short-circuit generators at low frequency is that the short-circuit power of the generators reduces proportionally with the power frequency. Sufficient transformers and generators can overcome this short-coming.

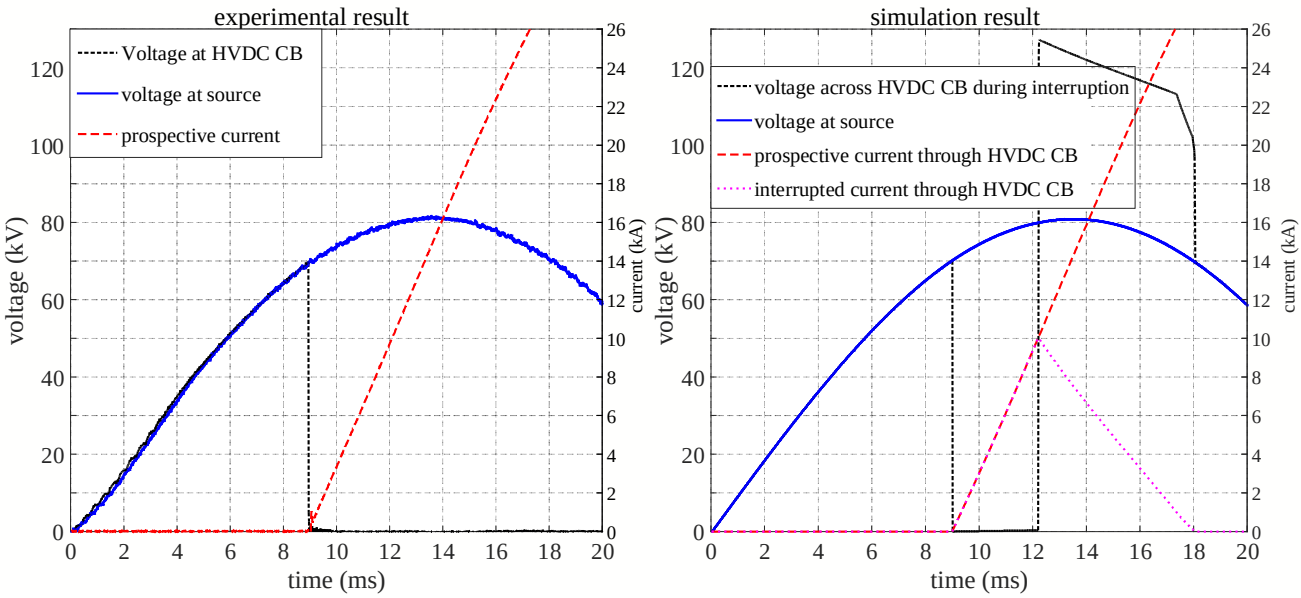

Fig. 8. Experimental results (left) versus simulation results (right). The experimental result is obtained by running four short-circuit generators at 18 Hz in combination with six transformers. Interruption process by a model of HVDC CB inserted in a simulation test circuit is superimposed (right graph).

The equivalent reactance of the test setup, including the sub-transient reactance of the four generators and the leakage reactance of the step-up transformers with the arrangement depicted in the Fig. 7, is circa 25 mH.

Fig. 8 juxtaposes experimental results (left) and simulation results (right) of a test circuit by ac short-circuit generators running at 18 Hz. Four generators and six step-up transformers are used for this demonstration experiment in order to determine the prospective current and voltage in the absence of the test object (HVDC CB) shown by dotted line in Fig. 7. The left side scales for both graphs show voltage measurements while the current measurements are on the right side scale of each graph. The short circuit is made at a making angle (θ) of 60^0. With this angle and generator frequency of 18 Hz, it can be seen from the experimental results (the graph on the left side) that the back emf of the generator remains within 80 % of the peak value from the moment of short circuit up to the next 10 ms. Moreover, sufficiently linear short circuit current rising at a rate of 3.2 kA/ms is achieved.

The graph on the right side illustrates simulation result obtained with the same system setting as the experimental set-up. The four generators and the six step-up transformers are represented by equivalent ac source behind impedance.

It is clear that the simulation result sufficiently agrees with the experimental result. Moreover, a model of hybrid type HVDC CB is inserted into the simulation set-up in order to observe the expected electrical stresses on a real HVDC CB during interruption process in this test circuit. Assuming a fault current neutralization period of about 3 ms, 10 kA current is interrupted.

V. Comparison of Simulation Results of Test Circuits

In order to investigate the performance and feasibility of the test circuits described above, a simulation study is discussed in this section. Fig. 9 shows simulation results of test circuits including the ideal DC source circuit (added to provide a reference) when current in each case is interrupted by a model of hybrid type HVDC CB having the interruption characteristics illustrated in Fig. 3. Considering the plots in Fig. 9a there is a slight difference in d*i*/d*t* during fault neutralization time especially for the charged reactor and the charged capacitor test circuits. However, the main difference among the various test circuits is during the energy absorption phase which results in a significant difference in time to clear the fault. This difference is due to the fact that for each of the test circuits, the magnitude of source voltage during energy absorption phase is different (see Fig. 9b). The difference is also clearly reflected in the amount of energy absorbed by the CB for each test circuit (see Fig. 9c).

Note that, for each of the test circuits the energy in the system ($(Li_p^2)/2$) at the moment the counter voltage starts to act (see Fig. 9a) is identical since the magnitude of reactor (L) used for each case is kept the same (20 mH). Therefore, the extra energy to be dissipated in the MOSA is contributed by the voltage source in the circuit.

Mathematically, this can be illustrated by using the energy balance equation during the energy dissipation phase of the interruption process which can be computed by using the corresponding expressions for current and voltage in each test circuit. Accordingly, the energy balance in the system is,

$$\int_0^{t_s} V_{source}(t)i(t)dt + \frac{1}{2}LI_p^{\,2} = \int_0^{t_s} U_{CB}i(t)dt + \int_0^{t_s} Ri^2(t)dt \quad (8)$$

The first term on the left side of (8) represents the energy supplied by the source during the fault current suppression period whereas the second term in the same side represents the energy initially stored in the reactor just before the fault

current suppression time. The right side of (8) represents the energy dissipated in the CB and in the circuit resistance where the latter is negligible compared to the former since a very small circuit resistance R (about 0.25 Ω used in the simulation) is considered. Thus, a test circuit using a charged reactor does not contain an intrinsic voltage source during the interruption process and hence only the energy stored in the reactor is dissipated. Similarly, for charged capacitor test circuit, since a significant portion of the charge stored in the capacitor bank is already lost at the beginning of the current suppression phase, the energy contribution from this source is minimal. Thus, with respect to the energy requirement, the charged reactor and charged capacitor test circuits cannot provide sufficient stress for testing an HVDC CB regarding its energy handling capability.

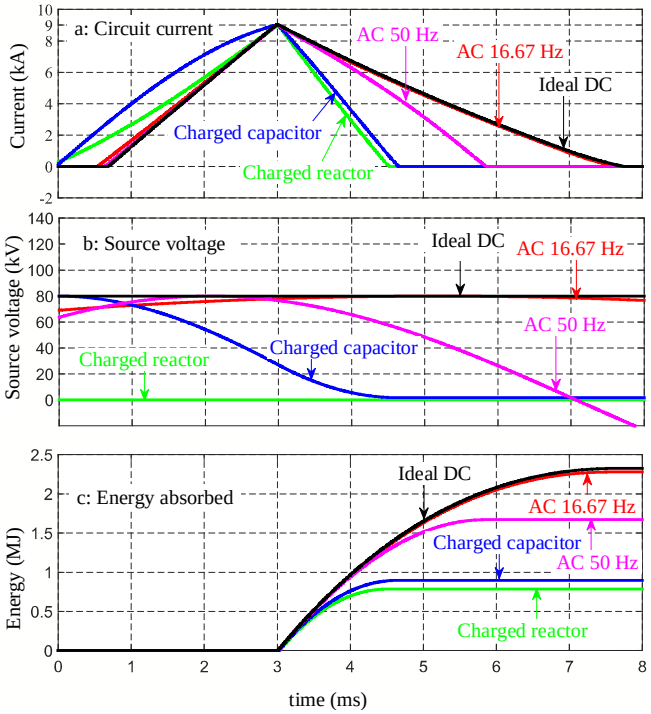

Fig. 9. Comparison of simulation results of various test circuits.

The main conclusion from the simulation results of the test circuits shown in Fig. 9 is that a test circuit using ac short-circuit generators having low frequency (specifically 16.7 Hz) is sufficient for testing the HVDC CB. (16.7 Hz is a power frequency applied in railway applications in various countries). Compared to charged reactor and charged capacitor test circuits, 50 Hz ac generator test circuit has better performance. However, when evaluated with respect to an ideal DC and 16.7 Hz ac source test circuits, the 50 Hz ac source lacks sufficient thermal stress on the test object.

Nevertheless, as illustrated in the preceding section, care must be taken when using ac sources for HVDC CB testing. The voltage magnitude, and hence the making angle, must be chosen in such a way that the crest of the source voltage appears during the energy absorption phase of the interruption process. In this way sufficient energy contribution from the source, and as a result, adequate stress on the energy absorption component of the breaker is guaranteed.

VI. Conclusion

The requirements of test circuits for HVDC CBs are as follows:

1. Produce a rapidly rising current. However, a test circuit need not necessarily produce steady state DC current.
2. Have sufficient energy stored in a lumped reactor that corresponds to an equivalent magnetic energy stored in DC grids at the beginning of the energy dissipation phase.
3. Stress the HVDC CB with nominal and “as constant as possible” voltage during the energy dissipation phase of the interruption process.

HVDC CBs must be tested not only for “local” current zero creation capability inside the interrupter, but also for their counter voltage generation, system current suppression and the energy dissipation throughout the entire fault removal process.

In this paper it is shown that, during fault current interruption, the energy to be dissipated comes from the magnetic energy stored in the system inductance (as an initial condition) as well as from converter stations during the current suppression process. The magnitude of the latter depends on the magnitude of the source voltage during current suppression period.

Several HVDC CB test circuits are investigated and compared via simulations. Current charged reactor and a pre-charged high-voltage capacitor banks cannot maintain the driving voltage sufficiently long enough during the interruption process. Consequently, these cannot be considered as sufficient for testing an HVDC CBs. Nevertheless, the use of high-power, low frequency ac short-circuit generators , with a proper choice of voltage crest value and making angle, is adequate for testing the DC switchgear in terms of di/dt, voltage stress as well as energy supply during the relevant periods.

VII. References

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