Analysis of Faults in Multi-Terminal HVDC Grid for Definition of Test Requirements of HVDC Circuit Breakers

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***Abstract*—The paper provides a detailed analysis of the temporal development of fault currents in a multi-terminal high voltage direct current (MT-HVDC) grid composed of bipolar converter configuration. The sequence of events following the occurrence of a pole-to-ground fault is identified, divided into three distinct periods; namely, sub-module capacitor discharge, arm current decay and ac in-feed periods. The critical parameters that have a significant impact on the fault current in each period are discussed. The impacts of various parameters of the HVDC grid such as the size of the current limiting reactor, ac grid strength as well as the location of the fault within the grid are studied through PSCAD/EMTDC simulation. Then, a fault current interruption process using models of various HVDC circuit breaker technologies and the resulting stresses are studied. Both serve as important inputs to define test procedures. It is found that the HVDC CBs are subjected to not only dc current and voltage stresses but also energy stress. These stresses are translated into test requirements.**

***Index Terms*—HVDC circuit breakers, HVDC transmission, multi-terminal HVDC network, power system transients, test circuits, testing, test requirements.**

I. Introduction

SEVERAL point-to-point HVDC connections are in operation, connecting large offshore wind resources in the North Sea to the European mainland. Expansion into a multi-terminal network is the next logical step to improve reliability, share capacity and interconnect various national networks. To date, only two voltage source converter (VSC) MT-HVDC grids are in operation [1], [2]. However, a few major technical challenges need to be addressed before such systems, with dc side protection, are realized. One of the main challenges is the lack of fast, low loss and reliable HVDC circuit breakers (CBs) capable of clearing dc faults.

Several manufacturers have proposed and developed prototypes of HVDC CBs [3]–[7]. The behavior of these prototypes has been studied through a range of development tests in the manufacturers' own labs. Testing of HVDC CBs is fundamentally different from that of ac CBs as both voltage across and current through the CB exist simultaneously, leading to an energy absorption requirement [8].

Meaningful demonstration of HVDC CB technology is achieved when tests accurately reflect realistic fault conditions. Thus, based on fault analysis of MT-HVDC networks, it is necessary to first define suitable test requirements and a test program, as well as to realize a proper test circuit. So far, due to the lack of practical VSC MT-HVDC networks in operation, research has been limited to simulation studies using different conceptual HVDC networks [9]–[12].

Nevertheless, fault current testing envelopes for HVDC CBs have been investigated for different converter topologies under various fault conditions in [13], and several design considerations of HVDC CB such as energy absorption requirement, minimum dc reactance required to prevent a converter from blocking, etc. have been studied in [14]. However, these studies mainly focus on fault currents supplied by a converter and do not consider the impact of the in-feed from multiple line/cable connections in a MT-HVDC environment. Network topology and converter configuration have significant impact on the requirements of HVDC CBs [10], [15]. In addition, an investigation of fault current contributions of various elements as well as the impacts of different grounding schemes in MT-HVDC networks have been conducted [16], [17]. In this case a bipolar converter represented by a simple diode rectifier, assuming a blocked converter during fault, is simulated. Moreover, a four-terminal meshed HVDC network developed based on the same assumption is used for the investigation of the current interruption processes in various HVDC CB technologies [18]. However, the fact that all converters are represented as blocked converters during a pole-to-ground fault is not realistic since in practice only the converters on the faulted pole and only stations located close to the fault are affected. In addition, this assumption has insufficient detail of the events occurring during the transition from normal operation to fault condition because of the lack of a control system. In another study, a four-terminal radial network based on symmetric converter configuration is used to simulate the use of dc current limiting reactors for suppressing dc fault currents [7]. Acknowledging the importance of having a unified benchmark system for harmonizing the research related to MT-HVDC networks, CIGRE WG B4-57 and WG B4-58 have developed an 11-terminal HVDC system, which consists of ac and dc grids having multiple in-feeds with OHLs and cables [19]. Detailed data and control parameters for steady state power flow have been provided.

Driven by various purposes of studies, a multitude of MT-HVDC network topologies along with various converter configurations and system parameters have been investigated. In most cases a fault analysis based on either initially blocked

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converter (rectifier) or a converter that does not block at all during faults are considered [7], [9], [12]. However, a generic study showing the detailed phenomena during dc faults, independent of network topology, is missing in the literature.

This paper provides a detailed analysis of the temporal development of fault current in MT-HVDC networks based on half-bridge modular multi-level converter (MMC) topology. For this purpose, a PSCAD model of MMC based on enhanced equivalent model (detailed equivalent model with blocked operation capability), developed by Manitoba HVDC research center (PSCAD/EMTDC^{TM}) is used [20], [21]. In addition, the electrical stresses on HVDC CB during fault current interruption are investigated and the stresses are translated into test requirements of the HVDC CBs.

The paper is organized as follows. In Section II a brief description of the background of the system used in the paper as well as the assumptions made in the study are provided. Detailed analysis of converter dc fault response is presented in Section III. In Section IV, fault current generic to half-bridge MMC based VSC MT-HVDC network is presented. The effect of various critical network parameters having an impact on the fault current are discussed. Finally, fault current interruption by HVDC CB and analysis of the resulting electrical stresses is presented in Section V. The conclusions based on the results of the study are provided in Section VI.

II. Background

Although the point-to-point offshore HVDC converters constructed so far are symmetric monopole, the choice of which converter configuration is suitable for offshore MT-HVDC network needs considerable techno-economic benefit analysis. For instance, a pole-to-ground fault in a network built from symmetric monopole converters may result in an overvoltage as high as twice the nominal voltage. This requires the system components to be rated for such an overvoltage, which especially for the cable can lead to a prohibitively high cost. In addition, even if the rating issue is technically possible to handle, the doubled floating voltage persists after a fault is cleared. This implies that the whole dc grid must be shut down, the healthy pole be discharged, and then re-energized every time a pole-to-ground fault occurs. In a network built from bipole converters, a pole-to-ground fault results in a very large current flowing in the system, thus, requiring very fast HVDC CBs to clear the fault before the entire system voltage collapses and the continuity of supply is lost. In any converter configuration, a pole-to-pole fault is the most severe, resulting in a rapidly rising fault current that can damage the system components. In this paper, only a pole-to-ground fault in a MT-HVDC network based on bipole converters is considered. A pole-to-pole fault for symmetric monopole converter is investigated in [22].

In order to selectively clear dc faults by the recently proposed HVDC CBs, suitably dimensioned dc current limiting reactors are required. These not only reduce the rate of rise of fault current but also delay the propagation of the impact of the fault (voltage collapse) within the network. Also for fast, selective and reliable protection algorithms the dc reactors are important [23]–[26]. Thus, in this paper, unless otherwise explicitly stated, a current limiting reactor of *100 mH* are placed at the ends of each dc cable to limit the fault currents within the breaking capabilities of the recently proposed HVDC CBs.

Nowadays, VSCs based on modular multilevel converters (MMC) have become the preferred converter topology because of its various advantages compared to other VSC converter topologies [27], [28]. Examples of MMC HVDC projects include the Trans Bay Cable project in USA, INELFE from France to Spain, etc. A typical half-bridge MMC is shown in Fig. 1 and the simulation parameters are shown in Table I.

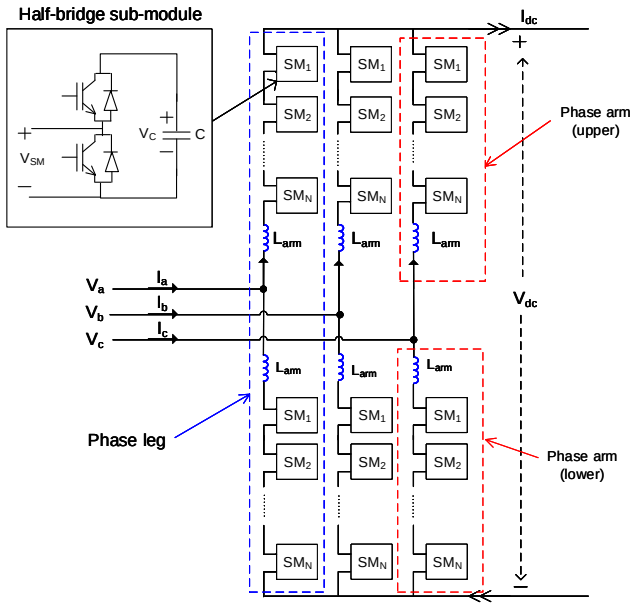

Fig. 1. Modular Multi-Level Converter (MMC)

TABLE I
SYSTEM SIMULATION PARAMETERS

Parameter	Value
Rated power per pole	800 MVA
Active power set point	600 MW
Arm reactor	15 %
Transformer leakage reactance	18 %
Primary voltage	145 kV
Secondary voltage	220 kV
AC system frequency	50 Hz
DC voltage	±320 kV
Number of submodules per arm	160
Submodule capacitor	12.5 mF
Modulation technique	Nearest level control (NLC)

III. MMC Converter DC Fault Response

A short circuit on a charged power line (cable or OHL) provokes travelling waves that propagate along the line in both directions of the fault location. The magnitude of the wave depends on the fault resistance [16]. The voltage wave travel along the cable, while discharging the distributed capacitance

along its way, towards the dc buses at either ends of the faulted cable, where converters and/or other links are connected. Considering a pole-to-ground fault on positive pole in a bipolar HVDC grid interconnected with cables, the incident travelling wave first arrives at the current limiting reactors at the ends of the faulted cable, before propagating into the other elements connected to the dc bus. A part of this incident wave is transmitted through the current limiting reactor while large part of it is reflected.

To illustrate this phenomenon, a simplified equivalent system of the two sides of the current limiting reactor (L_{dc}) is shown in Fig.2.

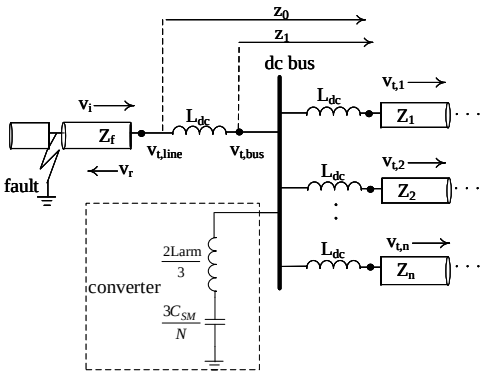

Fig. 2. Simplified system diagram demonstrating the impact of current limiting reactor during fault

Assuming the incident voltage wave as a (negative) step function for simplicity, the part of the wave that is transmitted through the current limiting reactor is given by the following mathematical equation (in Laplace domain),

$$v_{t,line} = \frac{2z_0}{z_0 + Z_f} v_i = \frac{2(z_1 + sL_{dc})}{z_1 + sL_{dc} + Z_f} v_i \qquad (1)$$

Where $z_0 = z_1 + sL_{dc}$ is the equivalent impedance of the system seen at line side of current limiting reactor, Z_f is the characteristic impedance of the faulted cable and v_i is the magnitude of incident travelling wave (see Fig. 2). Considering the right-hand side of (1) in reference with Fig. 2, the first term in the numerator represents the part of the incident wave going into the dc bus whereas the second term represents part of the transmitted voltage wave dropped across the current limiting reactor itself. Solving (1), the transmitted voltage wave in time domain,

$$v_{t,line} = v_i \left(\frac{2z_1}{z_1 + Z_f} \right) \left(1 + \frac{Z_f}{z_1} \exp\left(-\frac{z_1 + Z_f}{L_{dc}} t \right) \right) \qquad (2)$$

From (2) the part that is propagating into the system and, thus causing the discharge of any capacitive elements including sub-module capacitors; and the part that appears across the current limiting reactor, respectively, are

$$v_{t,bus} = v_i \left(\frac{2z_1}{z_1 + Z_f} \right) \left(1 - \exp\left(-\frac{z_1 + Z_f}{L_{dc}} t \right) \right) \qquad (3)$$

$$v_{L_{dc}} = 2v_i \exp\left(-\frac{z_1 + Z_f}{L_{dc}} t \right) \qquad (4)$$

Furthermore, part of the voltage wave propagating into the one of the cables connected to the dc bus is,

$$v_{t,i} = \frac{Z_i}{Z_i + sL_{dc}} v_{t,bus} = \frac{Z_i}{Z_i + sL_{dc}} \frac{2(z_1 + sL_{dc})}{z_1 + sL_{dc} + Z_f} v_i \qquad (5)$$

Where z_1 is the equivalent impedance seen at the bus side of the current limiting reactor on a faulted cable. Equations (1)-(4) show that the larger the dc current limiting reactor, the smaller the incident wave that is transmitted into the rest of the system during the transient period. Note that the transmitted voltage waves superpose onto the initial voltage across the capacitive elements and have opposite polarity to the initial voltage. Although much depends on the system under consideration, the choice of the size of dc current limiting reactor shall ensure the following important points:

1) Within the operation time of the HVDC CBs (including protection relay time), the magnitude of the fault current must not exceed the maximum interruption capability of the CB for any dc fault.
2) Preferably the converters connected to the healthy cables be able to continue their controlled operation. Thus, the dc voltage of the healthy part should remain within the acceptable limit for continued controlled operation.

It must be noted that as the wave travels along the cable it is attenuated due to the resistance of the conductor and this is not considered in the above analysis. For illustration purpose, the phenomena after the arrival of the first voltage wave at a converter terminal is demonstrated in three different time periods assuming no action is taken by either ac or dc side protection equipment for a fault occurring close to a converter terminal.

A. *Sub-module capacitor discharge period* $(t_1 < t < t_2)$

The part of the travelling voltage wave that is transmitted to the converter through the dc current limiting reactor propagates

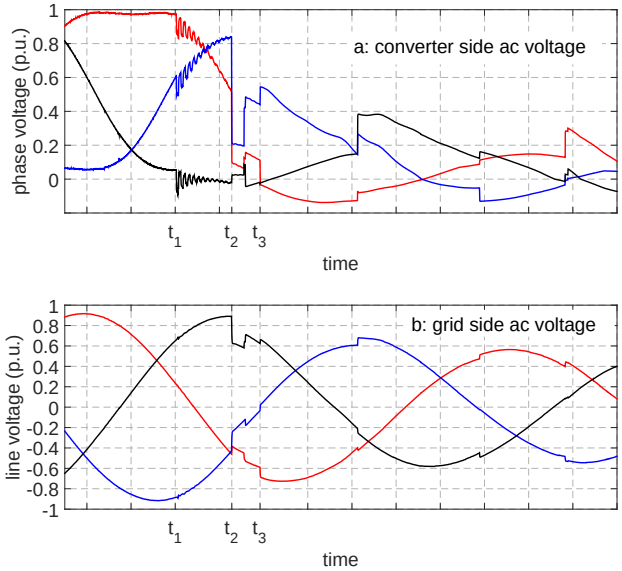

Fig. 3. a: Secondary (converter side) voltage. b: primary (grid side) voltage of a converter transformer

into the three phase-legs of the MMC converter (at t_1 in Fig. 3). Here, the wave partly discharges the sub-module capacitors, resulting in a rapidly increasing current. The converter keeps control of its ac side parameters (ac currents and line-to-line ac voltages) until the threshold for converter blocking is reached at t_2. Although identical oscillations are observed in the phase voltages (seen from $t_1 - t_2$ in Fig. 3a), the line-to-line voltage remains unaffected since the oscillations in the phases cancel out. This can be seen from Fig. 3b which depicts the line-to-line voltage on the ac grid side of the converter transformer. Thus, the converter is in full control of its ac voltage until it blocks at t_2. The flattened peaks of the phase voltages in Fig. 3a are due to third harmonic injection from a converter control.

By limiting the magnitude of the transient voltage wave transmitted into the converter, the dc current limiting reactor reduces the discharge of sub-module capacitors of the MMC converter. Therefore, depending on the inductance of this reactor it can significantly delay converter blocking time. Fig. 4 shows the current through the converter arms along with ac currents (per unitized with peak value of converter ac current). This figure shows that the converter can keep control of its ac currents although the dc components of the arm currents are increasing. The increase in the dc components of the arm currents is due to the additional discharge of the sub-module capacitors caused by the travelling voltage waves. Theoretically, the discharge of the sub-module capacitors continue until the converter is no longer able to control its ac outputs. However, in practice, the converter blocks before it loses its controllability. This can be either because over-current is detected in at least one of its arms and/or because its dc voltage has fallen below a certain threshold value. Hence, by blocking the converter, further discharge from the sub-module capacitors is prevented.

The overall dc current output of a converter is shown by

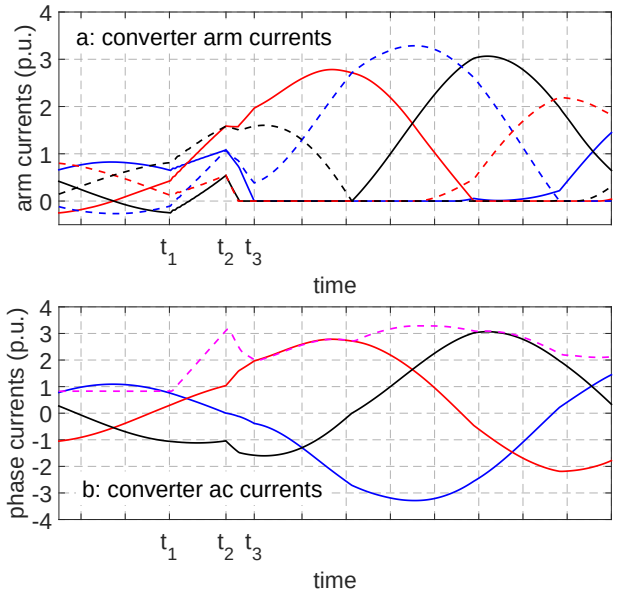

Fig. 4. a: arm currents (solid lines for upper arm and dashed lines for lower arm current). b: converter three phase ac currents (solid lines) and converter dc current (dashed line)

the dashed curve in Fig. 4b. The rate of rise of discharge current from the converter is limited by the arm reactors, the dc current limiting reactor as well as the inductance of the line up to the fault location. During this period, each phase leg can be considered as an RLC circuit operating in parallel resulting in the equivalent circuit shown in Fig. 5 using an approach similar to [12], [29]. Assuming equal discharge of

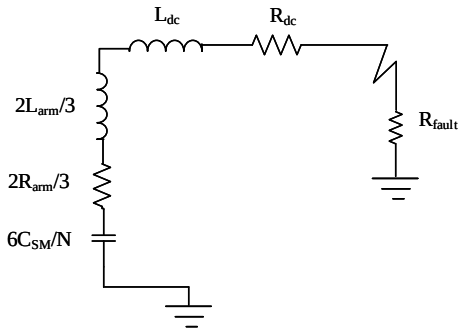

Fig. 5. Equivalent circuit of a converter during sub-module capacitors discharge period

sub-module capacitors in the phase leg due to the voltage balancing algorithm of the converter control, the rate of rise of fault current from the converter can be obtained as (valid for a fault close to a converter terminal, until blocking),

$$\frac{di}{dt} = \left[B\left(\omega^2 + \alpha^2\right) sin(\omega t) - A\left(\omega^2 - \alpha^2\right) cos(\omega t)\right] \exp(-\alpha t) \tag{6}$$

where, $\alpha = \frac{R}{2L}, \omega = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}, A = CV_{dc}, B = \frac{I_0 + A\alpha}{\omega}$

$R = R_{dc} + R_{fault} + \frac{2}{3}R_{arm}, L = L_{dc} + L_{line} + \frac{2}{3}L_{arm},$

$C = 6\frac{C_{SM}}{N}$, I_0 is the initial steady state dc current. Neglecting the resistance in the circuit, (6) can be simplified further,

$$\frac{di}{dt} = \frac{V_{dc}}{L} cos(\omega t) \tag{7}$$

From (6), it follows that the capacitance of the sub-module capacitor has an impact on the rate of rise of current from a converter. The capacitance of the sub-module capacitors are chosen such that the voltage ripple across these capacitors remain within tolerable limit during steady state operation, for instance, within a maximum of ± 10 % has been suggested as acceptable [30]. For small sub-module capacitors, the under-voltage threshold for blocking is reached before the over-current threshold for the arm current is reached. The size of the sub-module capacitor is proportional to the converter rated power.

B. Arm current decay period $(t_2 < t < t_3)$

During a dc fault, when a converter has not yet blocked, the dc components of the arm currents increase without affecting the phase currents (in the interval $t_1 - t_2$ in Fig. 4). When the converter blocks, the arm currents cannot be instantly switched off because of the presence of the arm reactors. In fact, by blocking the converter the sub-module capacitors are bypassed and there is no further discharge from these

capacitors. However, the arm currents continue to flow through the freewheeling diodes (from $t_2 - t_3$ in Fig. 4) and since the currents in all the arms have positive values, the freewheeling diodes in all the arms are conducting. Thus, for some time, the ac side is essentially decoupled from the dc side. Besides, the dc voltage of the converter significantly drops during this period (see Fig. 7b in Section IV). During this period, there is no inherent voltage source supplying the dc side.

On the ac side, until one of the phase arms ceases to conduct, the fault appears to be a three phase fault with an ac impedance equal to,

$$Z_{total} = Z_{ac} + Z_{tr} + \frac{1}{2}Z_{arm} \tag{8}$$

Where,Z_{ac}, Z_{tr} and Z_{arm} are, respectively, the impedances of ac system at the point of common coupling (PCC), the converter transformer and converter arms. However, the currents in three of the arms having the lowest values soon decay to zero thus changing the converter into a diode rectifier mode of operation and the impedance seen by the ac side also changes. The dc current from a converter also decays with the arm currents until the ac in-feed starts (see $t_2 - t_3$ in Fig. 4b).

C. *ac in-feed period* $(t > t_3)$

After current through three of the arms decayed to zero (at t_3,) the dc current output from the converter is entirely contributed from ac in-feed. Here it must be noted that due to the inductance of the arm reactors and the transformer leakage reactance (including any ac side reactance) at least three of the phase arms are conducting at a time. In fact, later, if the fault is not cleared by dc CBs or if the ac side is not disconnected from the converter by ac CBs, there will be a commutation overlap between more than three arms as the ac in-feed through each arm increases. Moreover, because of this commutation overlap, the dc voltage is not exactly a six-pulse rectified voltage. This can be seen from Fig. 7b in Section IV.

It is important to note that the magnitude of the ac in-feed depends on the strength of the ac network at the PCC, the impedance of the converter transformer, arm reactors as well as the impedance on the dc side up to the fault location. The strength of the neighboring ac network, however, does not affect the fault current until a converter blocks.

IV. Analysis of DC Fault Currents in MT-HVDC Network

If only one cable is connected to a dc bus, then the same current coming from the converter would flow through the faulted cable and the HVDC CB connected to it. Under this situation the need for an HVDC CB is not mandatory as the fault can be cleared by an ac CB on the ac side of the converter. However, when there are multiple cable connections at the dc bus, as shown in Fig. 6, the faulty cable needs to be selectively isolated to reduce the impact on the healthy part of the dc grid; thus, HVDC CBs are required. Therefore, the presence of multiple connections at dc bus have impacts on the fault current magnitude flowing through the CB of a faulted cable.

Fig. 7 shows simulation results when a fault is applied close to a converter with three cables connected to its dc bus. Fig. 7a

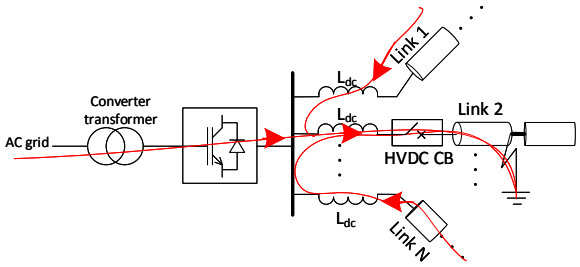

Fig. 6. dc fault close to a converter terminal with multiple connections

depict all current measurements (per unitized with converter dc current); the current through the CB of the faulted cable (solid curve), the current contributed by the converter side (dashed curve) and current from the discharge of two healthy cables (dotted and dash-dotted curves). Because of the additional discharge current from the adjacent cables, the rate of rise of current through a CB is higher than the rate of rise of current rising at the output of the converter. Nevertheless, the converter is the dominant contributor during the sub-module capacitor discharge stage (see between $t_1 - t_2$ in Fig. 7a).

Considering individual contributions, the discharge from the healthy cables is suppressed by two current limiting reactors; one at the end of the cable itself and the other at end of the faulted cable. This can be seen from (5) where the transient transmitted voltage wave at the dc bus is further divided between the drop across the current limiting reactor and the part that propagates along the cable. Nevertheless, the current contributions of the healthy cables become significant after the converter blocks (from t_2 on wards in Fig. 7a). Especially, during the arm current decay period, the voltage at the dc bus drops significantly since there is no inherent voltage source as mentioned earlier. The collapse in the dc bus voltage during this period creates another transient resulting in further discharge from the adjacent cables and hence, the current through CB keeps increasing although the current contributed by the converter is decreasing (see between $t_2 - t_3$ in Fig. 7a).

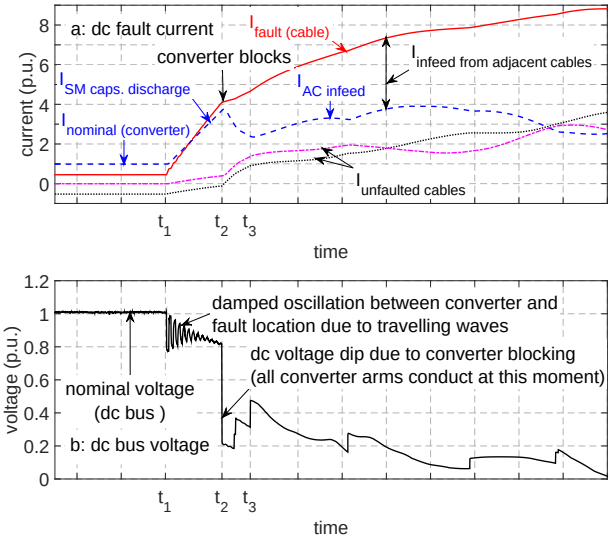

Fig. 7. a: converter dc current (blue) and current at CB location (red curve). b: converter dc output voltage

A. Impact of fault location

One of the key factors affecting the rate of rise of fault current is the location of a fault within the dc network. The location of the most severe fault condition is determined by several factors including whether a fault is on overhead line or a cable, the number of feeders at the bus to which the faulted link is connected, the distance of fault from the dc bus, etc.

Fig. 8 shows simulation results of faults on a cable at different distances from a converter. For comparison purpose, the time delays of the travelling waves from the fault locations to the converter terminals are removed in this figure. As the distance of a fault from a converter increases, the initial rate of rise of fault current increase. This can be seen from the curve of a fault at *100 km* in Fig. 8a having higher initial rate of rise of current. However, beyond a certain distance determined by the cable characteristics, the initial rate of rise of fault current start to decrease due to attenuation of the travelling waves. This is the reason why the current for a fault at *100 km* has the higher initial rate of rise compared to the current for a fault at *240 km* since the travelling waves are attenuated less in *100 km*. Nevertheless, this is valid only until the reflected travelling waves propagate to the fault location and come back to the converter terminal. Hence, assuming a fault neutralization time of t_N, the time from occurrence of a fault until a CB builds a counter voltage for current interruption, the highest theoretical rate of rise of fault current is when a fault occurs at a distance of at least S where S is determined as in [25], [31],

$$S = \frac{vt_N}{3} \tag{9}$$

Where v is the speed of the travelling wave through the cable. Note that t_N is measured from the moment the fault occurs and not from the moment the current starts to rise at the CB. Equation (9) is valid assuming zero attenuation of travelling waves in the cable. However, practically the resistance up to the fault location (including fault resistance) significantly attenuates the travelling waves and thus, reduces the rate of rise of current.

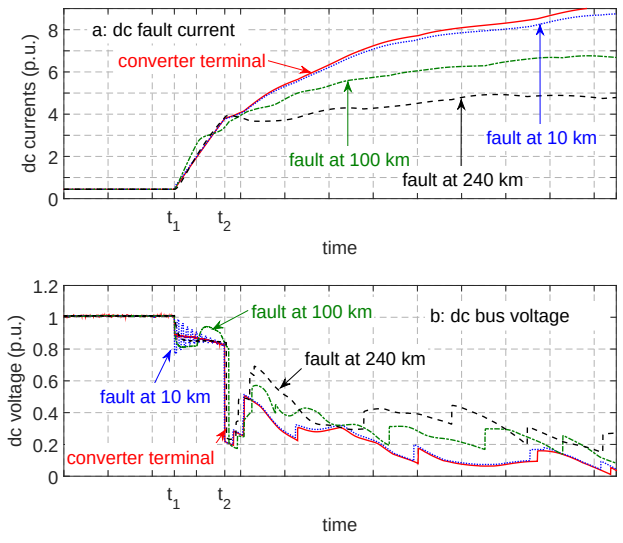

Fig. 8. Impact of distance of fault location from a converter. a: fault currents b: dc bus voltage

Furthermore, considering the ac in-feed period, the longer the distance of a fault from a converter the higher the dc side impedance. Besides, during this period, the travelling waves could significantly be damped out. Therefore, during ac in-feed period, a fault at a converter terminal results in large ac in-feed current. This can be observed from Fig. 8a where a fault at converter terminal has the highest magnitude after t_2. Moreover, assuming the same dc current limiting reactor is used, a fault at a converter terminal results in large current for OHL interconnected systems. This is because of the inductive nature of OHLs which limits the rate of rise of current. In general, considering a state-of-the-art HVDC CBs which require operation time of at least *2-3 ms*, a fault at a converter terminal for any case results in the highest average rate of rise of current in this period.

V. DC FAULT CURRENT INTERRUPTION

All fault clearing strategies by HVDC CBs that have been developed are based on the creation of a current zero through the normal current path by employing one or more parallel current paths as illustrated in Fig. 9 [8].

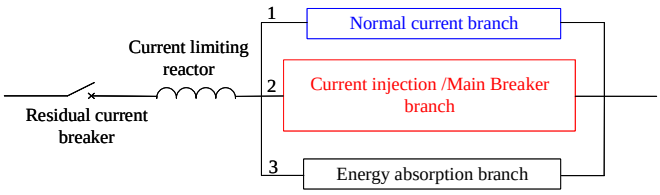

Fig. 9. Generic model of HVDC circuit breaker

An HVDC CB must fulfil the following basic conditions to successfully interrupt a dc fault current [32], [33].

1) Create a local current zero crossing for local interruption
2) Build up a counter voltage higher than the system nominal voltage to drive fault current to zero. This voltage is also referred to as transient interruption voltage (TIV)
3) Gain sufficient dielectric strength to withstand the voltage across its terminals during interruption process as well as the response from the network at later stage
4) Dissipate magnetic energy in the circuit inductance

Nowadays two different concepts of HVDC CB are promising for application in MT-HVDC networks. The first is the hybrid between power electronic and mechanical switches [3]–[5]. The second concept is the active current injection HVDC CB which consists of one or more mechanical interrupter(s) in the normal current branch [6], [7]. The latter employs a pre-charged capacitor in series with an inductor to inject a counter current to create a local current zero through the mechanical interrupter in the normal current branch of Fig. 9.

Fig. 10a shows the current interruption process by active current injection HVDC CB together with the associated stresses during current interruption. A fault occurs at t_1 and the counter current is injected at t_4. A fault neutralization time of *9 ms* is assumed in the simulation. In order to limit the fault

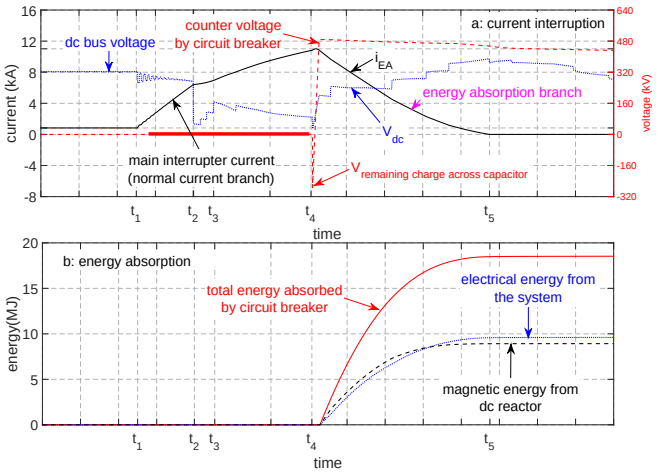

Fig. 10. Stresses on active current injection HVDC CB. a: current through and voltage across the CB during interruption, b: energy absorbed by CB

current to less than 16 kA over this period a *150 mH* dc current limiting reactor is used at the ends of each cable.

For any kind of HVDC CB, the energy absorption branch consists of several parallel stacks of metal oxide surge arresters (MOSA) designed to clamp the peak TIV as well as for the absorption of the system inductive energy. Fig. 10b shows the total energy absorbed by the surge arrester of the active injection CB. Depending on the size of current limiting reactor, the magnitude of the interrupted fault current and the voltage of the system during interruption, up to several tens of MJ of energy needs to be absorbed. In this case *18.5 MJ* of energy is absorbed by a CB while interrupting *11 kA*.

The total absorbed energy is further decomposed into two sources; namely, the magnetic energy stored in the dc current limiting reactor at the corresponding CB and the energy coming from the remaining part of the system. Note that the energy stored in the dc current limiting reactor at the beginning of the energy dissipation phase is $\frac{1}{2}Li_p^2$ and the curve in the Fig. 10b depict the dissipation of this energy is over the fault suppression period. Another noteworthy difference between ac and dc CBs is that in dc current interruption the system voltage recovers not at the end of the current interruption process but rather the moment the CB generates the counter voltage (at t_4 in Fig. 10a). In other words, the system voltage starts to recover at the beginning of the energy absorption phase of the interruption process while the interrupted current is at its peak. The total energy that a CB must absorb is given as,

$$E_{total} = \frac{1}{2}Li_p^2 + \int_{t_4}^{t_5} V_{dc} i_{EA} dt \qquad (10)$$

Where L is the current limiting reactor, i_p is the peak value of the interrupted current and, i_{EA} and V_{dc} are current through the breaker and the dc bus voltage, respectively, during energy absorption period ($t_4 - t_5$ in Fig.10a). Thus, it is not only the system magnetic energy that the CB must absorb but also the electrical energy supplied from a system during the fault current suppression period. The latter comes inevitably since the breaker requires some time to dissipate the magnetic energy in the reactor, with the duration depending on size of current limiting reactor as well as the difference between the counter voltage generated by circuit breaker and the dc bus voltage [8]. Due to the system voltage recovery during the energy dissipation phase, the energy coming from the grid in this case is even larger than the energy stored in the dc current limiting reactors (see Fig. 10b).

In reference [8] various test circuits are evaluated with respect to the current, voltage and energy stresses they provide to the HVDC CB. It is shown that beside producing sufficient short-circuit current, a test circuit having adequate voltage supply during energy absorption phase of the interruption process can provide the necessary stresses required for testing HVDC CBs. The reason for having voltage supply during this period is to compensate for the energy coming from the system as in the practical operation shown in Fig. 10. Moreover, as the faulty line is isolated by the CBs, the remaining part of the system continues to operate normally. Hence, after current interruption, the HVDC CB is subjected to dielectric stress of the system voltage.

Summarizing the above discussion, the key design parameters that need to be verified by a test are:

1) Capability to create a local current zero without re-strike/breakdown of mechanical switches/interrupters or thermal overload of power electronic components at the rated dc fault current interruption capability
2) The maximum current the breaker can interrupt within the breaker operation time
3) Generation of sufficient counter voltage to initiate fault current suppression
4) Capability of energy absorption components to absorb energy during fault current suppression. Depending on the rated sequence, this capability must be demonstrated several times within a defined sequence.
5) Capability to withstand the rated dc voltage for a certain duration after the interruption process
6) Dielectric withstand to ground, also during incident of superimposed travelling waves

The number of interruption operations that the CB can perform before thermal run away occurs on its surge arresters as well as the interruption intervals need to be defined, e.g. like auto re-closure in ac CBs. In addition, test duties similar to the standard duties for ac CB have to be defined.

In order to adequately verify these requirements of a circuit breaker, a test needs to fulfill the following conditions:

1) Produce sufficient short-circuit current that has adequate d*i*/d*t*; thus, within the operation time of a CB $(t_1 - t_4)$, a current must rise to peak interruption capability of a circuit breaker. For instance, in this case up to *11 kA*.
2) Supply sufficient energy stress as in service. For this a test needs to provide the energy equivalent to the energy stored in a current limiting reactor as well as the energy supplied by the rest of the system.
3) After successful current interruption by a CB, a test must ensure sufficient voltage stress equivalent to the rated system voltage

VI. CONCLUSION

The paper showed the temporal development of fault currents in multi-terminal HVDC network environment. Simula-

tions are performed by putting dc current limiting reactors at the ends of each cables assuming the maximum current breaking capabilities of the state-of-the art HVDC CBs. The major events during fault current build up are discussed in three distinct periods. During the sub-module capacitor discharge period, the fault current is mainly supplied by the converter directly connected to the dc bus. During the arm current decay period, the discharge from other feeders connected to the dc bus becomes prominent. The strength of the ac grid and the impedance of the converter transformer become critical during the ac in-feed period. The overall current through a CB on a faulted cable increases with the number of cables connected to the dc bus. It also concluded that considering the operation time of the recently proposed HVDC CBs, a fault close to (at) a converter terminal with multiple connections, results in the largest interruption current.

In order to study the stresses on HVDC CBs, fault current interruption is performed using models HVDC CBs inserted in series with the dc current limiting reactors. Proper size of dc current limiting reactor can reduce the fault current to within interruption capability of the CB. However, the HVDC CB is stressed with the duty to absorb the energy in the reactor. While the energy in the reactor is being absorbed the system voltage recovers and this introduces additional energy to be absorbed by the breaker. The paper shows that even more than the energy stored in the current limiting reactor is coming from the rest of the system. Therefore, a test needs to produce sufficient short-circuit current with adequate di/dt; that, within the operation time of a CB, rises to the peak interruption capability of a circuit breaker. It is also necessary to supply sufficient energy stress as in service. For this a test needs to provide the energy equivalent to the energy stored in a current limiting reactor as well as the energy supplied by the rest of the system. Finally, after successful current interruption by a CB, a test must ensure sufficient voltage stress equivalent to the rated system voltage

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