PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

D10.1: Test Report Describing Correct Functioning of Test Circuits

PROMOTioN – Progress on Meshed HVDC Offshore Transmission Networks
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LIST OF CONTRIBUTORS

Work Package and deliverable involve a large number of partners and contributors. The names of the partners, who contributed to the present deliverable, are presented in the following table.

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CONTENT

EXECUTIVE SUMMARY

The activities in Work package 10 (WP10) continue from the works in WP5. In WP5 several studies have been conducted ranging from system studies for determining the stresses on HVDC circuit breakers and their interaction with the system to designing and implemention of a test circuit supported by simulation and verification in a test laboratory. The next logical step in the design and verification of a test circuit is to test the implemented test circuit with real test objects, prototypes of HVDC circuit breakers. Thus, the main objective of this task is to verify the correct functioning of test circuit as wel as the HVDC circuit breakers of various technologies.

Hence, in this report prototypes of two candidate HVDC circuit breaker technologies are demonstrated and test results under application of full power and voltage are presented. The first prototype demonstrated is an active current injection HVDC circuit breaker with the peak TIV of 125 kV whereas the second prototype demonstrated is the voltage source (VSC) assisted resonance DC circuit breaker (VARC) with a peak TIV of 40 kV. Before the actual test, the procedures/steps required to calibrate the correct parameters of a test circuit and the different test duties intended for demonstration of the performance of HVDC circuit breakers while interrupting different current levels are defined and tests are performed accordingly.

The complete short-circuit current interruption test involves not only the current interruption in the main interrupter and suppression by the energy absorbing branch, but also post current interruption DC voltage stress. In some cases, particularly for the HVDC circuit breaker technologies having power electronic components in the nominal current path, pre-conditioning of the test object as in practical operation might also be needed. Thus, the test environment shall fulfil these features during the actual test. In addition, in this report, fine tuning of the control and operation of a test circuit as well as other functionalities such as over-current protection and arcing time prolongation and application of DC voltage stress after current interruption are performed under high-power conditions. The results demonstrate the validity and readiness of the complete test circuit for use. Besides the correct functioning of test circuits, tests intended for controlling different energy absorption of the test breakers are performed. Test results showing the performance of the test circuit as well as the tested breakers are provided and discussed in detail.

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1 INTRODUCTION

1.1 PURPOSE

Several manufacturers have developed prototypes of HVDC circuit breakers based on different DC current interruption principles and verified the functionalities of these prototypes in their own test labs as part of product development. The next step is the demonstration of the performance of these technologies at an independent and accredited test facility. In order to verify the performance of these devices it is necessary to supply the rated stresses as it would happen in practical operation. For this purpose, a test environment capable of providing complete and realistic (rated) stresses is essential. In the preceding works in PROMOTioN project (Work Package 5), various candidate test methods and test circuits have been compared and evaluated with respect to their capability as well as availability for testing HVDC circuit breakers. Theoretically, several test circuits can be designed to provide the necessary stresses to the HVDC circuit breaker. However, in practice, there are several challenges (some of which are unique to testing HVDC circuit breaker) that the actual test environment must meet to be able to successfully demonstrate the performance of HVDC circuit breaker under real power condition.

Some of the main challenges are described in detail below,

i. **Supply of rated stresses** – The rated stresses on HVDC circuit breaker during current interruption process are current, energy and voltage.
   - **Current:** within the breaker operation time, the test environment should be able to supply various values of current ranging from nominal (load) current to the maximum interruption capability of the various technologies of HVDC circuit breakers, as defined in test-duties. In other words, current with proper rate-of-rise and magnitiude is essential.
   - **Energy:** This is one of the unique features/functionalities of HVDC circuit breaker compared to, for example, HVAC circuit breakers. The HVDC circuit breaker needs to absorb the system's magnetic energy during DC current interruption. Hence, during testing, sufficient energy supply in the form of magnetic energy in the circuit inductance as well as the energy from power source (while the energy in the inductance is being absorbed) is necessary. Here, it must be noted that while energy is being absorbed by the energy absorber part (specifically the MOSA) of HVDC circuit breaker, the other components in the parallel paths, for example, vacuum interrupter, ultra-fast disconnector, power electronics in the main breaker part, etc. are subjected to the TIV stress that the circuit breaker maintains during fault current suppression.
   - **Voltage:** the other necessary requirement is the supply of voltage during both current interruption process as well as after current interruption. From the test circuit perspective, the HVDC circuit breaker sees only the DC voltage supplied from the test circuit after current interruption. However, the short-circuit power source should maintain its voltage during the entire the current interruption period. This is needed to obtain the test current at a desired rate-of-rise (during fault neutralization period) and the

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desired energy (during fault suppression period)[1]. Finally, the DC voltage stress after current interruption can be supplied from an additional voltage source if the short-circuit power source cannot provide which is the case for AC short-circuit based test circuit.

ii. **Withstand the voltage stress by the test breaker –** the other unique feature/functionality of HVDC circuit breaker is that it produces its own transient interruption voltage (TIV) during the current interruption process. In order to suppress the fault current, the HVDC circuit breaker must produce the voltage higher than the source voltage supplying the fault current which in real application is the system voltage. This voltage stress is seen by internal components of the HVDC circuit breaker as well as by the test installation. Thus, the test installation must be able to handle the stress coming from the test breaker. Especially, as the rated voltage of the HVDC circuit breaker increase, the TIV that it needs to produce increases making the test installation susceptible to even higher voltage. In other words, as the rated voltage of the HVDC circuit breaker increases the challenge of testing these devices becomes two-fold; one providing the desired stresses at the increased rating and the other is the increased TIV stress on the test installation.

Among the candidate test circuits evaluated in deliverable D5.6, the test circuit based AC short-circuit generators is readily available for use and have sufficient flexibility to supply the desired stresses to different technologies of HVDC circuit breakers. Therefore, the test circuit in this document refers to the test circuit based on AC short-circuit generators.

In this task the capability of a test environment to deal with the above requirements is practically verified by testing the prototypes of two different technologies HVDC circuit breakers. Therefore, while the correct functioning of the test circuit is verified the performance of the prototypes of HVDC circuit breakers is also demonstrated. With the measurements of current and voltage as well as operation times of the prototype circuit breakers, the provision of the necessary stresses is verified.

1.2 MOTIVATION

Increase in technology readiness level (TRL) of HVDC circuit breaker technologies by demonstrating their performance with proper and adequate test environment is one of the main objectives of the PROMOTioN project. This is achieved by demonstrating the performances of various technologies of HVDC circuit breakers. For this purpose, three different technologies of HVDC circuit breakers by three manufacturers within the project consortium will be demonstrated. Before demonstrating the performances of these technologies, there are other important steps such as definition of realistic test requirements, test procedure as well as criteria for evaluation of test results which have been qualitatively addressed in work package 5.

[1] In some cases, the test may be perfomed at lower energy absorption. In that case the source voltage must reduce proportionally to limit the energy. The short-circuit current can be interrupted as long as the breaker under test produces TIV higher than the source voltage. However, the TIV must always be compared with the rated voltage of the breaker with not the source voltage driving the circuit and it must be higher than the rated voltage with sufficient margin.

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1.3 DOCUMENT STRUCTURE

The remaining part of this document is organized as follows. In chapter 2, description of test environment is provided. In addition to supplying the test current, voltage and energy to the test object, successful demonstration of some special features of a test circuit needed for testing different technologies of HVDC circuit breaker are presented in detail. Chapter 3 discusses demonstration of a test circuit together with HVDC circuit breaker. Prototypes of two different technologies of HVDC circuit breakers are demonstrated and their corresponding test results are presented. Finally, Chapter 4 summarizes the discussion of this document.

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2 DESCRIPTION OF TEST ENVIRONMENT

2.1 INTRODUCTION

In deliverable D5.7, “realization of test environment for HVDC circuit-breakers” is discussed in detail. The functions of various parts of a test circuit based on AC short-circuit generators have been described and some example cases have been demonstrated in a test laboratory. First, considering various technologies of HVDC circuit breakers, the supply of prospective current at different rate-of-rise is verified assuming a range of rated voltages. This was performed considering hybrid HVDC circuit breaker with breaker operation time in the range of 2-3 ms and active current injection HVDC circuit breaker with breaker operation time in the range of 8-10 ms. Moreover, a few example cases showing the maximum capabilities of the test facility considering various technologies of HVDC circuit breakers at different voltage ratings have been demonstrated. It was shown that the capability of a test facility with respect to testing HVDC circuit breakers depends considerably on circuit breaker parameters, such as breaker operation time, maximum current interruption, energy dissipation, etc. In addition, the expected performance of the HVDC circuit breakers when interrupting the demonstrated prospective currents is then supplemented with simulation results using software models of HVDC circuit breakers taking into account realistic parameters. Moreover, other features of a test circuit such as protection of the test object as well as the test installation, application of DC voltage after current interruption, arcing time prolongation/initial current limitation are also verified at a full power level.

In the present task, the special features of a test circuit, the methods and functionalities mentioned above are optimized, some are combined and verified together in one go. The performance verifications with respect to supplying the needed stresses are performed under real test condition with prototype HVDC circuit breakers in the test circuit and this is discussed in Chapter 3. In this chapter the complete test circuit described in D5.7 is briefly reviewed and the functionalities of the test circuit demonstrated after submission of D5.7 are discussed in detail together with the test results.

2.2 TEST CIRCUIT SUPPLIED BY AC SHORT-CIRCUIT GENERATORS

The complete test circuit consisting of power source, over-current protection, arcing time prolongation and DC voltage application circuits is shown in Figure 2-1.

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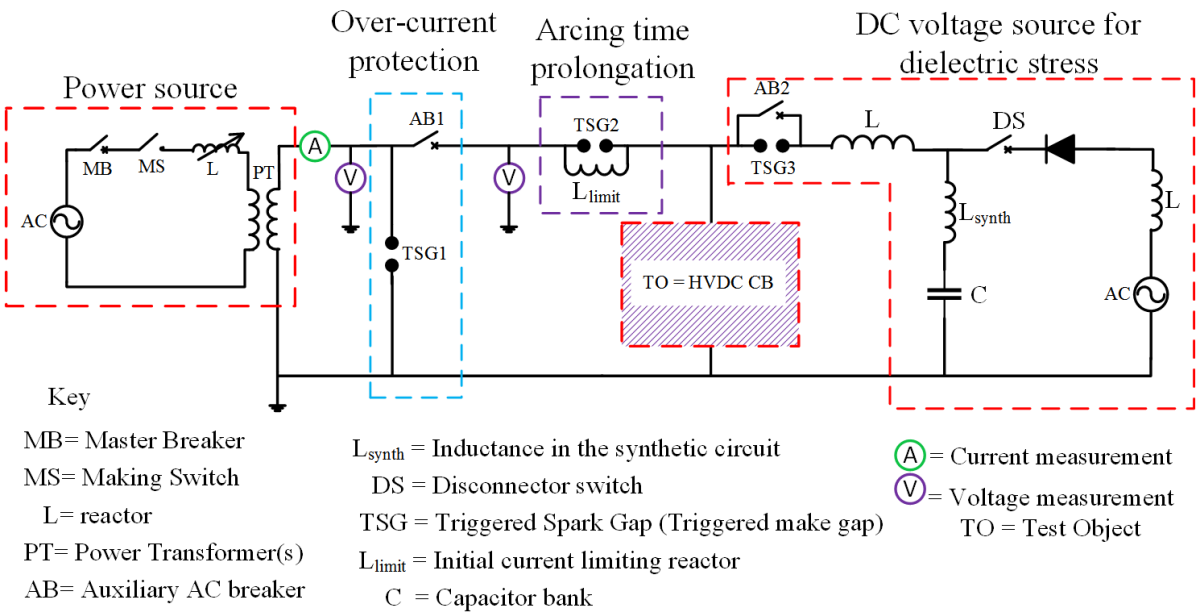

Figure 2-1: Complete Test Circuit for HVDC Circuit breaker testing (Designed and implemented in WP5, D5.7)

2.2.1 POWER SOURCE

This is the part supplying the short-circuit power during a test. Depending on the rating of the test object and the stresses required, several short-circuit generators and step-up transformers might be used.

When testing HVDC circuit breakers using AC short-circuit generators, only single-phase supply is needed. A typical connection of six generators in parallel and two parallel sets of five series connected step-up transformers is shown in Figure 2-2.

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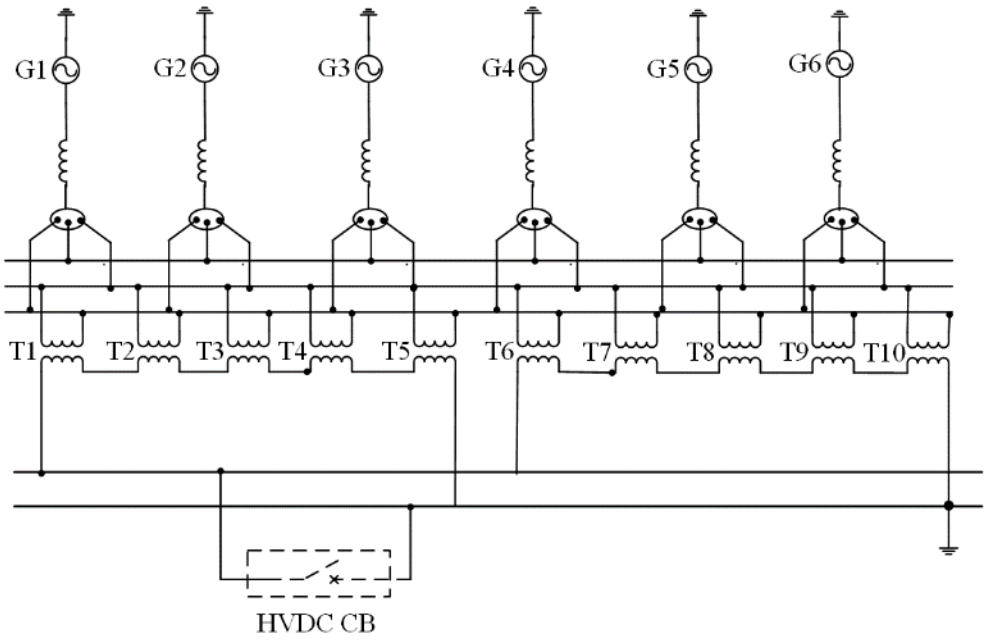

Figure 2-2: Schematic of power source part of the test circuit. It shows a possible connection of generators (G1-6) and transformers (T1-10)

2.3 ARCING TIME PROLONGATION AND OVER-CURRENT PROTECTION

The proof of concept for this method was performed in D5.7. However, in this section the experimental verification considering the exact test circuit to be used during the actual test later in the project is conducted. This significantly increases the level of confidence of the validity this method during the actual test. In addition, arcing time prolongation is demonstrated in combination with over-current protection and the test results are described in this section.

Referring to Figure 2-1, during the actual test of the HVDC circuit breaker, the auxiliary breaker AB1 (245 kV, 63 kA, SF_6 AC CB) is tripped simultaneously (or in some cases even before tripping the HVDC circuit breaker) with the test object in order to provide galvanic isolation between the power source and the test object just after current suppression. This galvanic isolation is needed for the application of DC voltage from another source (since the AC short-circuit generators cannot provide DC voltage) to the test object while avoiding interaction between the two sources. In some cases, depending on the test object as well as on the resulting voltage difference between the two sources, the AB1 may not have sufficient arcing time to provide the needed isolation. This is especially the case when the entire current interruption time by HVDC circuit breaker is short compared to the minimum arcing time of the AB1.

Hence, in the test circuit using AC short-circuit generators, a method to gain additional arcing time for the AB1 is proposed and verified in a test laboratory. The circuitry used for this purpose is shown in Figure 2-3 as the dashed box labelled as arcing time prolongation (see also Figure 2-1). As can be seen from the figures, the

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arcing time prolongation circuit consists of a current limiting reactor in parallel with a plasma triggered spark gap, TSG2.

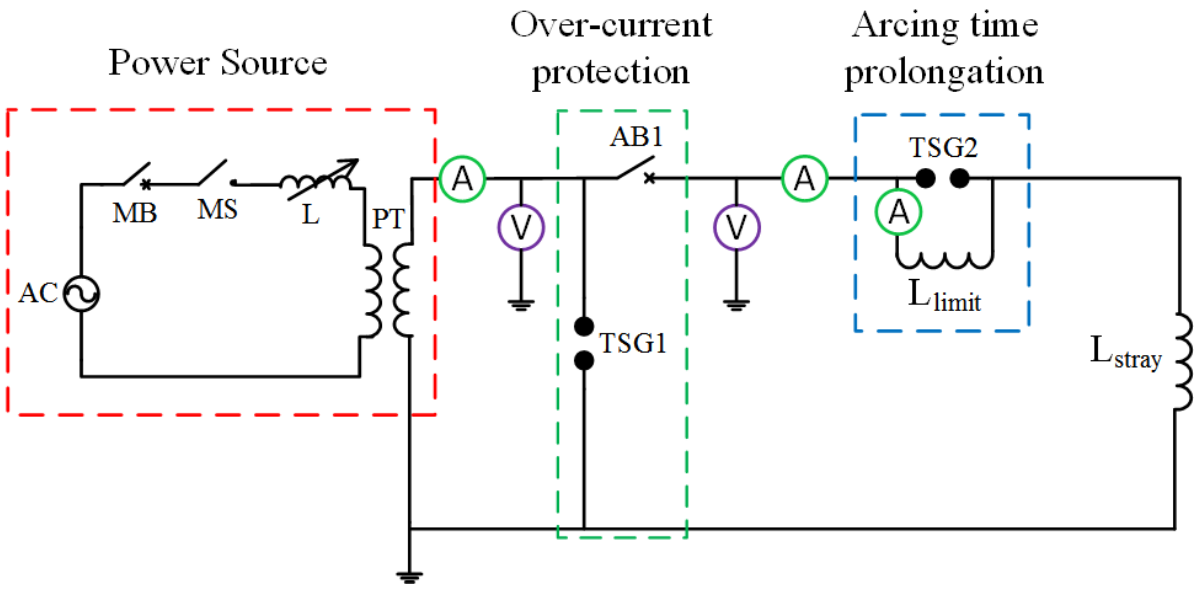

Figure 2-3: Schematic diagram of arcing time prolongation test circuit combined with over-current protection

The function and operation of the arcing time prolongation circuit is described as follows. Initially the short-circuit current flows through the current limiting reactor which forms a series connection with the test object (not shown in Figure 2-3). The current limiting reactor ensures a reduced current flow through the test object during this initial period. It must be noted that the making angle by the making switch (MS) is now reduced or even could 0º (measured from voltage zero crossing) to obtain maximum fault current asymmetry. The choice of the initial making angle depends on several factors such as the minimum arcing time of AB1, the total current interruption duration of the test object as well as on the power frequency. Later, the actual/desired making angle for the test object is realized by the triggering TSG2. Thus, when the desired making angle (the point on voltage wave at which the desired di/dt for the test object can be achieved) is reached, the TSG2 is fired. This bypasses the current limiting reactor and the short-circuit current flows through TSG2 at the desired di/dt needed for the test object. The current limiting reactor can be dimensioned in such a way that the initial current reaches the nominal (load current) just before the moment of bypass by TSG2.

The arcing time prolongation is demonstrated in the test laboratory with test circuit realized as shown in Figure 2-4 and Figure 2-5. As can be seen from the figures, three current limiting reactors (each with maximum inductance of 162 mH each of which has several taps) are connected in parallel. Although it was possible to obtain the desired current limiting inductance value with a single reactor, the arrangement shown in the figure was chosen for safety purpose. That is in case there is a failure to bypass the reactor and/or if the gap does not become conductive for whatever reason, the resulting current exceeds the maximum current carrying capability of the reactor. Thus, three parallel reactors, with taps adjusted to achieve the desired equivalent reactance, are used for sharing the prospective current if TSG2 fails to operate as desired.

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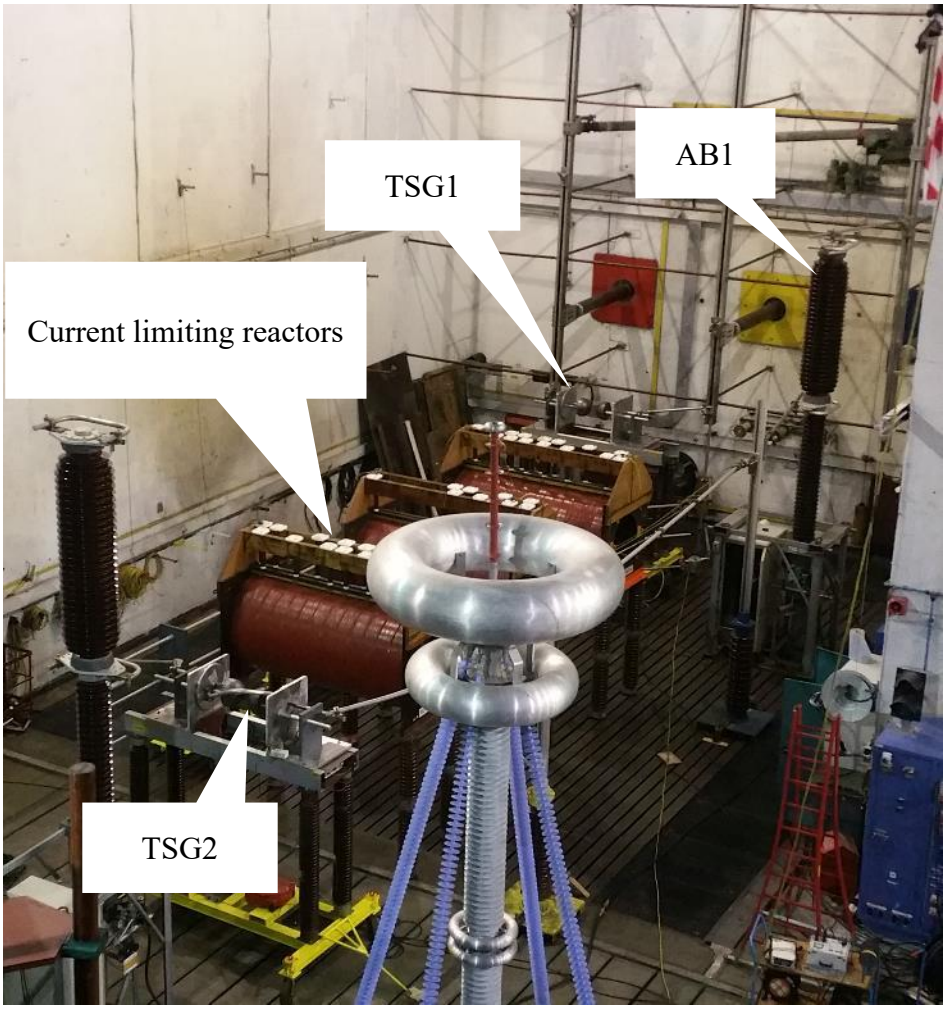

Figure 2-4: Test set-up for arcing time prolongation (over-current protection is also demonstrated in combination)

The test circuit parameters (desired making angle, circuit inductance, etc.) are adjusted first by short-circuiting the TSG2 as can be seen in Figure 2-4.

Figure 2-6 shows test result demonstrating the method of auxiliary breaker arcing time prolongation. The test is performed with short-circuit generators running at 30 Hz. The making switches (MS), see Figure 2-3, are closed at about 1 ms (11^0, electrical) after voltage zero. This will cause current to flow through AB1, current limiting reactors as well as a test object. After about 700 µs the contacts of the AB1 separate. To get contact separation of AB1 at this precise time, it is pre-triggered so that its contacts part after some current (larger than the chopping current of SF_6 AC circuit breaker) start to flow through it. In this case about 80 A current is flowing when the contacts of AB1 separate. This current is sufficient to establish arc between the contacts of the AB1.

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At this time, current continues to flow but at reduced rate-of-rise because of the current limiting reactor. After about 4 ms (determined based on the desired making angle for proper di/dt and breaker operation time), TSG2 is fired to bypass the short-circuit current from the current limiting reactor. At the moment of bypassing the current limiting reactor, 2.2 kA current is flowing through the test object path which can be considered as initial load current before inception of fault in practical application. However, the current limiting reactors remain charged (with 2.2 kA) and this current (ideally) circulates in the loop only between TSG2 and current limiting reactor. From this time on, the short-circuit generators supply the current to the test object through the TSG2. The desired test current with rate-of-rise of 5.5 kA/ms is obtained with additional 4 ms arcing time for AB1.The result is shown in Figure 2-6.

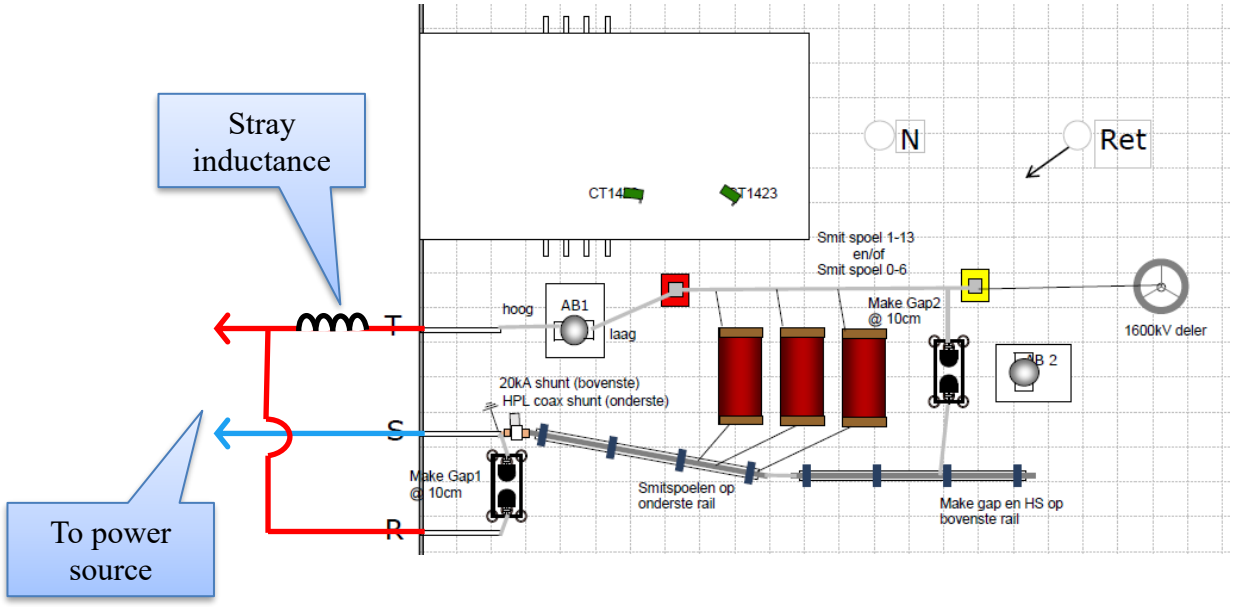

Figure 2-5: Schematic of the test circuit showing the actual connection in the test hall

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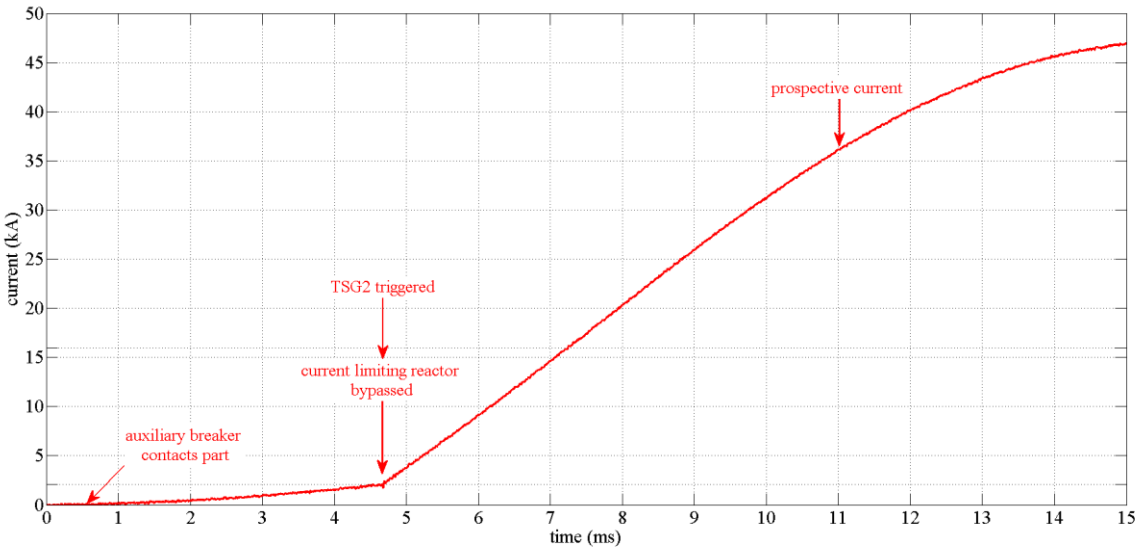

Figure 2-6: Demonstration of arcing time prolongation

It can be seen from the oscillogram in Figure 2-6 that the prospective current rises to a peak value of 47.5 kA if it is not interrupted by the test object. For instance, in this particular case the test object is expected to suppress the short-circuit current when it reaches 16 kA and the interruption happens (obtained by simulation using model of hybrid HVDC circuit breaker) as shown by red dashed trace in Figure 2-7. Now, if the test object fails to clear or to operate, not only the test object is subjected to a large and long duration prospective current but also the auxiliary breaker is subjected to long arcing time. Especially when the test is performed at low power frequency the duration of the short-circuit current could be as long as 30-50 ms. This may result in the considerable wear/damage of arcing contacts of the auxiliary breaker. For this reason, it is always necessary to ensure that the current is bypassed to another path in the case a failure of the test object (current above certain threshold) is detected. This is demonstrated in Figure 2-7. In this figure the demonstration of arcing time prolongation is combined with over-current protection. Thus, the TSG1 (see Figure 2-3) triggered when current threshold of 19 kA is exceeded. For this functionality, a real-time current level detector that can monitor current (real time) and produce firing signal upon detection of threshold value is developed. It can be seen from Figure 2-7 that the moment TSG1 is fired, the current starts to commutate from the test object path (see the blue trace in Figure 2-7) to TSG1 bypass path (see the black trace in Figure 2-7). Thus, in this way unnecessary long arcing of the AB1 as well as long duration large current flow through the test object is avoided.

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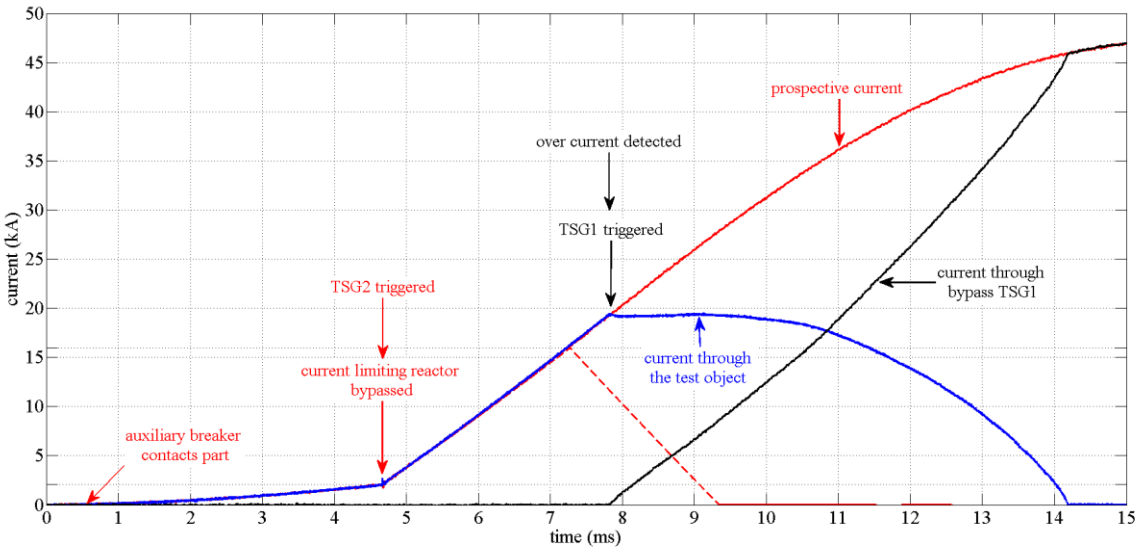

Figure 2-7: Demonstration of arcing time prolongation combined with over-current protection simultaneously

The current commutation from the test object path to the TSG1 is taking relatively long time due to stray inductance (in the order of 100 µH) because of long loop length between the two paths in the realized test circuit, see Figure 2-5.

2.4 DC VOLTAGE STRESS APPLICATION

The other important aspect of a test circuit for HVDC circuit breaker is the provision of DC voltage stress after current interruption. In real application, the HVDC circuit breaker is subjected to system voltage after current interruption. However, during testing, a test circuit supplied by AC short-circuit generators cannot provide DC voltage stress after current interruption. Therefore, this stress should be supplied by an additional source such as a charged capacitor as shown in Figure 2-1 with a circuit labelled as DC voltage source for dielectric stress. The main challenge, however, is how to determine when to apply this voltage stress and how to ensure the test object is subjected to this voltage for the desired duration.

In D5.7 a proof of concept of the method of applying dielectric DC voltage stress was conducted based on timer signal. i.e. injecting DC voltage at specified time. DC voltage application based on timer signal may not be accurate enough as the moment of current zero (duration of current suppression period) cannot not be precisely predicted. Also, the method based on timer signal does not prevent the application of DC voltage when the test object fails to clear as there is no point of doing this when the short-circuit current is still flowing. In this section the DC voltage injection upon current zero detection is described along with tests results.

To demonstrate the application of DC voltage stress, a test circuit is set-up in a laboratory with circuit diagram shown Figure 2-8. The principal idea is based on the fact that the HVDC circuit breakers have internal capacitors which is charged to the same voltage as the TIV of the HVDC circuit breakers. This capacitor is

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designated by C1 in Figure 2-8. The dielectric voltage is applied by creating electrical interaction due to voltage difference between the capacitor of the test object (C1) and the capacitor of an external source (C2), see Figure 2-8.

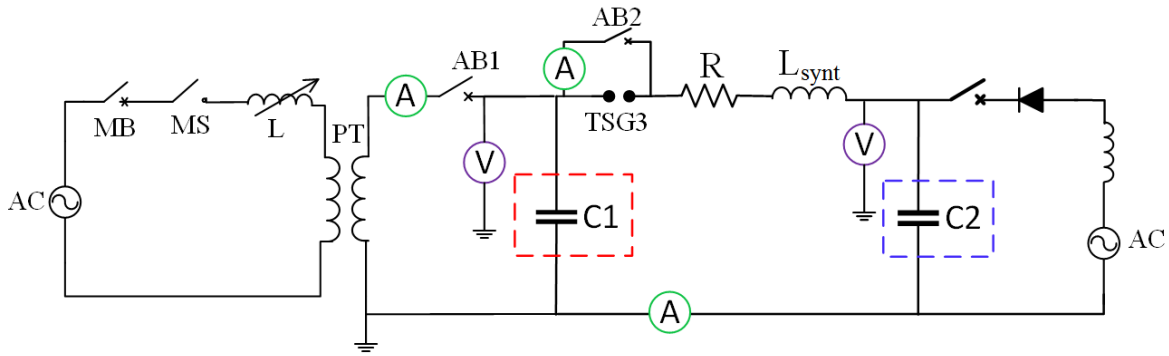

Figure 2-8: Test circuit for demonstrating DC voltage application to HVDC circuit breakers after current interruption

When the short-circuit current is suppressed by HVDC circuit breaker, the auxiliary breaker isolates the test object from the power source. This results in a trapped charge across the capacitor of the HVDC circuit breaker. When current zero is detected, TSG3 is fired which in turn initiates the charge balancing interaction between C1 and C2. This establishes an oscillating current through TSG3. In order to limit the oscillating current a large impedance (L_{synt}) is put between C1 and C2 as shown Figure 2-8. The magnitude of oscillating current in fact depends on the voltage difference between C1 and C2, the relative sizes of the capacitances, and the additional impedance between these two capacitors. Moreover, the interaction between these two capacitors exist as long as current is flowing through TSG3. In order to ensure DC voltage stress after current ceases to flow through TSG3 (which is the case after a short while), a parallel auxiliary breaker, AB2, see Figure 2-8, is closed.

The method to apply DC voltage after current interruption is demonstrated in the test laboratory using a test circuit realized as in Figure 2-10 and Figure 2-9. In order to mimic the situation during current interruption by HVDC circuit breaker, a capacitive AC current through C1 is interrupted by AB1. The objective here is to detect current zero following interruption and then triggering TSG3 to apply DC voltage from C2.

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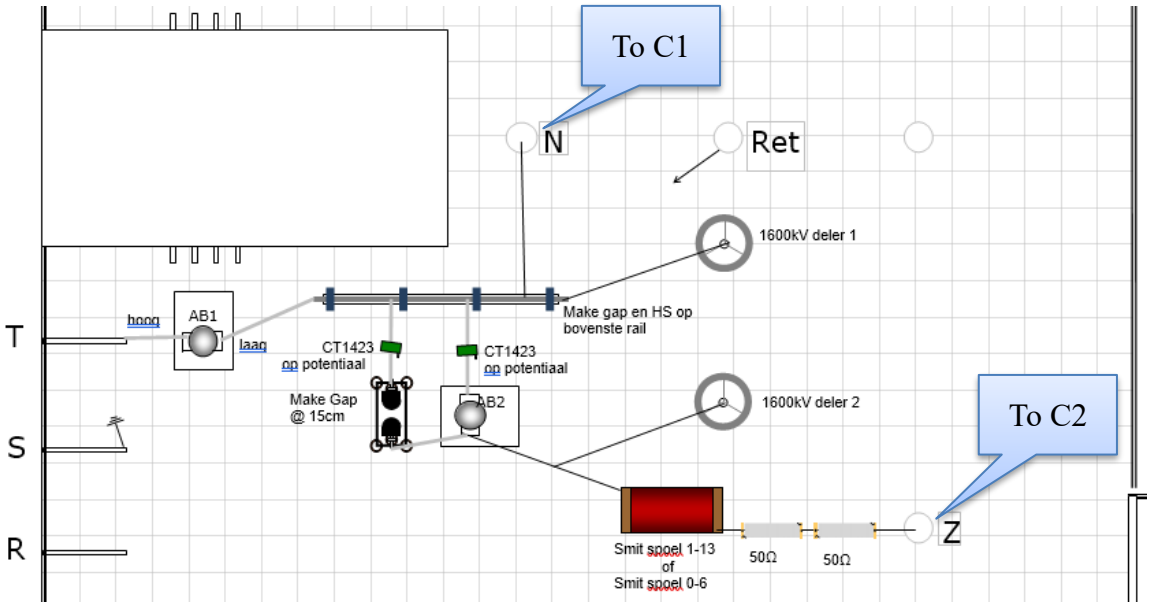

Figure 2-9: Diagram showing the actual connection in the test hall

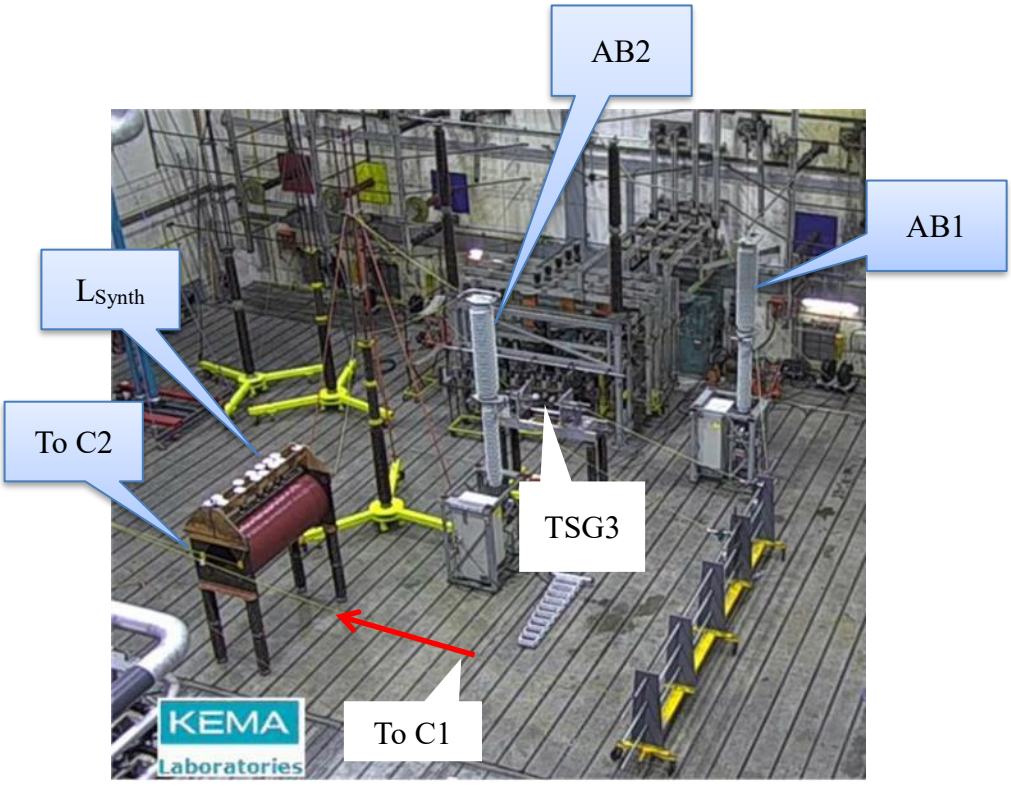

Figure 2-10: Test set-up for DC voltage application upon current zero detection

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Figure 2-11 shows test results of DC voltage application. First capacitive AC current of about 300 A (peak) supplied by short-circuit generators is established through capacitor C1, see the blue trace in the bottom graph of Figure 2-11. The auxiliary breaker AB1 is tripped with current interrupted at natural current zero. At current zero the capacitor C1 is charged to the peak value of the supply voltage which is 100 kV in this case, see the red trace in the top graph of Figure 2-11. This voltage corresponds to the TIV voltage of the HVDC circuit breaker due to trapped charge when AB1 isolates from the power source. Upon current interruption, a real-time current zero detector detects this interruption and fires the TSG3. Initially, the DC source capacitor is charged to 90 kV. Now, when TSG3 is fired current starts to flow between C1 and C3 because of their voltage differences. The current through TSG3 is shown by the red curve in the bottom graph of Figure 2-11. After a few milliseconds, AB3 which is in parallel to the TSG3 is closed to ensure that the DC stress after current is damped. Note that a damping resistance is also used between C1 and C2 to provide quick voltage balance to avoid oscillation of voltage.

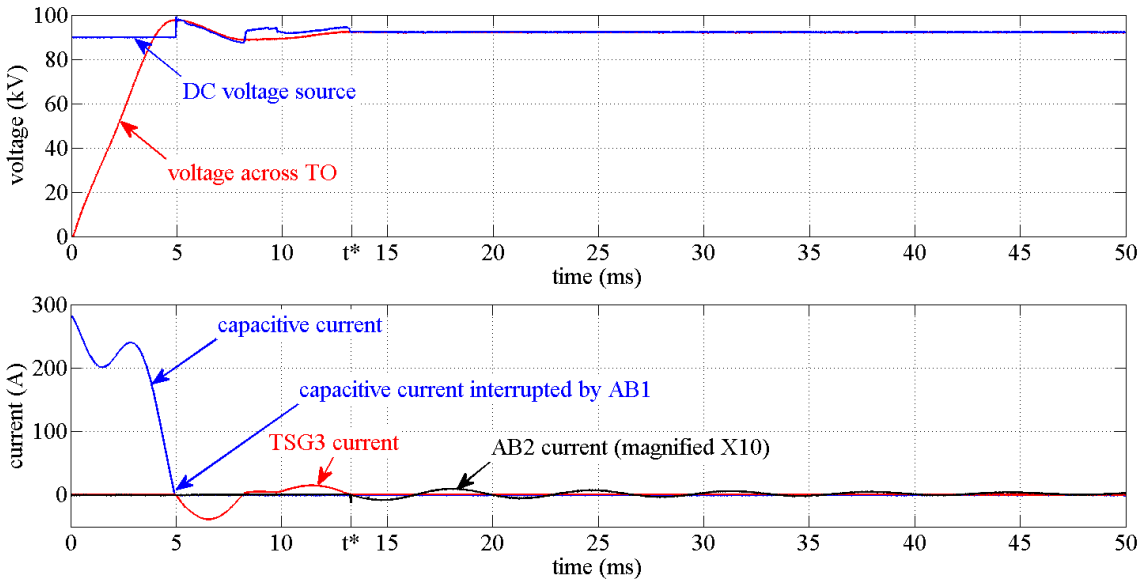

Figure 2-11: Demonstration of DC voltage application after current suppression by HVDC CB

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3 TEST CIRCUIT VERIFICATION – TESTING OF PROTOTYPE HVDC CIRCUIT BREAKERS

3.1 INTRODUCTION

Based on the designed test environment described in Chapter 2, tests have been performed on HVDC circuit breakers. The primary goal of the test is verification of performance of a test circuit. In addition, in this process the performance of the HVDC circuit breaker is tested. The focus of the chapter is on the results as evaluated with respect to the test environment.

3.2 TEST PROCEDURE

Before the actual current interruption test, two parts check procedures are performed. The first part is pre-test check of the test breaker. This is intended to make sure whether the test breaker is properly installed and the controls can be operated as desired. In addition, if the test breaker requires charging of its internal capacitor, this is performed as part of the test breaker preparation procedure. The second part is calibration of the test circuit i.e. to check and verify proper settings of test parameters and make necessary adjustments in case there is a deviation from the required test parameters. The procedures in the latter part are described briefly below.

3.2.1 TEST CIRCUIT PREPARATION PROCEDURE

After the test breaker is checked for its readiness, the test circuit components are adjusted and test parameters are verified. Depending on the desired test duty (the peak value of interrupted current), the breaker operation time and energy dissipation, the desired test circuit parameters are first, computed via simulation and/or analytical calculation. This results in the short-circuit power, the source voltage and hence the number and configuration of transformers, etc. needed for the test.

After the test circuit is prepared, fine tuning of test parameters are performed with actual measurements with the major steps and objectives illustrated below.

Step 1. Frequency verification

Verify the desired frequency of the short-circuit generators.

Step 2. Voltage verification

Adjust the excitation voltage of the generators so as to obtain the desired voltage at the test object after transformation.

Step 3. Current verification

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This is to make sure whether the desired symmetric current matches with the analytically computed impedance realized in the test circuit. The impedance calculated analytically (with simulation) is considering the combined impedance of the transformer(s), busbars, generator transient reactance and additional adjustable reactors. Thus, the desired current (impedance) is verified by making a short-circuit with the test object in a closed position (or by bypassing the test object). Fine tuning of the adjustable reactors might be necessary if there is significant deviation from the desired current.

Step 4. Making angle verification

Once the desired symmetric current is obtained, the making angle is adjusted to obtain the required current with its proper rate of rise. The making angles are realized by the making switches (MS) which close precisely at the desired point on voltage wave with a resolution of 3 electrical degrees. These switches are located on the low-voltage side (generator side), see Figure 2-1.

Step 5. Determine the timing of trip command timer for the test object

Part of the performance test of the HVDC circuit breaker is determining the minimum operation time (specifically breaker operation time). That is the time duration needed by the breaker from receiving the trip order until the start of fault current suppression.

Once the test current with the desired rate-of-rise is obtained (step 4), a timer signal for trip command to the test object is set as shown in Figure 3-1. This time is equivalent to the relay time of the protection system in the actual HVDC grid [1]. The reference time for the timer is the moment of short-circuit making or the time when the current starts to rise. This can be determined based on the breaker operation time and the time at which the desired value of a given duty current is achieved, see Figure 3-1. In the example shown in the figure, t_2 is the trip command timer set point.

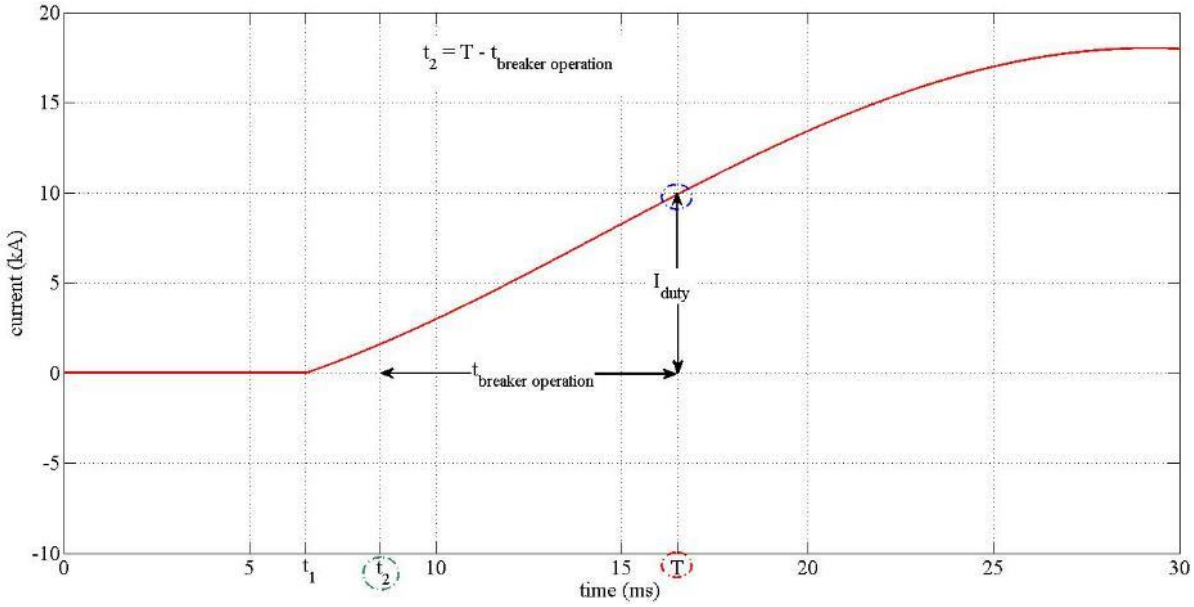

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Figure 3-1: Setting trip signal timer for HVDC circuit breaker testing

Step 6. Testing of the HVDC Circuit Breaker

Finally, the test is performed on HVDC circuit breaker. Bidirectional current interruption tests are performed by delaying the making angle (the point in time on the voltage wave at which the short-circuit is applied) by 180º (electrical degrees) while keeping the connection of the test object as well as its charging voltage polarity (if this is part of the test procedure) the same for all the cases. The same applies when testing different currents.

From the measurements of the test results, the following points to be noted after test

- The peak value of interrupted current
- The time from trip order until the peak interrupted current is reached (verification of breaker operation time)
- The TIV measurement
- Other measurements within the breaker (if necessary)
- Later the energy absorbed by the breaker is computed

3.3 ACTIVE CURRENT INJECTION HVDC CIRCUIT BREAKER

The active current injection HVDC CB is composed of a vacuum interrupter in the main current path and a parallel L-C circuit which is used to inject high-frequency counter current, see
Figure 3-2a. The current injection is controlled by a high-speed making switch which, when closed, results in a high-frequency (in the order of several kHz) as shown Figure 3-2b. The oscillation frequency and magnitude is determined by choice of passive components (reactor and pre-charged capacitor). The inverse current generates a current zero within the main interrupter, which can typically be achieved within 8 ms from trip order from the DC relay.

The topology can perform multiple operations in rapid succession if required (e.g. auto-reclosing function). This can be achieved by parallel connection of a second making switch and pre-charged capacitor, as shown by the dotted lines Figure 3-2a. After the first operation is performed, the first high-speed making switch (HSMS1) is left in the open position. HSMS2 and Cp2 are then used to inject a second counter-current.

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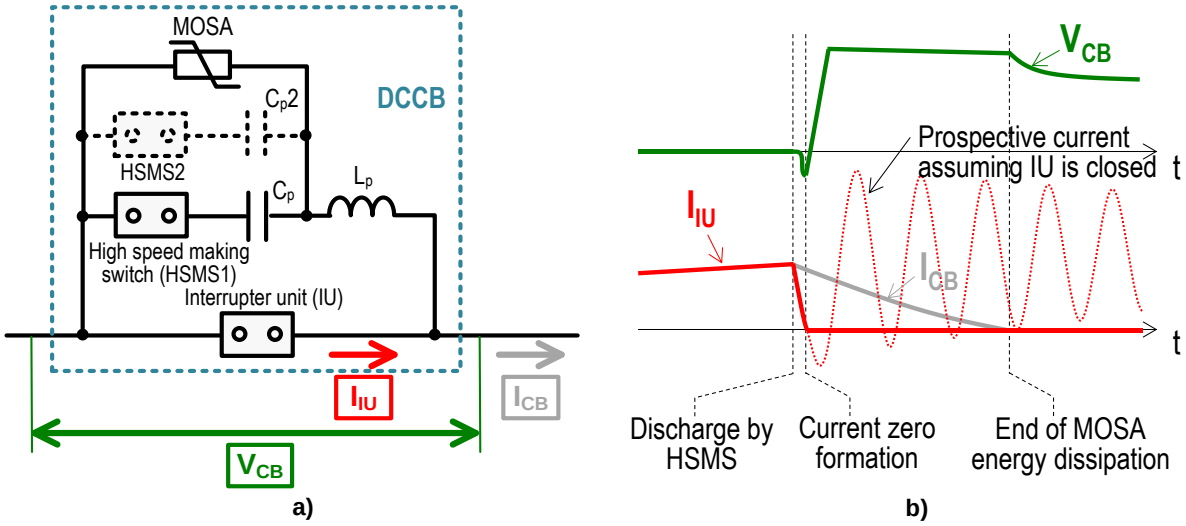

Figure 3-2: Schematic of circuit and waveform of active injection current zero creation scheme

3.3.1 TEST SET-UP

The test set-up of prototype active current injection HVDC circuit breaker in the laboratory's test hall is shown in Figure 3-3. The part of the prototype breaker includes the vacuum interrupter and the high-speed making switch both contained in the same tank, the metal oxide surge arrester (MOSA), the pre-charged current injection capacitors, current injection inductors as well as the control cubicle all of which are labelled in Figure 3-3. In addition, some parts of a test circuit such as the auxiliary breaker (AB1) and the over-current protection bypass triggered spark gap (TSG1) are shown. The current and voltage measurements can also be seen in the figure but not labelled for clarity purpose.

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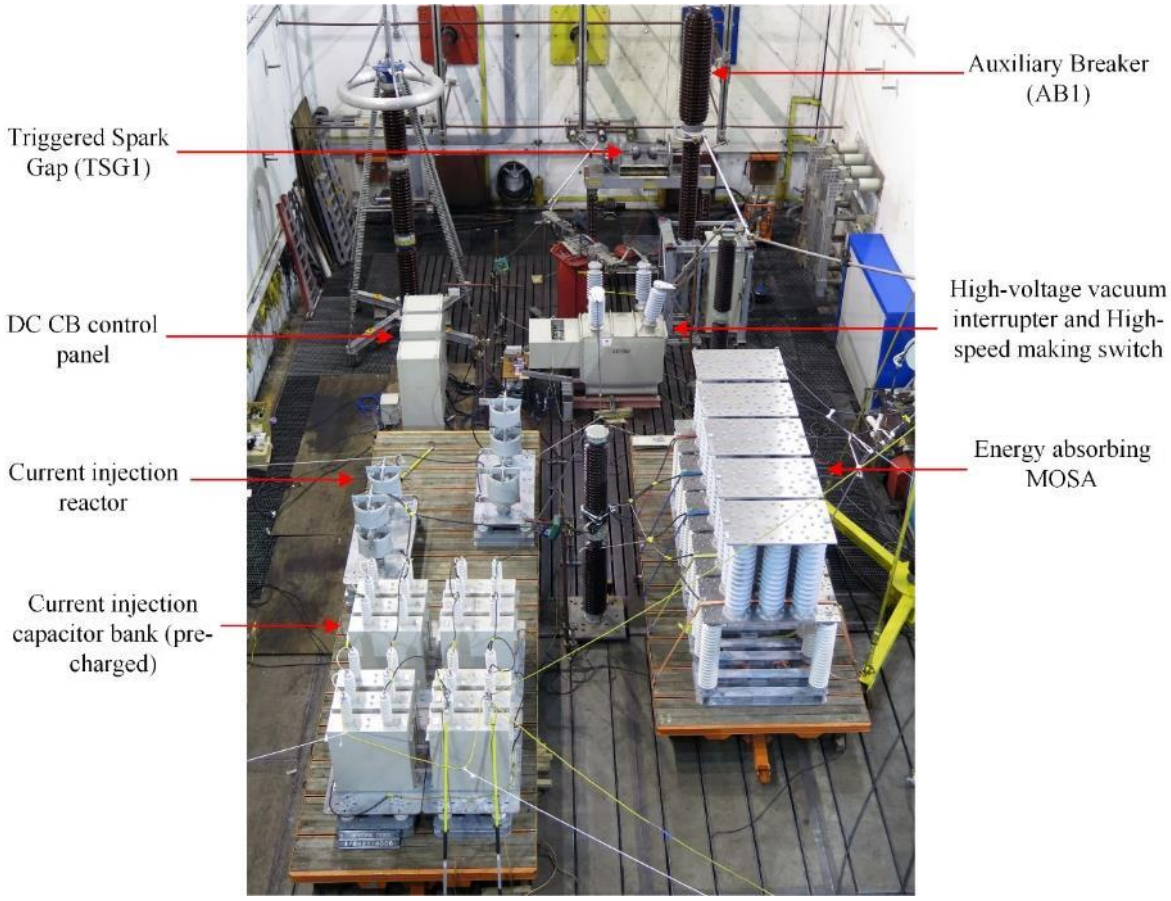

Figure 3-3: Test set-up of active current injection HVDC circuit breaker

3.3.2 TEST RESULTS [2]

In order to test the performance of the HVDC circuit breaker while interrupting different current magnitudes, four different test duties named as T100, T60, T30 and T10 (similar nomenclature as AC circuit breaker test duties) are defined with interruption currents as follows;

1. T100 – 16 kA interruption current
2. T60 – 10 kA interruption current
3. T30 – 5 kA interruption current
4. T10 – 2 kA interruption current

The test circuit is designed to provide the above current duties with proper rate-of-rise. For all the cases, a fault neutralization time (which includes breaker operation time and relay time) of 10 ms is assumed in the tests. It

[2] The pass or fail criteria in the following tests are that the test object suppresses the short-circuit current from the expected value (test duty current) to zero/leakage current level. In addition, that the test circuit provides the necessary stresses as desired (current with the desired rate of rise and energy as well as voltage (both during and after current interruption)). Thus, while generating the desired TIV and hence absorbing energy in the circuit.

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must be noted that the energy absorbed at each test duty does not exceed the maximum energy absorption capability of the test breaker. Initially, the test circuit is designed to supply energy not exceeding 1.5 MJ. In addition, for all the test duties the injection capacitor of the test object is charged to a voltage of 70 kV and the polarity remains the same when interrupting current both in the forward and reverse direction.

Figure 3-4 shows T100 (16 kA) current interruption both in the forward and reverse direction. Before current is interrupted prospective current is first verified. This is shown by dashed black traces in the figure. In both cases the prospective current rises to a value of 33.5 kA peak and 16 kA is reached at 10 ms after the moment of short circuit making. The breaker receives a trip command shortly after current starts to rise. It can be seen form Figure 3-4a and c that the prototype HVDC circuit breaker interrupts the short-circuit current from 16 kA. The local current interruption through the vacuum interrupter is also shown in these graphs, see the blue traces in Figure 3-4a and b. For reverse current interruption, it can be seen that the counter injection current is first superimposed on to the current through the vacuum interrupter during the first half cycle and current zero is created during next half cycle.

Figure 3-4b and d show the TIV generated by the HVDC circuit breaker during current suppression. The TIV rises from negative value (-25 kV) due to the remnant charge across the capacitor to 125 kV peak value. There is a high-frequency oscillation at the peak of TIV due to stray elements in the circuit. The circuit breaker maintains a steady TIV of about 110 kV after the high-frequency transient has decayed.

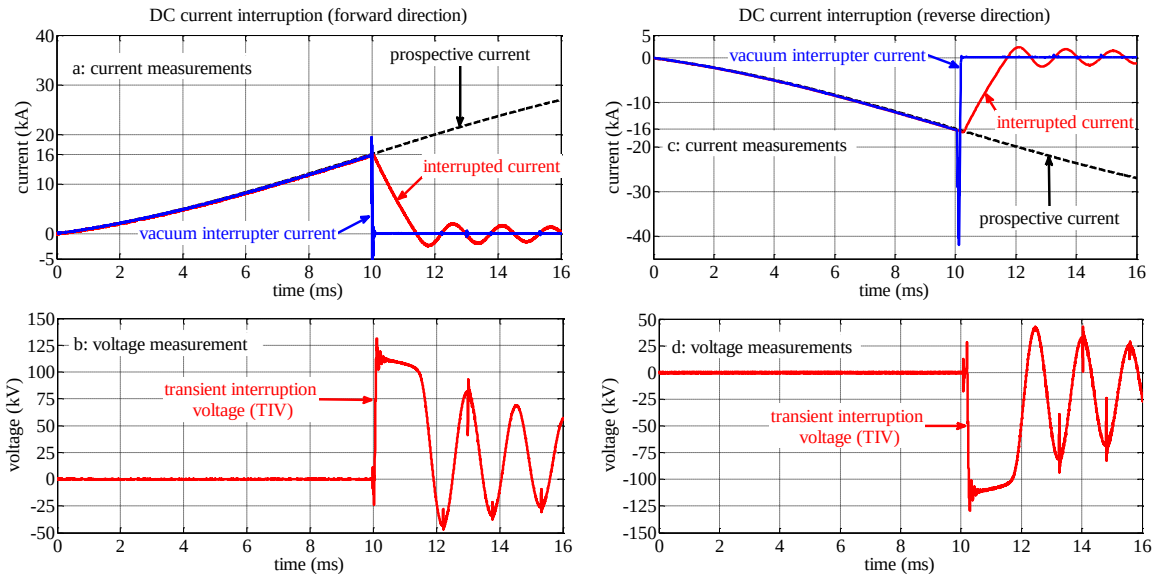

Figure 3-4: T100 forward and reverse current interruption in a 16. 7 Hz AC test circuit

After current suppression, there is an oscillation on the current and voltage waveforms. This is due to the interaction between the capacitor of the test object and the total inductance in the circuit including the counter current injection inductance of the test object. Normally a series residual current breaker trips simultaneously with the HVDC circuit breaker which prevents such an oscillation after current suppression.

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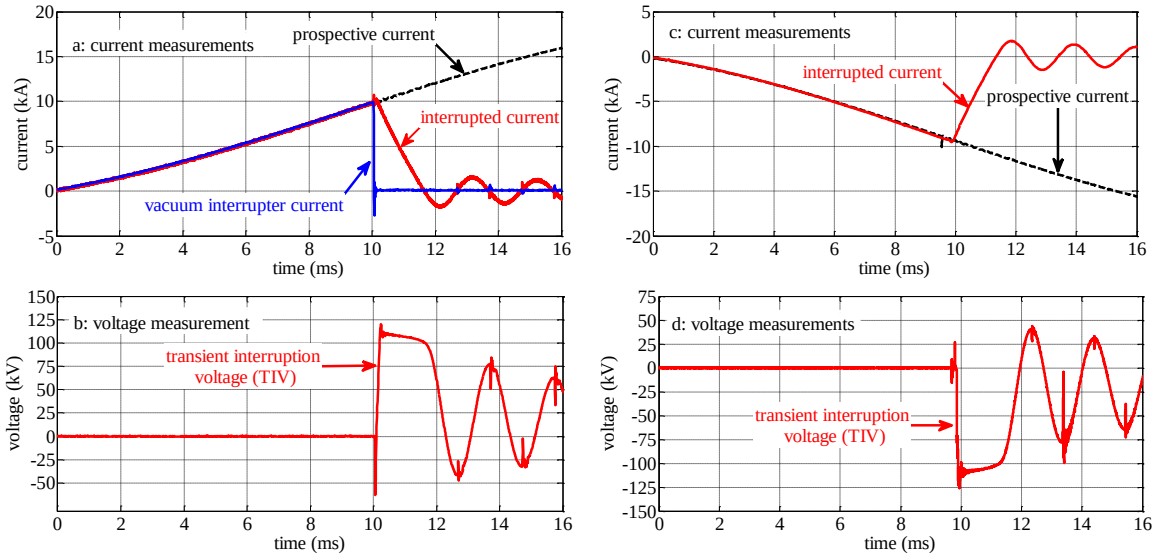

Figure 3-5: T60 forward and reverse current interruption by active injection HVDC circuit breaker in a 16.7 Hz AC test circuit

Similarly, Figure 3-5 shows T60 (10 kA) current interruption both forward and reverse directions. The interruption process is similar to T100 interruption except the initial TIV due to the remaining charge across the capacitor of the breaker, which is higher when the current to be interrupted is lower. In addition, the rate of rise of TIV is lower in the case of T60 current interruption. This because lower current (10 kA) is charging the capacitor as compared to 16 kA in the T100 case. This can be clearly seen from Figure 3-5b. However, the di/dt through the vacuum interrupter at local current zero is higher for T60. In general, the lower the interrupted current, the higher the di/dt at local current zero of the vacuum interrupter, the higher the initial TIV due to remaining charge across the capacitor, and the lower the rate-of-rise of TIV. This is further discussed in the following sub-section. This is the reason that (for this breaker technology) low-current interruption is not by definition less severe than high-current interruption.

3.3.3 TESTING AT 30 HZ AND DEMONSTRATION OF DIELECTRIC STRESS AFTER CURRENT INTERRUPTION BY CAPACITOR CHARGE TRAPPING

Depending on the speed of operation of HVDC circuit breaker and the amount of energy stress needed from a test circuit, different source power frequencies can be used for testing HVDC circuit breakers. Therefore, in addition to 16.7 Hz test circuits are designed at 30 Hz and tests are performed to demonstrate the possibility to use other source frequencies. Test results of 30 Hz AC supply are shown in Figure 3-6. To achieve the same stress as 16.7 Hz test circuit, a slightly higher source voltage is used for the tests at 30 Hz.

Besides, since the driving voltage is supplied by the AC generator, it cannot provide dielectric DC stress after successful current interruption. However, some HVDC CBs, for example, the active current injection HVDC CB have capacitors as part of the CB which are charged during the current interruption process. These capacitors

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remain charged during the entire energy absorption period to a value equal to the TIV of the breaker. This can be utilized to provide dielectric stress after interruption (although not a good practice in testing). Figure 3-6 demonstrates the application of dielectric stress after current interruption in addition to current interruption by the HVDC circuit breaker.

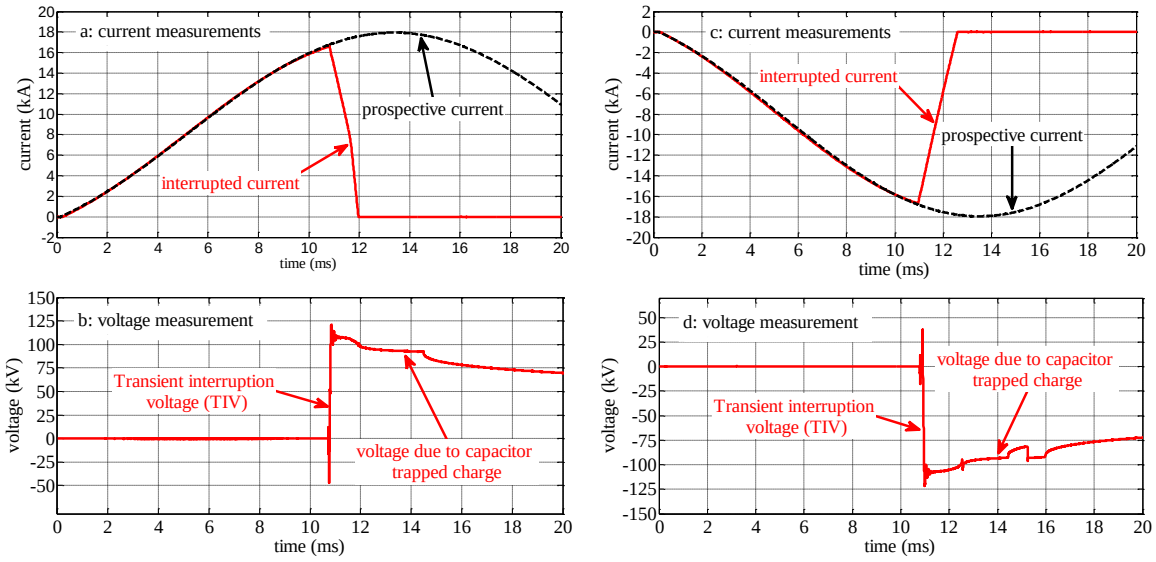

Figure 3-6: T100 forward and reverse current interruption by active current injection HVDC circuit breaker in a 30 Hz AC test circuit

The dielectric stress by charge trapping is demonstrated for test circuit at 16.7 Hz as well, see Figure 3-7c and d. However, it can be seen from the TIV plots that the trapped charge decays quite rapidly. Also, this approach makes the test procedure dependent on the internal components of the HVDC circuit breaker which is not the best test practice. Thus, the method that provides DC voltage stress as part of test circuit is investigated and this is discussed in Section 2.4 .

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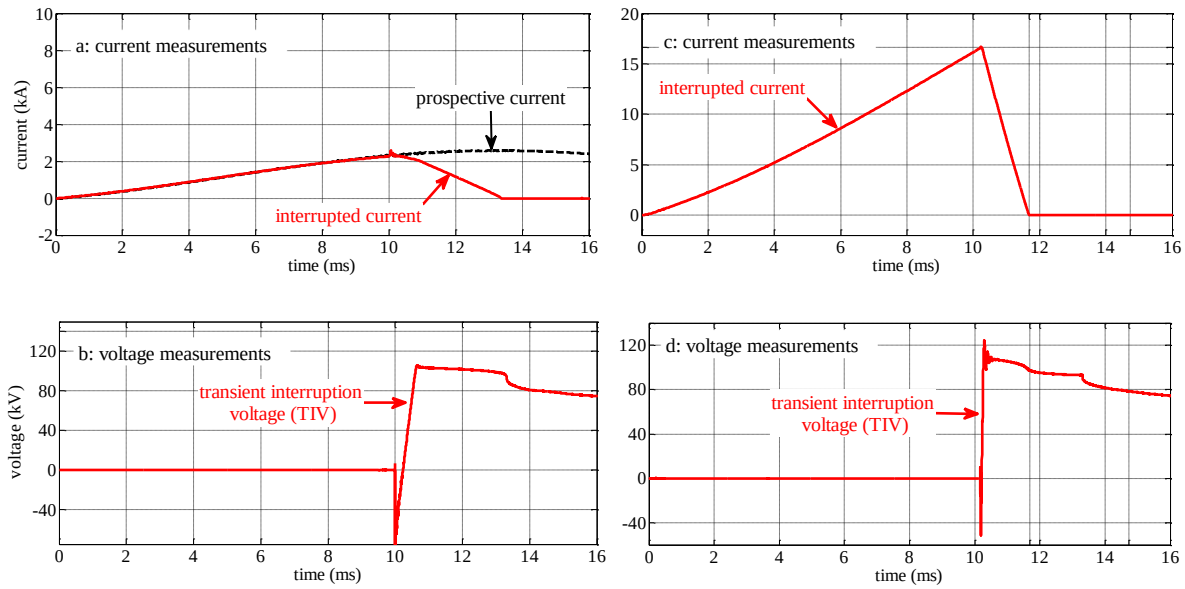

Figure 3-7: T10 and T100 forward current interruption in a test circuit supplied by 30 Hz and 16.7 Hz, respectively AC short-circuit generators

3.3.4 DEMONSTRATION OF HIGH ENERGY STRESS

Another important aspect of HVDC circuit breaker is the energy absorption capability. While interrupting the same current magnitudes, different energy levels can be absorbed by the HVDC circuit breaker. A test demonstrating an absorption of 3.6 MJ energy is performed. The oscillograms of the test result including the absorbed energy is shown in Figure 3-8. Thus, it can be seen from this figure that while interrupting current just over 16 kA, 3.6 MJ of energy is absorbed by the MOSA of the circuit breaker.

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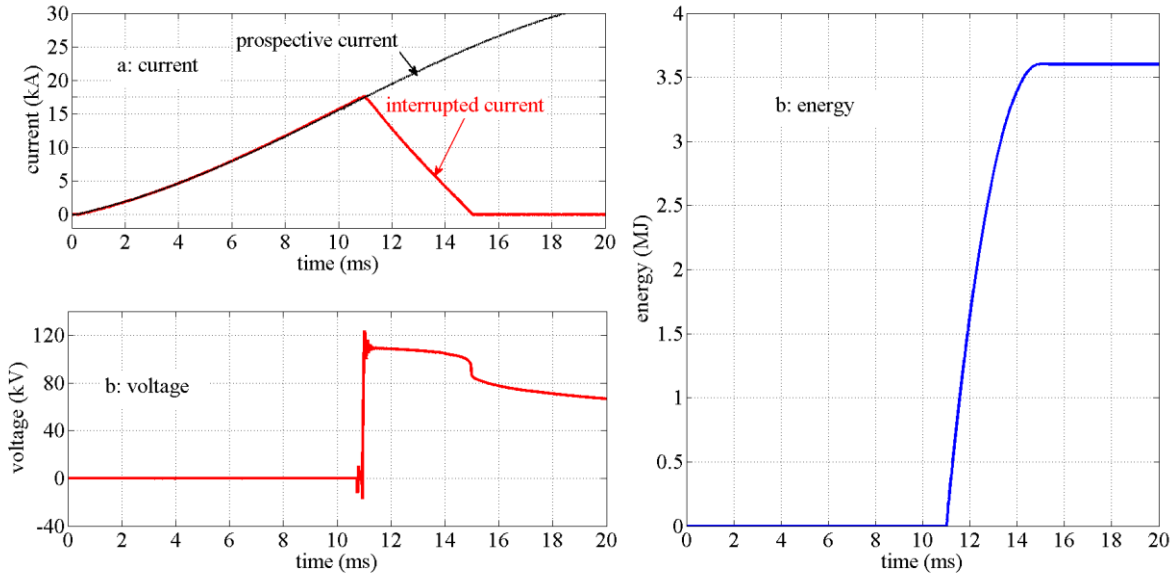

Figure 3-8: Demonstration of high energy absorption and dielectric stress by charge trapping during T100 duty interruption in 16.7 AC test circuit

3.4 VSC ASSISTED RESONANT DC CIRCUIT BREAKER

The VSC (Voltage Source Converter) Assisted Resonant Current, or VARC for short, technology for DC circuit breakers uses a vacuum interrupter as its main current interrupting element. The technology builds upon the idea to successively ramp up the amplitude of an oscillating current in the main breaking element until an artificial zero-crossing, which leads to interruption of the fault current, occurs.

The main components in the design and their interconnections are shown in Figure 3-9. In this section the converter in Figure 3-9 is called the VSC and the rest of the components will be called as they are labelled in Figure 3-9.

A description of the main components in the VARC DC CB and the events during an opening operation are as follows.

During the beginning of the opening operation of the breaker, the surge arrester can be disregarded, and thought of as an open circuit. Upon receiving an order to open, the breaker begins separation of the contacts in the Residual Current Interrupter and in the Main Interrupter. The Main Interrupter is required to open very quickly, reaching sufficient contact separation for interruption in less than 3 ms, but the Residual Current Interrupter can use a slower mechanism for opening, allowing for times up to 30 ms until contact separation.

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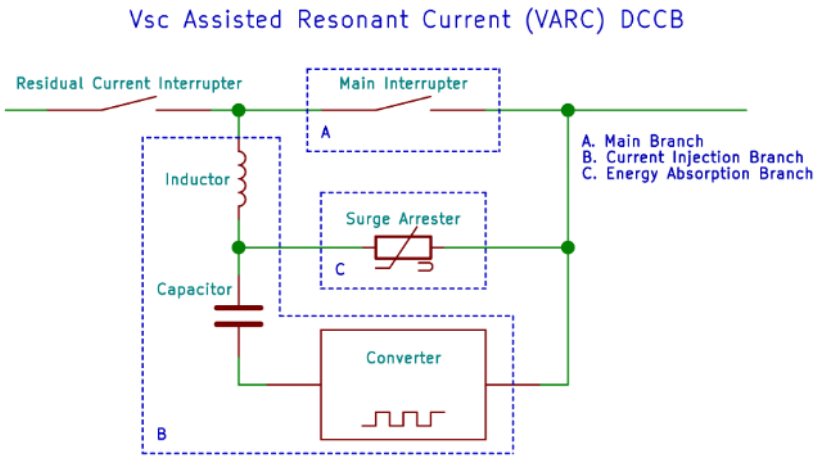

Figure 3-9: Schematic diagram of VSC assisted resonant DC circuit breaker

When sufficient contact separation has been reached in the Main Interrupter, the oscillation in the Current Injection Branch is initiated by letting the VSC successively switch the polarity of its output voltage.
Since the VSC is connected in series with a resonant circuit, the resonant circuit will oscillate after the first voltage step from the VSC. Thereafter, the VSC is controlled so that its output voltage is in the same direction as its output current, so that the instantaneous output power is always positive. An idealised illustration of how the VSC current and voltage look during oscillation is shown in Figure 3-10.

The step response in the current of the resonant circuit for a voltage step at time zero, $\mathrm{U(t)U_{vsc}}$, is $sin(\omega t)\frac{U_{vsc}}{X}$, where ω, X and U_{vsc} denote the angular resonant frequency of the resonant circuit, the characteristic impedance of the resonant circuit and the DC-link voltage of the VSC respectively. The letter H denotes the Heaviside step function.

The switching of the converter can be represented as a sequence of voltage steps with alternating polarity, so that the total current through the converter at time t can be written as a sum of the corresponding step responses, $\frac{U_{vsc}\,sin(\omega t)}{X}\left[1+2\sum_{k=1}^{N}\mathrm{H}\left(t-\frac{\pi k}{\omega}\right)\right]$, where N is the number of polarity switches and the first step of the VSC is placed at time zero. If the initial VSC output voltage is zero, the first step has amplitude U_{vsc}, but the following steps have amplitude $2U_{vsc}$.

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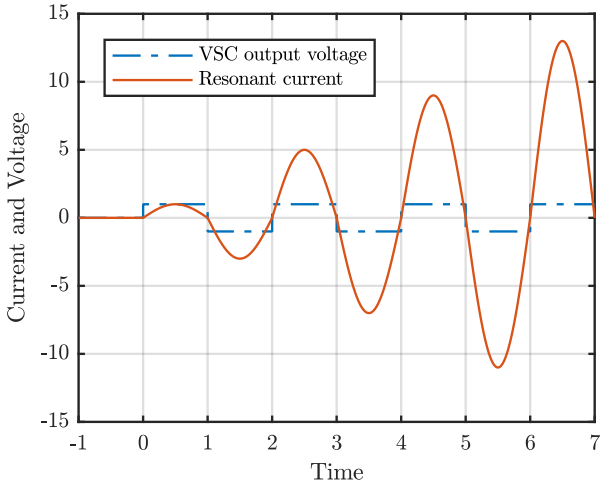

Figure 3-10 An idealised illustration of current through and voltage between terminals of the VSC during excitation of the current oscillating in the Current Injection Branch. The scales of both axes are arbitrary, but numbers have been placed on the axes for readability.

Ensuring that the output voltage of the VSC always has the same polarity as the current through it leads to the fastest possible increase in amplitude of the resonant current. It also has the benefit that switching is performed only when the current through the VSC is zero. Switching only at zero current leads to that the semiconductor switches inside the VSC never need to break significant current, and therefore experience lower over-voltages and have lower switching losses than they would have if they needed to switch at high current. Because of this, the design of the VSC can be very economical, considering its output power. In the demonstrated breaker module, the converter has a peak output power of 20 MW but can be housed in the small white box shown in Figure 3-12.

Once the oscillating current has reached the amplitude of the line current, there is a current zero crossing in the main interrupter. At the moment when the line current and the oscillating current are equal, i.e. at the time of current zero-crossing in the main Interrupter, the line current is fully commutated into the resonant branch.

The current in the resonant branch is at that time near a local maximum, so the voltage across the resonant capacitor is close to zero. As the line current continues to flow into the resonant capacitor, the capacitor voltage rises. When the resonant capacitor voltage reaches the surge arrester clamping voltage, the current starts to flow into the surge arrester as well, until the line current has been brought down to zero. Data from a simulation of these currents and voltages close to current zero can be seen in Figure 3-11 below.

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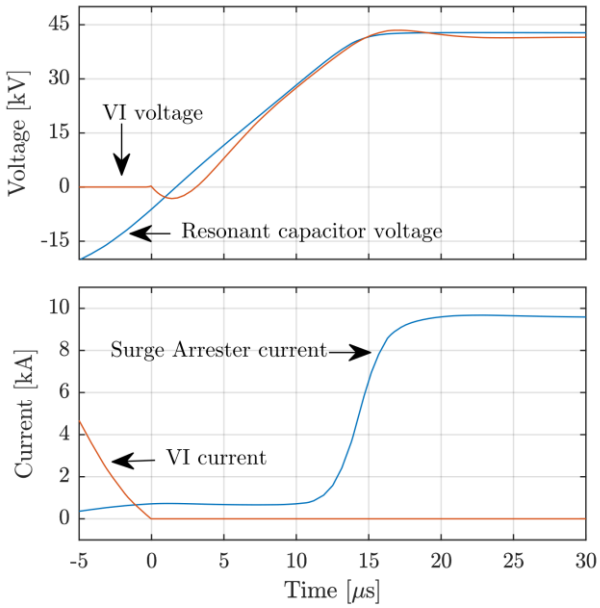

Figure 3-11 This figure shows the simulated voltage and current through the Main Current Interrupter (here labelled VI), current through the Surge Arrester and voltage across the resonant capacitor just after current zero. Note how the resonant capacitor continues to charge after current zero, until it rises above the knee-point of the surge arrester, at which point the current starts to flow through the surge arrester.

When the line current is close to zero, a relatively small oscillation between the resonant capacitor and the series inductance in the grid or test circuit ensues. This oscillation creates plenty of current zero crossings for the residual current breaker to interrupt.

The main interrupter can be closed some time after the residual current interrupter has interrupted the small oscillating residual current and will stay closed until the next operation. The making is performed by the residual current interrupter. More details on the VARC technology can be found in literature [2] [3].

3.4.1 TEST SET-UP

The breaker module prototype that was tested was designed for a 40 kV TIV and 10 kA interruptions current. This voltage rating corresponds to a 27 kV system voltage, so that 12 modules would be required for a 320 kV breaker. The surge arrester for the module was designed to withstand dissipation of 2.5 MJ before cooling to ambient temperature.

The test circuit used for the tests was the one described in section 2.2, but without the arc prolongation or additional dielectric stress circuits. Since the residual current interrupter was not tripped in advance, the charge in the resonant capacitor was not trapped, and so dielectric stress was exerted on the main interrupter only during the current suppression time. Primarily the breaking capability and the voltage withstand capability for a few milliseconds after current zero was tested during the test sessions shown in this report.
A picture of the breaker module prototype can be seen in Figure 3-12. A picture of the module standing in the test hall can be seen in Figure 3-13.

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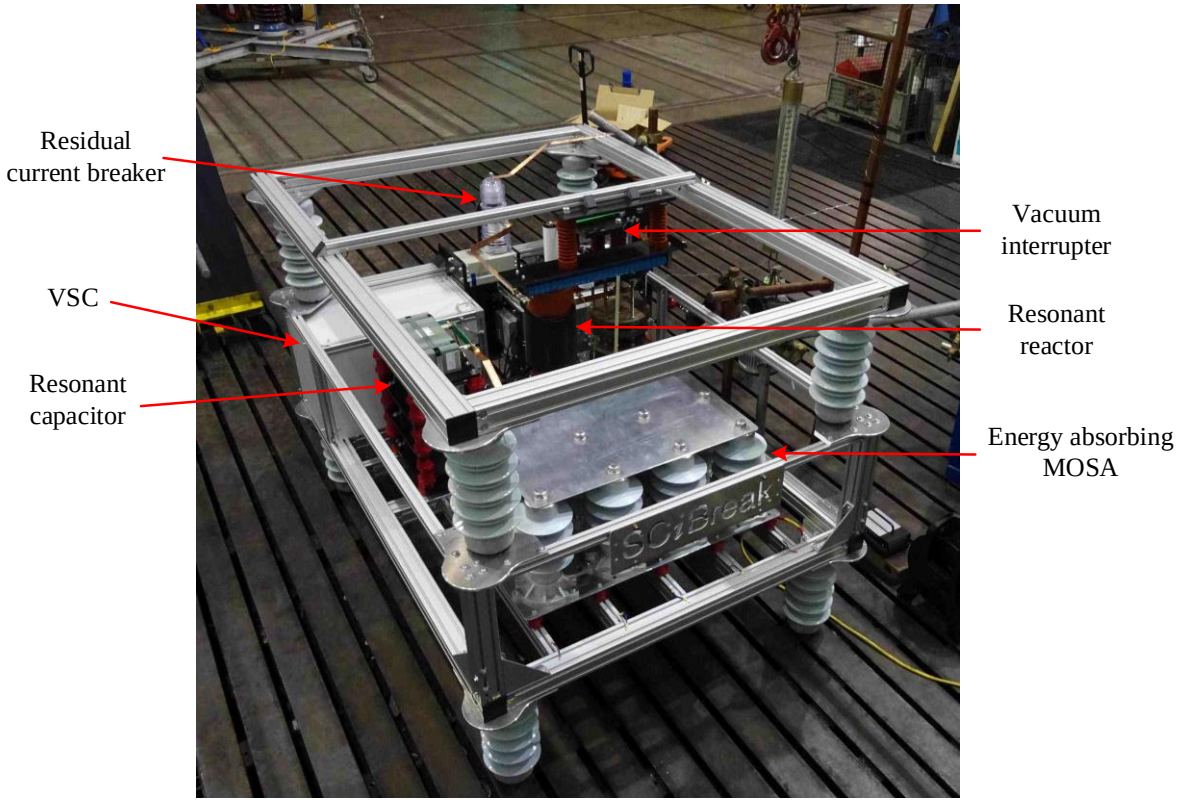

Figure 3-12 Photo of the VSC assisted resonant current DC circuit breaker prototype in a test hall at the laboratory. The top part of the frame is one pole of the breaker, and the bottom part of the frame constitutes the other pole.

Measurements of the voltage across and current through the breaker were performed by the test laboratory. In addition SCiBreak had two measurement systems also connected to the test object – one oscilloscope floating at the potential of the test object, and the measurement system that is included in the breaker control system.

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Figure 3-13: Test set-up of VSC assisted resonant current (VARC) DC circuit breaker prototype module at KEMA laboratories.

3.4.2 TEST RESULTS

A test program consisting a set of 12 test duties (or 12 tests? The word duties were used in a different sense before) were prepared for the testing sessions. Of the 12 test duties that were prepared for, test duties 2, 3, 4, 9 and 10 were performed. The energies and current levels for these tests are shown in Table 3-1.

The tests 2, 3 and 4 used a relatively low rate of rise of the fault current of 0.67 kA/ms, whereas the test 9 and 10 were, at 2.0 kA/ms, closer in di/dt to an expected rate of rise of fault current in an HVDC application.

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The maximally interrupted current in any test was 10.8 kA, with a corresponding dissipated energy of approximately 300 kJ. The maximal dissipated energy for any test was approximately 610 kJ, with a corresponding interrupted current of 10.1 kA.

Measured waveforms from a sequence of tests 2, 3 and 4 are shown in Figure 3-14. This sequence of tests was carried out with the same test circuit configuration for all three tests, but with different times at which a trip signal was sent to the breaker. The breaker operating time, i.e. time between trip signal and current zero in the Main Interrupter, was kept constant at 2.7 ms.

Table 3-1 List of test specified ahead of testing. The lines marked in blue correspond to tests chosen for the actual test sessions.

Test number	Peak current (kA)	Dissipated energy (kJ)
1	2	30
2	5	200
3	8	440
4	10	610
5	1	6.4
6	5	270
7	10	800
8	-1	6.4
9	-10	300
10	10	300

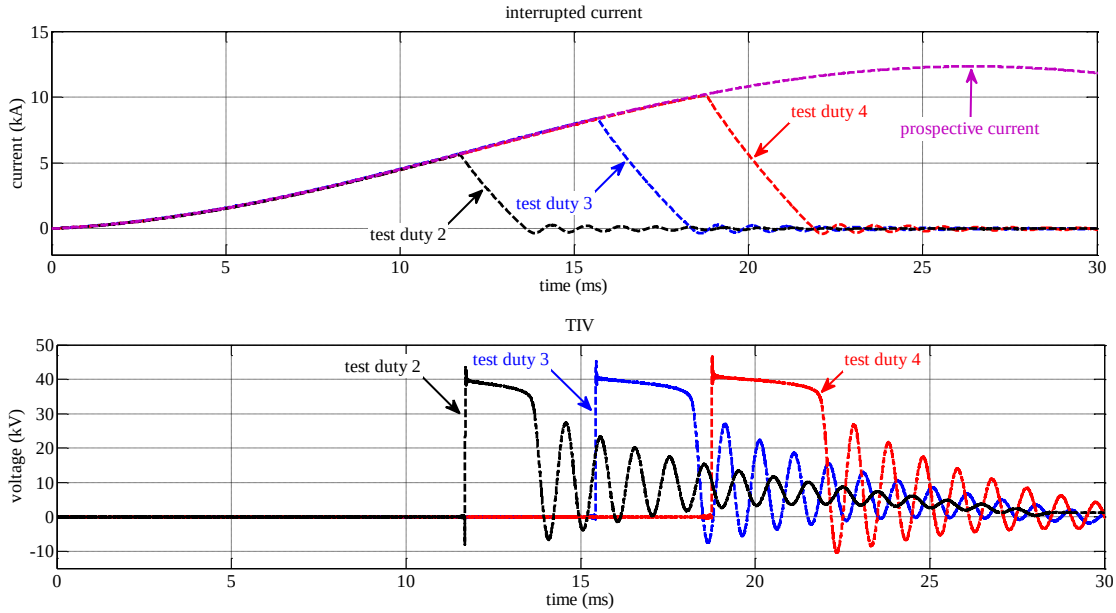

Figure 3-14: Test results 5.6 kA, 8.3 kA and 10.1 kA current interruptions

Interruption of currents in both directions was verified - test 9 was performed with a current direction opposite to that in the previous tests, and no difference was seen in operation of the breaker with regards to direction of the

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fault current. Figure 3-16 shows a reverse direction current interruption at -10.8 kA. A corresponding positive current test can be seen in Figure 3-15.

The oscillations that ensue following suppression of the fault current are oscillating between the series inductance external to the breaker and the capacitor in the resonant branch.

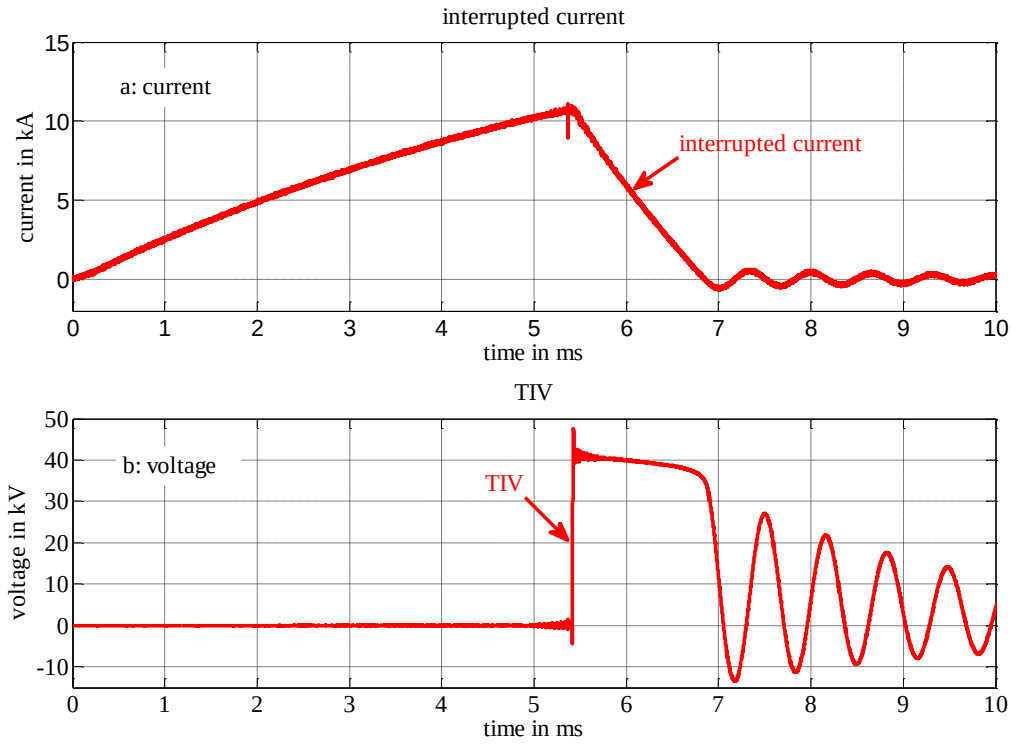

Figure 3-15: 10.8 kA current interruption test result

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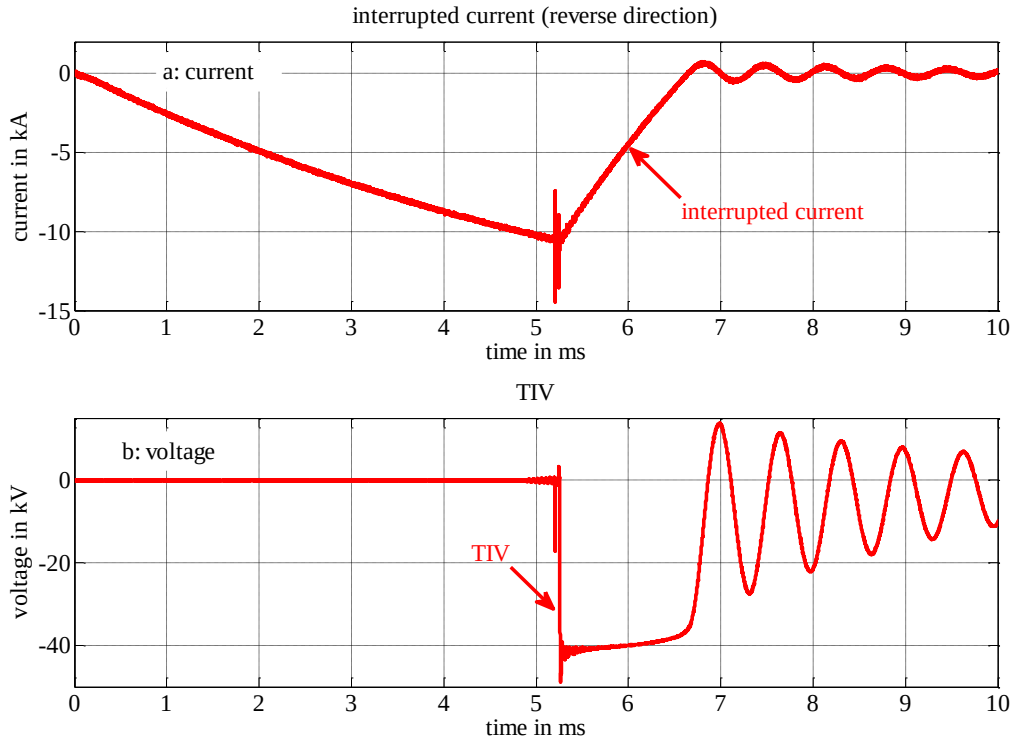

Figure 3-16: 10.8 kA reverse current interruption

The figures shown so far in this section have all been based on data from the laboratory measurement system. A view of a 10.8 kA interruption recorded with SCiBreak's control system can be seen in Figure 3-17 and Figure 3-18. The Figure 3-18 shows a magnified view of the time close to the current zero of the interruption shown Figure 3-17. The difference in magnitude between the VSC output voltage and the TIV of the breaker is clearly visible in these figures. It can also be seen that 16 reversals of the output voltage of the VSC, when including the first one, were performed for this particular interruption.

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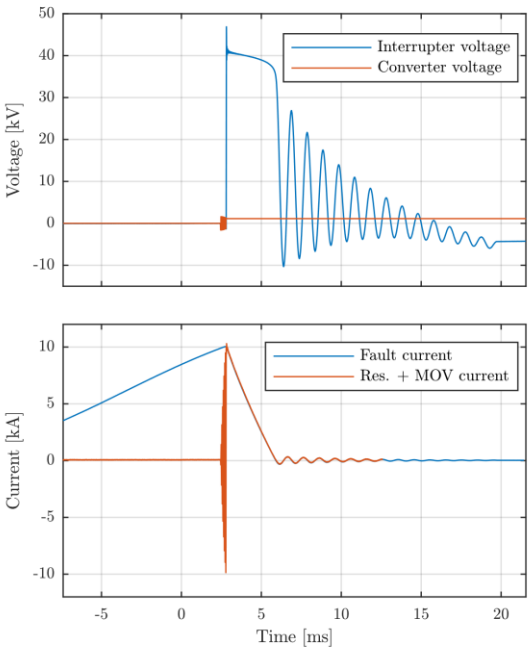

Figure 3-17 A view of a 10.8 kA interruption recorded with SCiBreak's measurement system. The converter (VSC) voltage is reconstructed, and not measured. The Interrupter voltage here refers to the Main Current Interrupter voltage. The time is counted from the trip signal was sent to the breaker.

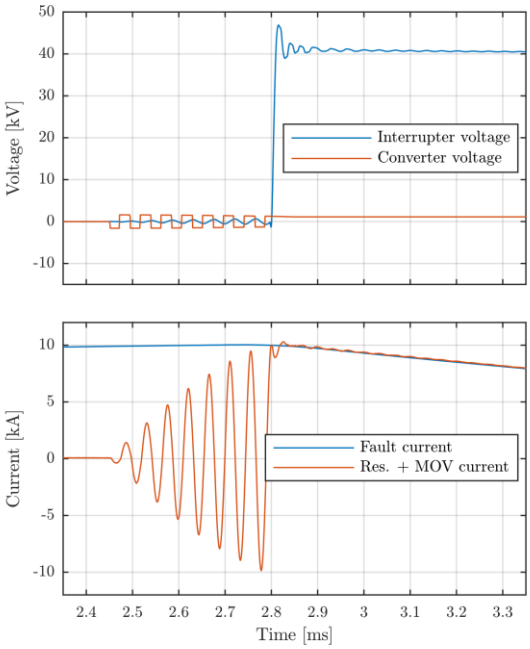

Figure 3-18 This figure shows a zoomed in view of the interruption case shown in Figure 3-17. The data used for this plot comes from SCiBreak's measurement system. The converter (VSC) voltage is reconstructed from other measurements, and not directly measured. The Interrupter voltage here refers to the Main Current Interrupter voltage. The time is counted from when the trip signal was sent to the breaker.

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3.5 CAPABILITIES AND CHALLENGES OF A TESTING MULTIPLE MODULES OF HVDC CB

Testing of HVDC circuit breaker requires high short-circuit power. This is needed to supply the necessary current with sufficient rate-of-rise and energy. When using AC short-circuit generators, there are many other parameters that need to be adjusted before testing HVDC circuit breaker. For example, accurate making angle, proper reactance in the circuit, source voltage and flexibility in power frequency are the major ones. However, each of these parameters have limits within which they can be adjusted, thereby putting a limit on the capability of the test facility. For example, the minimum circuit inductance at different voltage levels considering test installation at KEMA laboratories has been presented in D5.7. The minimum inductance in turn determines the maximum rate-of-rise of current. Moreover, the capability of a test installation, to a significant extent, depends the HVDC circuit breaker parameters.

Figure 3-19 shows the capability of DNV GL's KEMA Laboratories with respect to testing different technologies of HVDC circuit breakers at different system voltages. The computation is performed considering all the breakers can interrupt a maximum current of 16 kA. It can be seen that the maximum energy that can be supplied depends on the breaker parameters such as breaker operation time. The faster the breaker the breaker, the lower the energy that can be supplied. This is in line with the fact that the faster the breaker, the smaller the DC current limiting reactor and hence lower energy absorption.

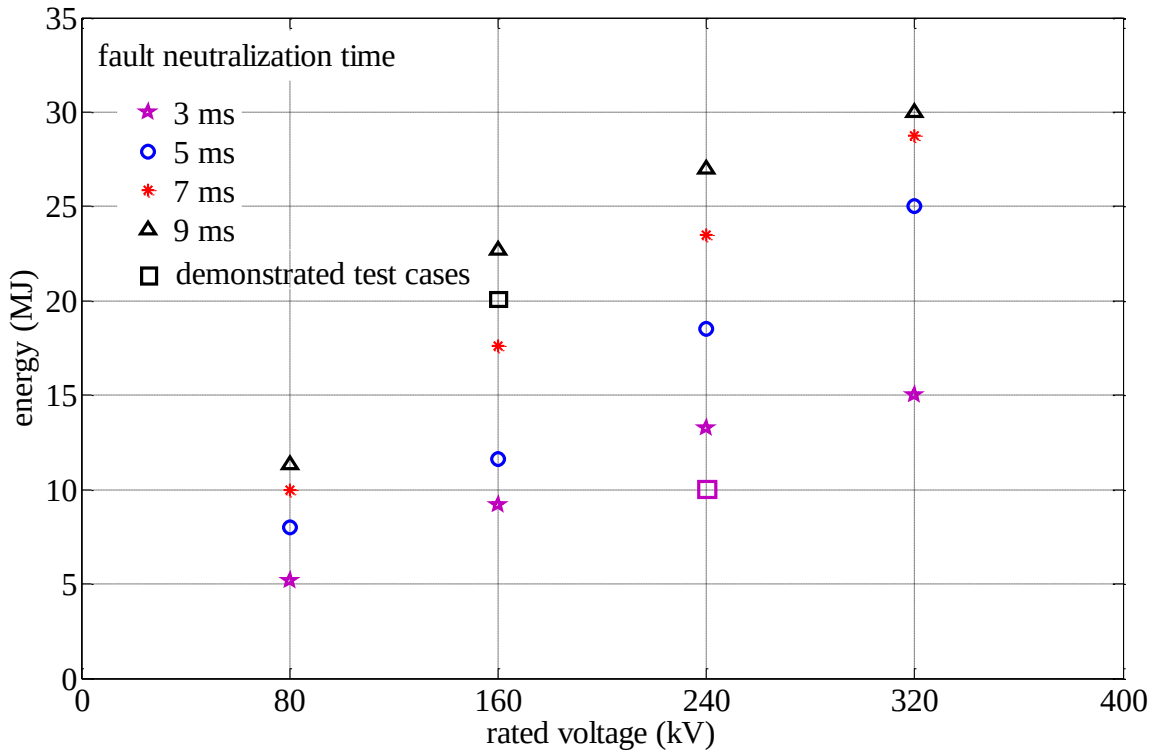

Figure 3-19: Capability of KEMA Laboratories with respect to testing different technologies of HVDC circuit breakers at various system voltages

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4 SUMMARY

This deliverable presents demonstration of the use of AC short-circuit generators based test circuit for demonstrating the performance of two HVDC circuit breaker technologies. The mentioned test circuit is designed, implemented and its correct functioning has been verified in the presence of prototypes of HVDC circuit breakers.

In addition to showcasing the suitability of the test circuit, the tasks performed in this deliverable demonstrate the performance of the test object although the performance shown here my not be the limiting performance. Hence, in this report prototypes of two candidate HVDC circuit breaker technologies are demonstrated and test results are presented.

The first prototype demonstrated is an active current injection HVDC circuit breaker with the peak TIV of 125 kV whereas the second prototype demonstrated is the voltage source assisted (VSC) assisted resonance DC circuit breaker (VARC) with a peak TIV of 40 kV. Before the actual test, the procedures/steps required to adjust the correct parameters of a test circuit and the different test duties intended for demonstration of the performance of HVDC circuit breakers are defined and tests are performed accordingly.

The complete short-circuit current interruption test involves not only the current interruption in the main interrupter and suppression by energy absorbing branch, but also DC voltage stress after interruption. The method of applying this has been demonstrated practically in the absence of prototype HVDC circuit breaker. In addition, in this report, fine tuning of the control and operation of a test circuit as well as other functionalities such as over-current protection and arcing time prolongation and application dielectric dc voltage stress after current interruption are performed under real, high-power conditions. The results show the validity and availability of the complete test circuit for use. Besides the correct functioning of test circuits, tests intended for controlling different energy absorption of the test breakers are performed. Test results showing the performance of the test circuit as well as the test breakers are provided. The document also presents the limits and capabilities of a test environment considering the actual installation at the test facility and considering the performance parameters of the three proposed HVDC circuit breaker technologies.

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