PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

D4.5 Requirements for DC switchgear

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NOMENCLATURE

ABBREVIATION	DESCRIPTION
DCCB	DC circuit breaker
ACCB	AC circuit breaker
HVDC	High-voltage direct current
DC-FRT	DC fault-ride-through
IED	Intelligent electronic device
MMC	Modular multilevel converter
LCS	Load commutation switch
UFD	Ultra fast disconnector
MB	Main breaker
BIGT	Bimode insulated gate transistors
SOA	Safe operation area
SA	Surge arrester
O-C-O	Open-close-open
BF	Breaker failure
PTG	Pole-to-ground
PTP	Pole-to-pole
CBM	Converter breaking modules
LBM	Line breaking modules
PIR	Pre-Inserted Resistance
TIV	Transient interruption voltage
FB-MMC	Full-bridge MMC
HB-MMC	Half-bridge MMC

LIST OF SYMBOLS

SYMBOL	DESCRIPTION
$t_{br,o}$	Breaker opening time
$I_{br,pk}$	Rated breaking current
L_{line}	Series line inductance
t_{cl}	Fault clearing time
$t_{U_{DC}}$	DC voltage restoration time
$t_{P_{AC}}$	Active power restoration time
E_{SA}	Energy absorbed in the energy absorption branch (surge arresters) of a DCCB
i_{LCS}	Current in the LCS
$I_{LCS,n}$	Rated current of the LCS
I_C	Rated DC collector current of a BIGT module
i_{int}	Peak interrupting current
I_{sp}	Overcurrent threshold of DCCB self-protection function
$I_{LCS,dp}$	Overcurrent threshold for the LCS of DCCB driver-protection function
$I_{MB,dp}$	Overcurrent threshold for the MB of DCCB driver-protection function

Content

EXECUTIVE SUMMARY

DC switchgear is one of the key technologies to enable the deployment of large-scale meshed HVDC grids, as successful clearing of DC-side faults is essential to ensure the reliability of hybrid AC/DC systems. Recently, great progress has been made on DC switchgear technologies, in particular DC circuit breaker (DCCB) technology for high-voltage applications. Various DCCB technologies with a wide range of functions and capabilities have been proposed, tested and even installed in real projects, such as in the multi-terminal HVDC systems in China. Besides these functions and capabilities, these DCCB technologies may be used in various application scenarios which each impose specific requirements. This is due to the fact that HVDC grids may take different forms in terms of system configuration and grounding schemes, and use one of the three main protection philosophies: non-selective, partially selective and fully selective fault clearing. These application scenarios entail different requirements for the DCCBs, as the fault behavior varies largely depending on the transmission line technology, system configuration, and the employed protection strategy. Therefore, it is necessary to identify the scenarios in which DCCBs can be applied, and to define the DCCB requirements in line with the applied scenarios.

This deliverable proposes general requirements of DCCBs based on results obtained in the PROMOTioN project, particularly in work package WP4 and WP6. The requirements of DCCBs are classified into three types mainly based on their operating speed and breaking current capability: (1) Type-I: fast DCCBs with short-circuit current interruption capability, which are applicable in a fully selective (or partially selective) strategy, requiring the DCCBs to deal with both pole-to-pole and pole-to-ground faults, regardless of the HVDC system configuration, grounding schemes and the type of transmission lines; (2) Type-II: slow DCCBs with low current interruption capability, which are applicable in high-impedance grounded cable-based HVDC systems using a fully selective strategy, requiring the DCCBs to deal with only pole-to-ground faults; and (3) Type-III: slow DCCBs with short-circuit current interruption capability, which are applicable in HVDC systems using a non-selective strategy.

The requirements for these three types of DCCBs, in terms of breaker opening time, breaking current capability, series inductor size and energy absorption capability, are specified using either a generic approach or simulation studies:

- For Type-I DCCBs used in a fully selective protection strategy, a methodology to specify the general requirements for the DCCBs is developed, and illustrated with results obtained on the PROMOTioN small impact test network. First, the required functions of a DCCB should be specified in the intended application, as the dimensioning of DCCB components is closely related to its functions. Second, the DCCBs should be dimensioned to fulfil the requirements imposed by the HVDC grid and its components, such as requirements on the DC fault-ride-through (DCFRT) of the converters, stability of the HVDC grid voltage, the selectivity by the protection IEDs, multi-vendor interoperability and protection coordination between the DCCBs and IEDs. The required opening speed and breaking current capability for the Type-I DCCBs are high, in the range of few ms and larger than 10 kA, respectively. A large series inductor and high energy absorption capability are also required for the Type-I DCCBs, although the exact range is system dependent and should be studied for each system.

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- For Type-II DCCBs used in a high impedance cable-based system with a fully selective protection strategy, feasible ranges of breaker opening speed, breaking current and energy absorption capability are given, designed to only deal with pole-to-ground faults. Similar requirements as type-I DCCBs such as converter DC-FRT, selectivity, HVDC grid stability and multivendor interoperability requirements are generally applicable for dimensioning the Type-II DCCBs, as they are used in a fully selective strategy. The required opening speed and breaking current capability of the Type-II DCCBs are low, in the range of 20 ms and few kA, respectively. Potentially medium/large series inductance is needed, similar to that required for Type-I DCCBs. The exact range for the inductance and the required energy absorption capability are system dependent and should be studied for each system.
- For Type-III DCCBs used in a non-selective protection strategy, specifications derived from studies performed in the PROMOTioN small impact test network are given as examples. The opening speed of the Type-III DCCBs is 20 ms. The required breaking current capability is very high, for instance, 20 kA in the PROMOTioN test network. The exact value may change depending on the system, particularly the transmission line types, capacity of the converters, and the size of the HVDC grid. This type of DCCBs requires zero inductance and hence very low energy absorption requirement.

The classification of different types of DCCBs based on their application scenarios and their general requirements are considered as the first step towards standardization of DCCBs for HVDC grid protection applications. It is believed that the results obtained in this deliverable are valuable inputs for international standardization bodies to establishing standards on DCCBs.

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1 INTRODUCTION

In existing HVDC projects, a great number of different DC switchgear may be involved to ensure safe operation, protection and maintenance of the system [1] (Figure 1-1). Within a DC substation, DC switchgear can be roughly grouped in four categories according to their functionalities: disconnecting, earthing, current transfer and current interruption.

- Disconnecting switches (abbreviated with "D" in Figure 1-1) are used to disconnect a component or circuit for isolation, and are typically only required to interrupt small leakage currents. Recently, high-speed switches (HSS), with an opening speed in the range of few ms to few tens of ms, have been proposed for fast isolation in non-selective protection strategies for fast isolation [2].
- Earthing switches (abbreviated with "ES" in Figure 1-1) are used for earthing and short-circuiting de-energized components, thus withstandability of short-circuit for a specified period of time is required.
- Transfer switches can be operated under no-load and nominal current conditions, and their switching duties involve to commutate a load current from one branch to another for reconfiguration. Examples of transfer switches are neutral bus switch (NBS), metallic return transfer switch (MRTS), earth return transfer switch (ERTS), bypassing switch (BPS) and parallel switch (PS).
- DC circuit breakers (DCCBs) are designed to interrupt a short-circuit fault current, absorb the energy and withstand the voltage associated with the interruption. DCCBs are by far the most challenging among the various types of DC switchgear due to the required high operation speed and high breaking current capability.

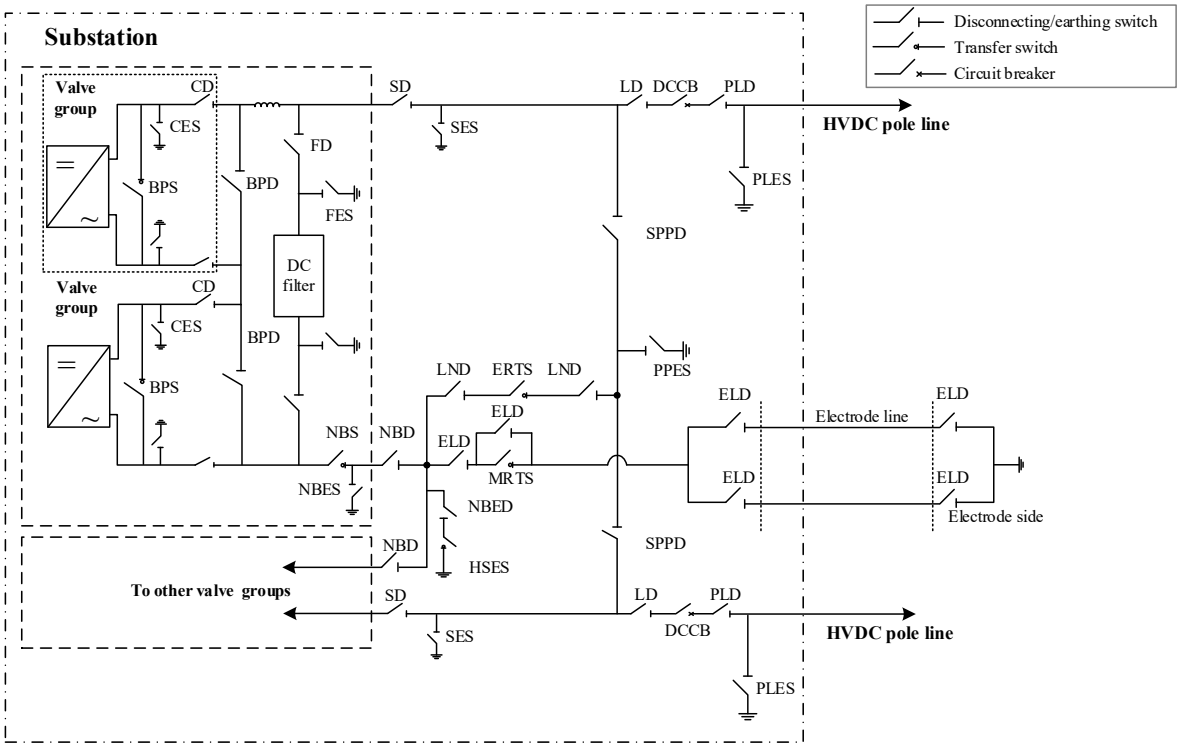

Figure 1-1 DC switchgear in a typical HVDC substation [1].

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Although various types of DC switchgear have been installed in the field, the requirements of the existing DC switchgear are typically project specific given the distinctive properties and requirements of each HVDC project. As the majority of the HVDC projects are provided by one single vendor, standardization on different types of DC switchgear has yet to be established. In a future system where different parts of the DC grids will be supplied by various vendors, such standardization efforts become necessary.

This deliverable focuses on specifying the requirements of DCCBs, as it is the most challenging type of DC switchgear. First, various DCCB technologies with a wide range of functions and capabilities have been proposed in literature, and it is not yet clear which functions will be required in the future HVDC grids. Second, DCCBs may be used in various scenarios, each imposing different requirements. Third, DCCBs are the type of switchgear that is expected to differ most from traditional LCC HVDC equipment
This deliverable summarizes the results obtained from relevant work packages in a structured way and specifies general requirements for the three types of DCCBs, in terms of breaker opening time, breaking current capability, series inductor size and energy absorption capability. First, relevant studies on HVDC grid protection strategies and DCCB technologies are briefly summarized in chapter 2 and chapter 3, respectively. Chapter 4 specifies the requirements of two types of DCCBs in a fully selective protection strategy. Chapter 5 specifies the requirements of the Type-III DCCBs in a non-selective protection strategy. Conclusions and summaries of this deliverable are provided in chapter 6.

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2 HVDC GRID PROTECTION STRATEGIES

Various DC grid protection strategies have been proposed over the years to deal with the challenges associated with HVDC grid protection using voltage source converters (VSCs). Extensive investigations have been carried out regarding DC grid protection strategies in WP4. The most relevant deliverables are D4.2 “Broad comparison of fault clearing strategies for DC grids” [3] and D4.3 “Report on Performance, interoperability and failure modes of selected protection methods” [4].

- An exhaustive literature review on DC grid protection strategies have been carried out in D4.2. Based on the scope of the protection zone, these strategies are classified to one of the three protection philosophies, namely, non-selective, partially selective or fully selective. These protection strategies were broadly compared in terms of their impact on the AC systems, main cost driver, risk analysis and extensibility.
- An in-depth analysis of few selected protection strategies were performed in D4.3, aiming to increase their technological readiness to accelerate a practical implementation. Key performance indicators (fault clearing time, DC voltage, active power and reactive power restoration time) were proposed to compare the impact on the AC/DC grids of the protection strategies. In addition, failure mode analysis and interoperability analysis on the key components were performed for the selected protection strategies. These selected protection strategies are briefly summarized in this section to serve as background of this deliverable.

Fully selective fault clearing

DCCBs are placed at both ends of a line in the fully selective protection philosophy; thus, the protection zone is confined in a line as illustrated in Figure 2-1. Fully selective fault clearing using hybrid and mechanical DCCBs were investigated in detail in D4.3. The study results show that fast active and reactive power restoration can be achieved after a DC fault clearance. The series inductor sizes associated with the DCCBs are key parameters in determining not only the fault clearing but also the dynamics of the HVDC grid. In particular, large inductor sizes, e.g. larger than 100 mH, may result in low frequency oscillations during post-fault restoration. Control bandwidth needs to be studied in conjunction with the selection of these inductors to achieve fast restoration and ensure the stability of the HVDC grid.

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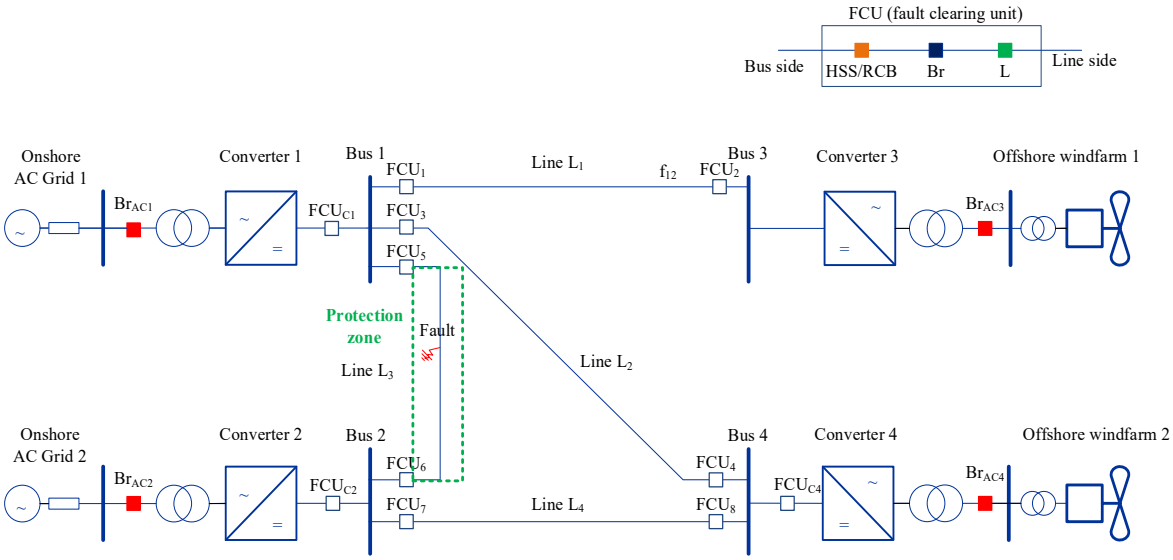

Figure 2-1 Fully selective fault clearing with DCCBs.

Non-selective fault clearing

In a non-selective protection philosophy, the whole HVDC grid is essentially one protection zone as illustrated in Figure 2-2 using converter DCCBs or Figure 2-3 using full-bridge MMCs (FB-MMC). DC-side faults on any of the lines in the HVDC grid result in de-energization of the whole HVDC grid. Both non-selective fault clearing strategies were shown to be able to restore active power within few hundreds of ms on the PROMOTioN small impact test network. Unlike a fully selective protection strategy, which can be applied to all types of networks, whereas, non-selective protection strategies are likely to be restricted to small to medium impact networks. Since for a medium or high impact network, it is very unlikely to allow all converters to apply a temporary or permanent stop simultaneously.

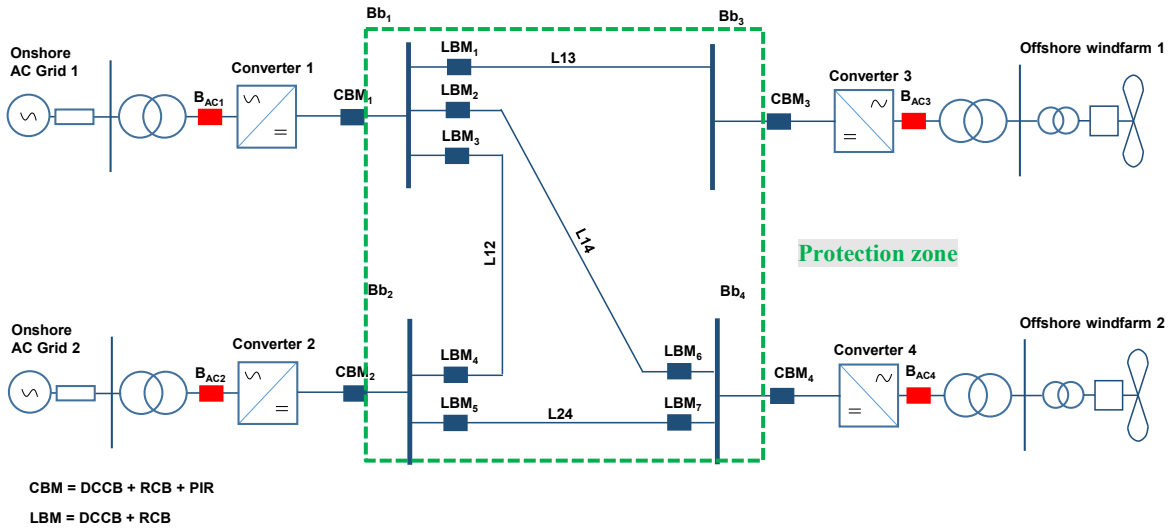

Figure 2-2 Non-selective fault clearing with converter and line DCCBs.

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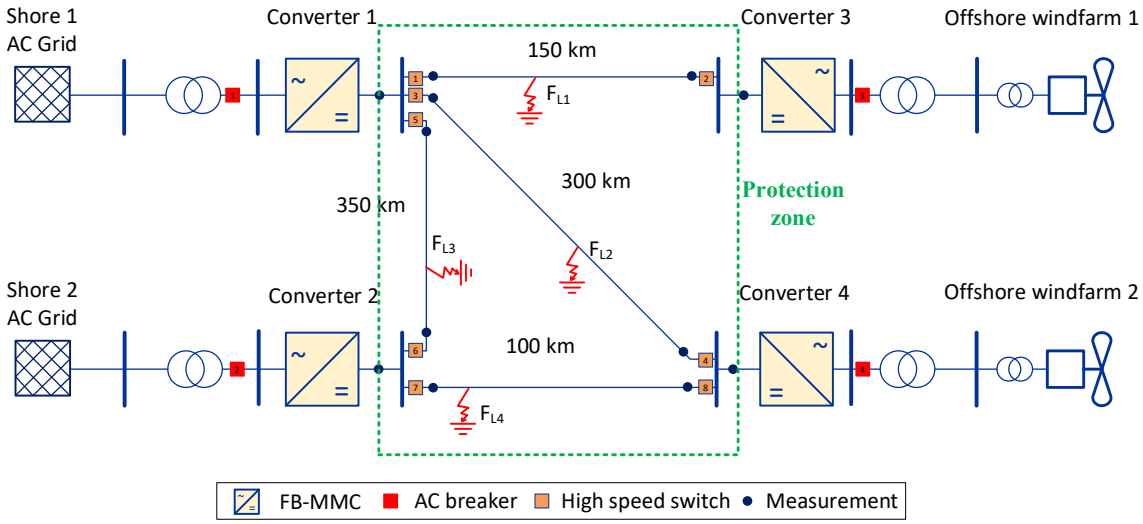

Figure 2-3 Non-selective fault clearing with FB-MMCs.

Partially selective fault clearing

The protection zone in a partially selective fault clearing depends on the adopted protection strategy in each sub-grid. For instance, a whole sub-gird can be one protection zone if a non-selective protection strategy is used in the sub-grid, as shown in Figure 2-4. Fast DCCBs in conjunction with large series inductors can effectively limit the impact of a DC fault in the faulted sub-grid.

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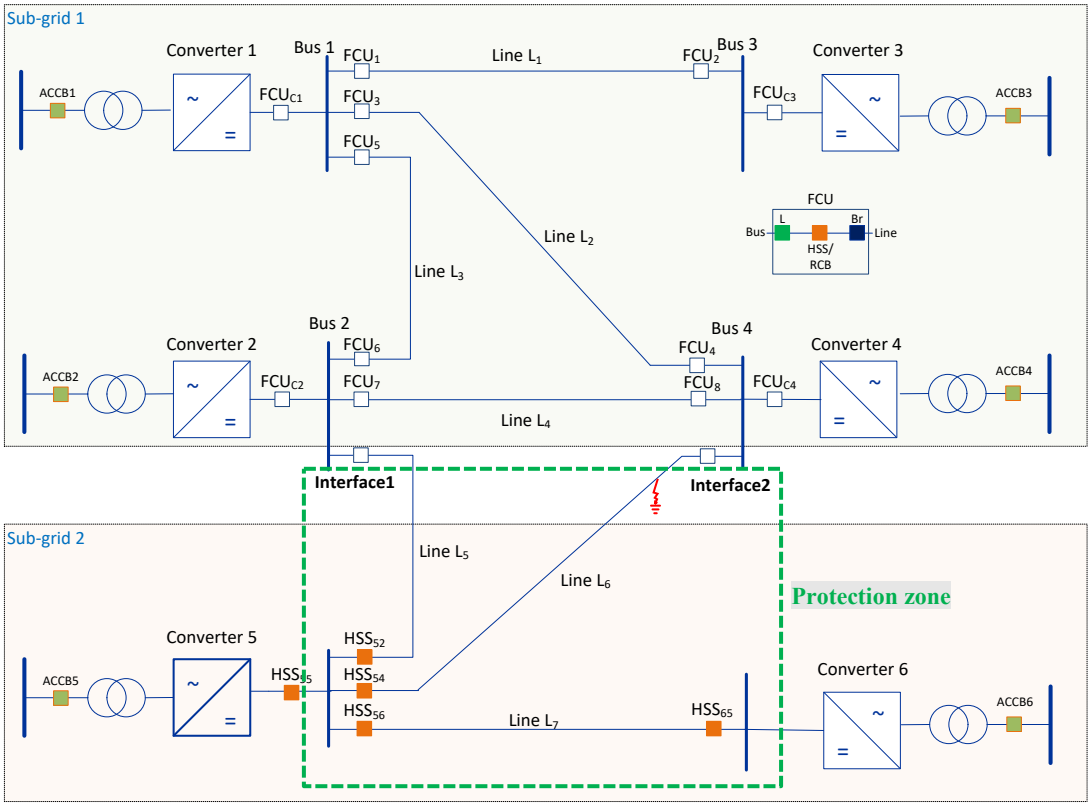

Figure 2-4 Partially selective fault clearing with hybrid DCCBs.

Generally speaking, the requirements on the DCCBs are primarily defined by the type of transmission lines, the type of DC faults to be considered, the protection strategy and the expected fault clearing performance.

First of all, DC fault response depends on system configuration and grounding scheme, the type of transmission lines and the adopted protection strategy [5]. In low-impedance grounded systems, such as a bipolar configuration or asymmetrical monopolar configuration, both pole-to-pole and pole-to-ground faults result in a high fault current and a low voltage. By contrast, in high-impedance grounded systems, such as a symmetrical monopolar configuration, the fault current during a pole-to-ground fault may initially have a large peak value, but evolves to a very low value in steady-state. Meanwhile, the faulted pole experiences a very low voltage whereas the healthy pole is subjected to a persistent overvoltage if no countermeasures are taken. Cable-based HVDC systems lead to a higher rate-of-rise of the current due to cable discharge, as compared with overhead line based systems. Furthermore, the adopted protection strategy influences the fault behaviour primarily due to the additional line inductances used in conjunction with DCCBs, the applied converter types and controls. Typically, line inductances in the range of tens of mH have to be applied to limit the rate-of-rise and the peak of the fault current in partially or fully selective strategies.

Second of all, the likelihood of the different types of faults is primarily determined by the type of the transmission lines. Pole-to-pole and pole-to-ground faults are likely to occur in overhead line based HVDC systems, whereas a pole-to-pole fault in cable-based HVDC systems is deemed unlikely. The protection system can be designed

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considering the likelihood and severity of different types of faults, the acceptable impact to the AC/DC systems, and the cost-benefit of the protection strategy [6].

Based on studies carried out in WP4, WP5 and WP6, particularly the analysis done in D4.2 and D4.3, three distinctive application scenarios have been identified according to their requirements on DCCBs,

(1) Application in fully selective or partially selective strategies, considering both pole-to-pole and pole-to-ground faults, regardless of system configuration and grounding scheme.
(2) Application in fully selective or partially selective strategies, considering only pole-to-ground faults in a high-impedance grounded cable-based HVDC system.
(3) Application in non-selective strategy with both converter and line-side DCCBs.

The classification of the DCCBs in this deliverable is tightly coupled with the application scenarios, as these application scenarios require DCCBs with different capabilities in terms of opening speed, breaking current capability, series inductor size and energy absorption capability.

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3 DC CIRCUIT BREAKER

This chapter gives a brief overview of different DCCB technologies and their functions. As modelling and control of various DCCB technologies have been analysed in detail in WP6, the reader is referred to [7, 8, 9] for an in-depth discussion on these aspects.

3.1 DC CURRENT INTERRUPTION

Compared with AC fault current interruption, the absence of naturally recurring zero-crossings in a DC fault current requires alternative solutions, such as using power electronic switches or creating artificial zero-crossings if mechanical switches are used for interruption [10, 11, 12]. In addition, DCCBs are required to dissipate the inductive energy stored in the system associated with the interruption process. Consequently, DCCBs typically consists of several branches to carry a load current (load current branch), to commutate current during interruption (commutation branch), and to absorb the associated energy (energy absorption branch). In addition, a residual current breaker (RCB) is typically required to provide isolation and prevent overloading of the energy absorption elements. A series line inductor may be needed in order to limit the rate-of-rise and the peak of the current to achieve successful interruption. The size of the line inductor may vary depending on the application scenarios.

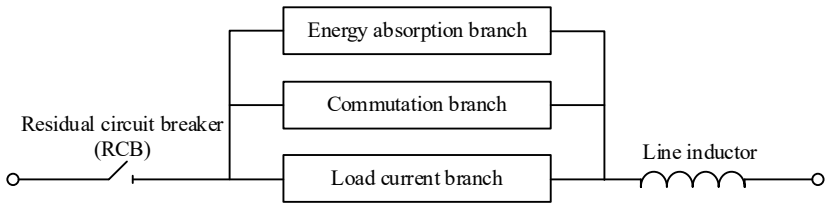

Figure 3-1 A generic representation of a DCCB.

3.2 DCCB TECHNOLOGIES

Depending on the technologies used for interrupting a current, DCCBs can be broadly grouped to mechanical (or resonance current injection), hybrid and pure power electronic types, each having their advantages and disadvantages in terms of operation speed, on-state loss, complexity and cost [13] [14]. With respect to hybrid and power electronic DCCBs, there is also an option to implement them with bidirectional or unidirectional current interruption capability. The three main technologies are briefly introduced in section 3.2.1, 3.2.2, and 3.2.3. Unidirectional DCCBs are discussed in section 3.2.4.

3.2.1 MECHANICAL DCCB

Mechanical DCCBs superpose a high-frequency AC current provided by a resonant circuit on the DC fault current to create zero-crossings, and consequently use an AC breaker for current interruption. There are two sub-types,

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namely passive and active resonance current injection, depending on if the resonant current is passively or actively injected to the load current branch.

Examples of mechanical DCCBs using passive and active resonance current injection are given in Figure 3-2 and Figure 3-3, respectively. Existing mechanical DCCBs using passive resonance current injection have reached rated current of 5.3 kA with interruption time within 20 ms [15]. Recent development on active resonance breakers demonstrates commutation can be achieved within 5~8 ms with breaking capability of 16 kA [11, 12].

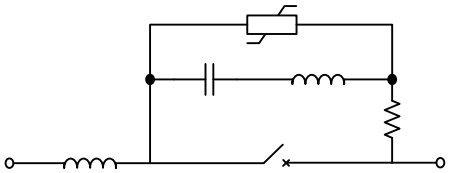

Figure 3-2 An example of mechanical DCCB using passive resonance curent injection [15].

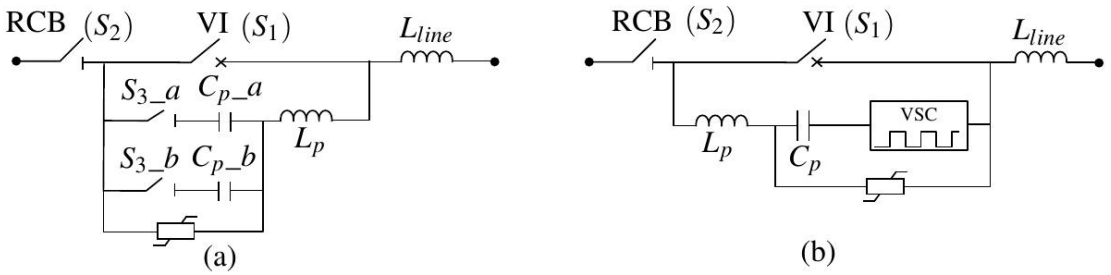

Figure 3-3 Examples of mechanical DCCBs using active resonance current injection, (a) using high speed switch for current injection [11], and (b) using VSC for current injection (VSC assisted resonance current, VARC) [12].

3.2.2 HYBRID DCCB

Hybrid DCCBs use a low loss load current branch and a commutation branch consisting of power electronic switches. Two examples of hybrid DCCBs are given in Figure 3-4. During normal operation, the load current flows through the load commutation switch (LCS, T_1) and the ultra-fast disconnector (UFD, S_1). When interrupting a current, the LCS is tripped first to commutate the current to the commutation branch (main breaker (MB, T_2) and time delaying branches in Figure 3-4 (a) and (b)). Once the current in the load current branch decreases below the residual current level, the UFD is opened. The current is interrupted by the blocking the power electronic switches in the commutation branch.

The breaker opening time is primarily determined by the opening speed of the UFD. A typical opening speed ranges from 2 ms to 3 ms [10, 16, 17]. The rated breaking current capability varies from 9 kA, 16 kA to 25 kA [10, 17, 18].

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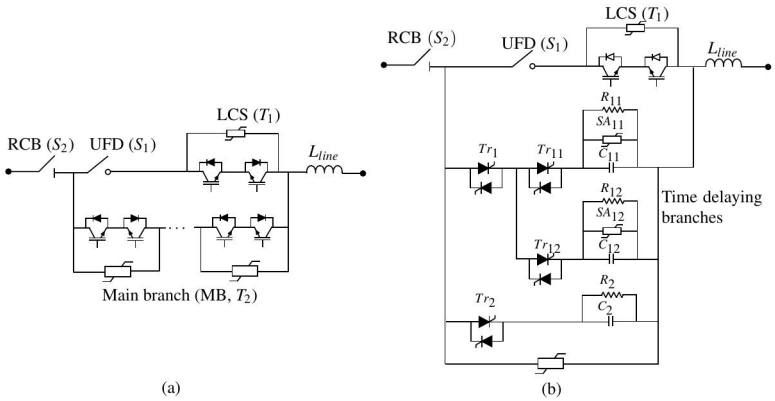

Figure 3-4 Examples of hybrid DCCBs, (a) IGBT-based [10], and (b) thyristor-based [19].

3.2.3 POWER ELECTRONIC DCCB

Power electronics-based circuit breakers are capable of interrupting a DC fault current in the microseconds range, but have high on-state losses. An example of such a breaker is the IGBT-based hybrid breaker without the load current branch [20].

3.2.4 UNIDIRECTIONAL DCCBS

Hybrid or power electronic DCCBs can be implemented either with bidirectional or unidirectional current interruption capability [21, 22]. An example topology of a unidirectional hybrid DCCB is shown in Figure 3-5 (a). The main advantage of unidirectional DCCBs is the reduced cost due to the reduced number of components. However, compared to a protection strategy using bidirectional DCCBs, a different method is required when using unidirectional DCCBs to clear busbar faults and towards providing breaker failure backup. In case of a busbar fault or breaker failure backup protection, unidirectional DCCBs at the remote line ends are required to be tripped. As a result, the system may need longer time to recovery depending on the fault detection algorithms and protection sequences. However, the general requirements for unidirectional DCCBs in terms of inductor size, breaking current, opening speed and energy absorption capability are considered similar as those of bidirectional DCCBs when used in a fully selective protection strategy [23]. Consequently, the requirements presented in this report do not differentiate between unidirectional and bidirectional DCCB. A fully selective protection strategy using unidirectional DCCBs has been analysed in detail in D4.2 [3].

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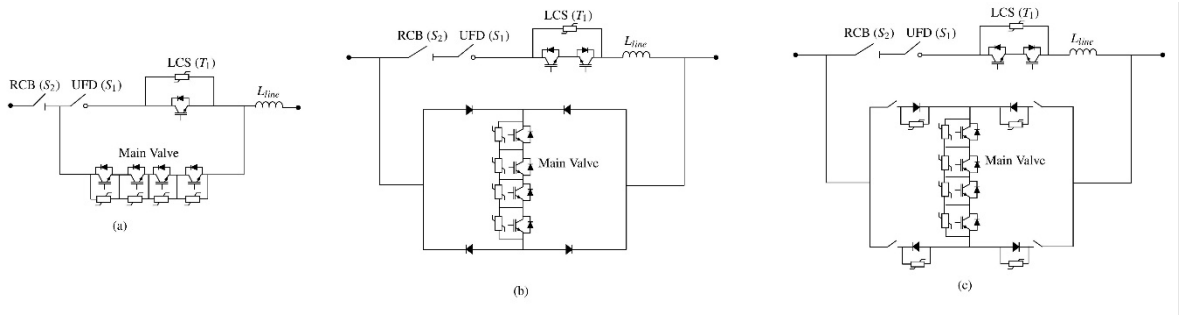

Figure 3-5 Hybrid DCCBs with different topologies: (a) unidirectional interruption capability with a single main valve, (b) bidirectional interruption capability with a single main valve (topology 1 [17]), and (3) bidirectional interruption capability with a single main valve (topology 2 [24]).

For comprehensiveness, it has to be mentioned that alternative topologies using a single main valve to provide bidirectional current interruption capability have been proposed in the literature [17, 24]. Two example topologies are shown in Figure 3-5 (b) and (c). To provide bidirectional current interruption capability, additional switches are used in these topologies, such as diodes in topology 1 Figure 3-5 (b) and a combination of UFDs and diodes in Figure 3-5 (c). These topologies offer system-level performance in the same range as a typical bidirectional hybrid DCCB, but with a reduced number of semiconductors. Bidirectional DCCBs using a single main valve may provide a viable alternative to unidirectional DCCBs in terms of interruption capability. However, the reliability of bidirectional DCCBs using a single main valve may differ as additional switches and operating control are required.

3.3 DCCB FUNCTIONS

In the literature, various breaker functions have been proposed in addition to the basic function of fault current interruption. To ensure interoperability between different breaker technologies, classify them into minimally required and auxiliary functions has been proposed in [25]. The minimally required functions are referred to those that any DCCB is required to fulfil for HVDC grid protection applications regardless of the employed technologies. By contrast, the auxiliary functions are optional by definition and not required for all types of DCCB technologies. These functions can be used in HVDC grids to improve the performance of the protection system. Both types of functions are briefly summarized in this section.

3.3.1 MINIMALLY REQUIRED FUNCTIONS

- Current interruption: interrupt a DC current upon receiving a trip order.
- Close operation: close upon receiving a closing order.
- Repeated O-C-O operation: a DCCB is required to have a repeated O-C-O capability upon receiving trip-closing-trip order from the IED, in case of backup protection, overhead line applications, or required by the protection strategy, such as the non-selective strategy using converter terminal DCCBs and the open grid strategy [26, 27].

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- Monitoring and communication: a DCCB is required to monitor and communicate breaker status (such as, open/close and ready-to-operate) to its associated IED(s) for protection coordination and the SCADA/EMS system for grid operation.

3.3.2 AUXILIARY FUNCTIONS

- Proactive opening: refers to the capability of a DCCB to proactively open the load current branch and commutate the current to the main branch upon receiving an initiating signal from the IED, prior to the fault being identified on the line [10]. The DCCB is also required to abort the proactive opening and revert to normal operation, preferably without causing voltage and current transients if the fault is not identified on the line.
- Fast reclosing/reopening: refers to the capability of a DCCB to keep certain component(s) in close/open position to perform fast reclosing/reopening. For instance, the DCCB can keep the RCB in closed position during an O-C cycle in case of breaker failure backup operation to eliminate the opening and reclosing delay of the RCB, or keep the load current branch in open position to achieve fast second opening during an O-C-O cycle [9].
- Fault current limiting (FCL) mode: refers to the capability of a DCCB to control the DC current to desired values during a fault or DC voltage restoration [28, 29, 30, 31, 32].
- Breaker failure internal detection: refers to the capability of a DCCB to internally monitor and detect a breaker failure during current interruption [33].
- Self-protection: this function entails two sub-functions: (1) opening without a trip order from the IED. In case of abnormal operating conditions, such as thermal overloading of power electronics or surge arresters, the DCCB may be required to trip without the receipt of an external trip order [9], and (2) remaining in closed state even with a trip order. Although the DCCB is ordered to open by an external trip order, the DCCB closes itself again during the opening process if its internal monitoring predicts the DCCB is not able to interrupt the fault current [33, 34].
- Driver-level protection: this function is implemented at the gate unit driver level, to trip the power electronic switches if the current and/or voltage exceed the pre-determined thresholds. The aim of the driver-level protection is to prevent the power electronic switches from irreversible damage, but maybe at the expense of damaging the protective surge arresters [35].

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4 REQUIREMENTS OF DCCB IN A FULLY SELECTIVE PROTECTION STRATEGY

4.1 DESCRIPTION OF THE STRATEGY

The fully selective protection strategy using DCCBs is studied in detailed in the PROMOTioN work package WP4 deliverables, D4.2 [3] and D4.3 [4]. The description of the strategy is briefly summarized in this section. In a fully selectively protected HVDC system, DCCBs are installed in both ends of each line to selectively protect each line. In addition, DCCBs can be installed at the converter terminal ends to provide fast breaker failure backup protection for DC busbars with two or more lines. Key components and their locations are illustrated in Figure 4-1. The primary protection sequence involves in

(1) fault detection and identification by the relevant IEDs,
(2) tripping the associated DCCBs to clear the fault
(3) system recovery

In case of a line breaker failure, the backup protection sequence includes

(1) breaker failure detection
(2) tripping backup DCCBs. At the meantime, for the isolated converter, maintaining connection to the AC-side. This will require switching control mode if the pre-fault control mode is in active power control.
(3) opening the disconnector of the failed DCCB for isolation
(4) reclosing backup DCCBs and controlling the converters for system restoration

In case of a pole-to-ground fault in high-impedance grounded system, an extra step of rebalancing the pole voltages is needed using either AC-side groundings or DC-side dynamic braking systems (DBSes), as described in [36, 37].

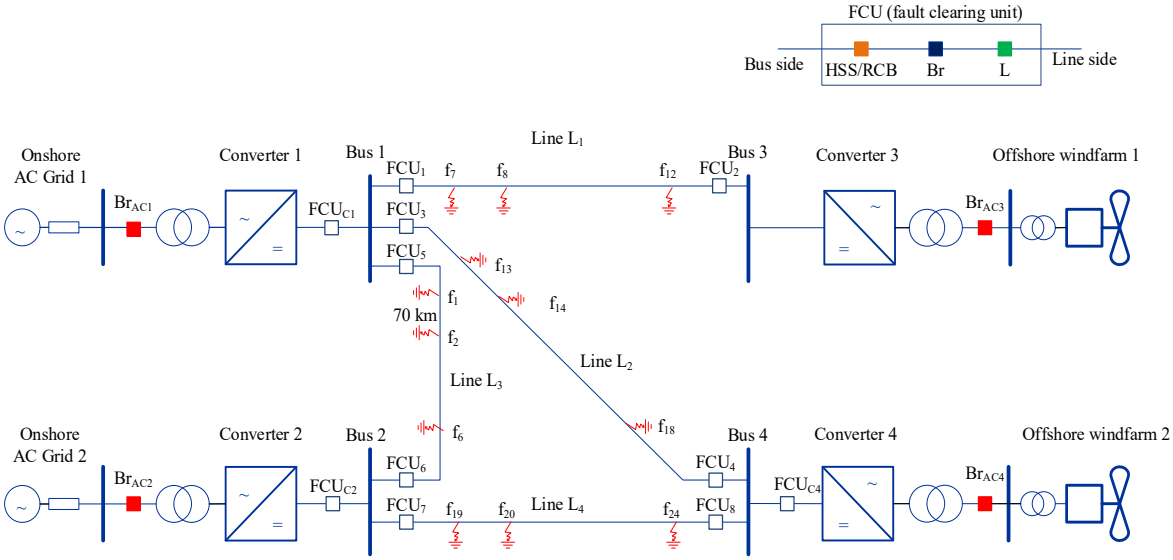

Figure 4-1 Key components locations for fully selective fault clearing strategies employing DC circuit breakers. The equipment for two backup options are included (using converter side DCCB: converter 1,2, and 4 or using converter side ACCB: converter 3).

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Depending on the type of transmission lines, system configuration and grounding scheme, and the type of faults to be considered, two application scenarios are identified using a fully selective protection strategy, namely:

(1) HVDC systems requiring DCCBs to deal with both pole-to-pole and pole-to-ground faults. This scenario requires Type-I DCCBs: fast DCCBs with short-circuit current interruption capability to quickly clear the faults to minimize the impact on the overall HVDC grid.

(2) High-impedance grounded cable-based HVDC systems requiring DCCBs to deal with only pole-to-ground faults. This scenario provides a possibility to use Type-II DCCBs: slow DCCBs with low current interruption capability for clearing pole-to-ground faults to achieve a cost-effective DC grid protection system.

The general requirements of DCCBs used in partially selective protection strategies are considered to be similar as those in fully selective protection strategies. Therefore, the requirements of the DCCBs used in fully selective protection strategies are discussed in detail in the following sections. First, generic requirements of DCCBs in fully selective protection strategies are summarized in section 4.2. These generic requirements apply to both Type-I and Type-II DCCBs. Then specific aspects of the Type-I and Type-II DCCBs are discussed in section 0 and section 0, respectively.

4.2 GENERIC REQUIREMENTS OF DCCBS IN FULLY SELECTIVE STRATEGIES

In a fully selective protection strategy, DCCBs need to operate in conjunction with the overall system to achieve successful DC fault clearing and good restoration performance. When dimensioning the DCCBs, in particular to determine the required opening speed, breaking current capability, series inductor size and energy absorption capability, it is necessary to consider the requirements or constraints from the HVDC grid and its components. Generally speaking, the DCCBs are required to be dimensioned considering the following constraints:

- Converter DC fault-ride-through (DC-FRT) requirements: converters in the HVDC grid may be required to have different DCFRT characteristics, for instance, allowed to be temporarily blocked or not. As the series inductors associated with the DCCBs have a significant influence on the currents in the converters during a DC fault, the converter DC-FRT requirements in turn impose minimally required series inductances.
- Selectivity requirements: the series line inductors are often used to separate different protection zones to allow for selectivity of non-unit protection algorithms. To ensure the selectivity of the protection algorithms, certain series inductor sizes are required.
- HVDC system stability requirements: the series line inductors have influence on the system dynamics, and hence can have impact on the system stability.
- Multivendor interoperability requirements: key components, such as converters and DCCBs are likely to be provided from multiple vendors in a HVDC grid. Multivendor interoperability of DCCBs should be ensured when dimensioning these DCCBs.
- Protection coordination requirements from system-level and DCCB-level functions: some DCCBs may use fault detection and protection functions internally within the DCCBs, such as self-protection and driver-level protection. These DCCB-level functions should be coordinated with system-level protection

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by the IEDs. Additional series inductances may be required to allow for proper coordination of the DCCB-level and system-level functions [38].

In the remainder of this section, the aforementioned constraints are discussed individually to demonstrate their impact on DCCB dimensioning. The intersections of the DCCB requirements imposed by these constraints should be selected to fulfil all the constraints.

4.2.1 CONVERTER DC FAULT RIDE THROUGH REQUIREMENTS

Depending on the overall power system requirements of the HVDC network and the connected AC systems, there is an explicit or implicit requirement on the converter behaviour following a fault. A HVDC system connected to a weak AC system (i.e., the power ratings of the HVDC system are relatively large compared with the AC system) might lead to a requirement that converter stations are able to continuously operate following a line fault, such that the HVDC system is able to continuously provide power to the connected AC system. Conversely, a relatively small HVDC system connected to a strong AC system might have no requirement to support the AC system and therefore there is no requirement for converter fault ride through capability in this scenario.

When designing the HVDC protection system, there are several design choices and hardware limitations that change the impact that the HVDC fault has on the healthy network and converters. Importantly, fault current limiting inductors are expected to be applied at each DCCB location on the HVDC network such that the DCCB is able to operate correctly. The increased system inductance slows the rate of change of fault current and therefore results in a longer time before the HVDC converter is required to block its submodules. On the other hand, the speed of the DCCB can also result in differing system-level consequences following a DC fault. From a protection system design perspective, a very fast DCCB would typically cause the least system level impact following a fault. The design of the converter station itself also has an impact on the protection system design – depending on the converter configuration/design, the inductance and capacitance within the converter, the overcurrent rating and the self-protection settings, the converter might be less or more sensitive to DC-side faults. In this work the design of the converter station is considered constant, although in the future it may be of interest to consider how the converter station design and control could be adapted according to different protection strategies.

The eventual HVDC protection system requires a co-design between the circuit breakers and the additional inductors, taking into account the constraints of the HVDC converter station. The approach taken in this section is to constrain the circuit breaker operation time and maximum current rating to known industrial DCCB designs, and vary the additional inductance at each DCCB in order to meet various fault ride through requirements. Fault ride through scenarios are defined based on the fault response imposed on converter topologies according to their location relative to the fault. The fault ride through scenarios are an extension of the ‘Continuous Operation’ (CO) and ‘Temporary Stop’ (TS) concepts used previously in WP4 and in the forthcoming CENELEC document CLC/TS 50654-1 [39, 40]. Here TS refers to a state for which the converter is blocked and cannot control power, but the AC-side is not necessarily isolated such that following DC-side fault isolation the converter could rapidly unblock. Several fault ride through scenarios are considered, each of which was developed in reference [41]:

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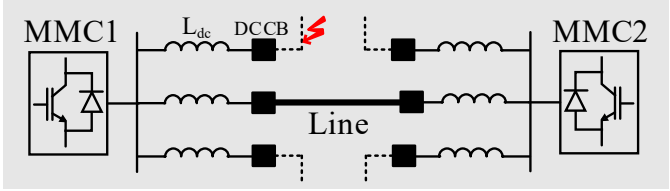
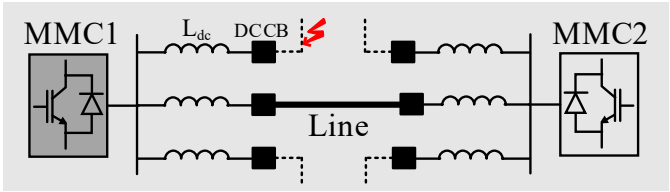
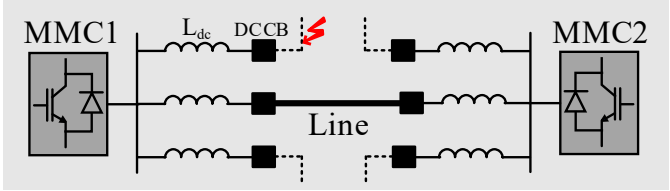
- **DC fault ride through scenario 1 (DC-FRTS1)** is the most strict requirement and means that all converters must remain in CO following a DC fault (Figure 4-2 (a)). This implies little to no interruption to the operation of the remaining healthy network. In practical implementations this often leads to a requirement for very large inductors across the network. The minimal protection matrix for DC-FRTS1 on the small impact HVDC system is shown in the annex (Table 9-1).
- **DC fault ride through scenario 2 (DC-FRTS2)** allows for converters connected directly to the faulted element to be temporarily blocked (TS), but all other converters must remain in CO (Figure 4-2 (b)). This implies some interruption to the operation of the remaining healthy network, although this interruption could be momentary. The inductance required for this scenario is likely to be larger than required just for DCCB operation, although might provide a good compromise between inductor size and fault impact. The minimal protection matrix for DC-FRTS2 on the small impact HVDC system is shown in the annex (Table 9-2).
- **DC fault ride through scenario 3 (DC-FRTS3)** is the least strict requirement and allows all of the converters to TS (Figure 4-2 (c)). In this scenario, the inductors should be chosen considering the operational limits of the anti-parallel diodes in the MMCs. The minimal protection matrix for DC-FRTS3 on the small impact HVDC system is shown in the annex (Table 9-3).



(a) DC-FRTS1: all converters are prohibited from blocking



(b) DC-FRTS2: converters connected directly to the faulted line are allowed to be temporarily blocked



(c) DC-FRTS3: all converters are allowed to be blocked temporarily

Figure 4-2 Illustation of converter DC-FRT scenarios (converters allowed to be temporarily blocked are grayed-out) [41].

The methodology proposed in [41] to calculate the minimally required inductor values for each DC-FRT scenario is summarized in Annex 8.1, with examples calculated for the PROMOTioN small impact network. An example extracted from [41] is given in Figure 4-3 to demonstrate the scale of the DCCB requirements depending on the DC-FRT scenarios. Although the exact values vary for each HVDC grid, this example, calculated for a five-terminal HVDC grid, gives a good indication of the ranges.

- DC-FRTS1 leads to high values of line inductors (e.g. > 300 mH) for the given five-terminal HVDC grid test system, which may be impractical towards real applications.

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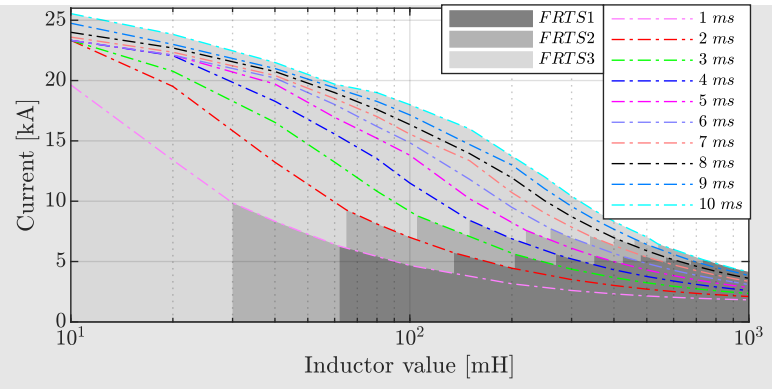
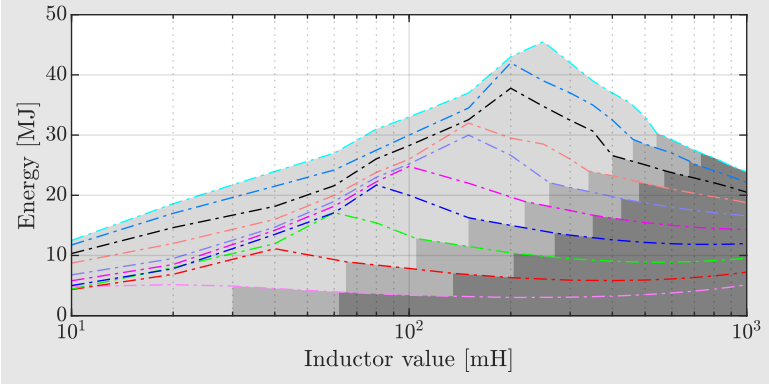
- DC-FRTS2 reduces the requirements for the line inductors in the grid for all DCCB operating times. Particularly for ultra-fast DCCBs (e.g. 2 ms), the required inductor value is about 65 mH in the test system. However, it shows higher line inductor values for longer DCCB operating times in combinations with low converter ratings (e.g. > 500 mH for a DCCB with opening time of 10 ms in the test system).
- DC-FRTS3 can be used for any HVDC grid with any DCCB technology, and the DCCB operating time and line inductor value can be determined depending on the allowable fault level in the grid (e.g. 10 mH can be used with DCCBs with opening times from 1 ms to 10 ms in the test system).



(a) Breaking current requirement



(b) Energy absorption requirement

Figure 4-3 An example of breaking current and energy absorption requirement in relationship to series inductor for a particular network configuration and network location, for the three DC-FRT scenarios [41].

4.2.2 SELECTIVITY REQUIREMENTS

In a fully selective protection strategy, series line inductors are often used to separate different protection zones to allow for selectivity of non-unit or communication-less protection algorithms relying only on local measurements, since the series line inductance has a great influence on the voltage and current waveforms seen at the IED location. The series inductor should be selected to allow enough margin for selective fault detection, considering the selected detection algorithms and worst fault scenarios. The impact of the series line inductor on fault discrimination has been analysed in detail in [42, 43]. A DC protection IED has to discriminate an internal fault (F_1) from external faults (F_2 and F_3) as illustrated in Figure 4-4.

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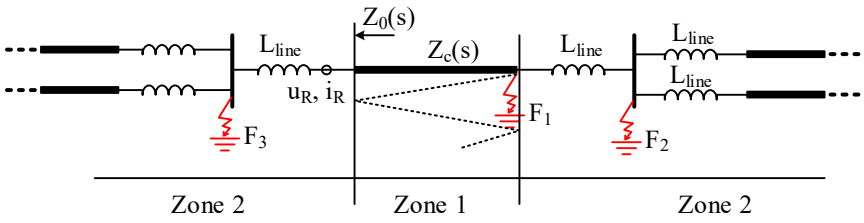

Figure 4-4 Example cable-based system with inductive termination and faults.

Regardless of the used non-unit protection algorithms, the series line inductor is required to be large enough so that the fault voltages due to an internal and an external faults at F_1 and F_2 can be discriminated [42]. The fault voltages at fault location F_1 and F_2 are expressed as equation (2). The difference between an internal fault and an external fault is that the line inductor filters out high frequency components of the fault voltage, whereas the fault resistance R_f provides damping overall the whole frequency spectrum [42].

$$\begin{cases} U_{fault,F_1} = \dfrac{Z_c(s)/2}{R_f + Z_c(s)/2}(-U_0) \\ U_{fault,F_2} = \dfrac{Z_c(s)}{sL + Z_c(s)}(-U_0) \end{cases} \quad (1)$$

For non-unit algorithms without directional elements, such as voltage derivative [44], the line inductance is required to be large enough so that it is possible to discriminate an internal fault F_1 from an external fault F_3. Voltage measured at the IED position due to faults at F1 and F3 can be calculated by equation (3).

$$\begin{cases} U_{R,F_1}(s) = \dfrac{2Z_0(s)}{Z_0(s) + Z_c(s)} \times H \times U_{fault,F_1} \\ U_{R,F_3}(s) = \dfrac{Z_c(s)}{sL + Z_c(s)}(-U_0) \end{cases} \quad (2)$$

Where $Z_0(s)$ is the total equivalent impedance seen from the IED location and H is the propagation matrix.

A generic methodology to calculate the voltage at the IED position is given in [43] for various HVDC system configuration and grounding schemes. The voltage measured at the IED position is attenuated when travelling along the cable, resulting in a damped voltage derivative. This effect is particularly evident for a long cable. Examples simulated on the PROMOTioN small impact network are given in Annex 8.2. The selective requirement on the series inductor is not likely to be the dominant factor compared with the converter DC-FRTS1 and DC-FRTS2 requirements, but may fall in a similar range with the DC-FRTS3 requirement particularly for long cables.

4.2.3 HVDC SYSTEM STABILITY REQUIREMENTS

The line inductors associated with the DCCBs have influence on the system dynamics, and hence can have impact on the system stability. Consequently, the choice of the line inductor sizes needs to take into account system stability aspects in addition to the DC fault current and energy handling requirements.

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In a multivendor environment employing a fully selective protection strategy, where a combination of different types of DCCBs can be employed on different lines, and the size of the line inductors associated with the DCCBs can also vary depending on whether the DCCBs have slow or fast operating times.

In HVDC grids employing DC voltage droop control strategy, the use of larger line inductors associated with slower DCCB's would extend the electrical distance between converter stations and can have an influence on the DC voltage control and thereby potentially affecting the stability of HVDC grids.

In HVDC grids, which are selectively protected by DCCB's which require the use of larger line inductors, the dynamic behaviours of DC voltages at different DC terminals may differ significantly, mainly due to the increase of line inductors. This can effectively slow down the propagation of dynamic changes of DC currents from one DC terminal to the other.
Thus, the introduction of large dc reactors throughout a HVDC grid can have a significant impact on its stable operation and may require additional damping controls to damp out oscillations during the system recovery process [45].

During severe transients and during the system restoration process following outages of faulty lines or blocking of converters by protective actions, the HVDC grid effective impedance seen by each converter would change and consequently the interactions with the MMC controls following the system changes might lead to instability depending on the following factors [45]:

1. **The type of HVDC grid controls used**: The type of DC voltage control strategy followed in an HVDC grid can lead to different dynamic behaviours under the presence of large line inductors. In HVDC grids employing DC voltage droop control strategy, the droop gains need to be carefully selected, as larger proportional gains can affect the system damping and can even lead to instability, especially in the presence of large line inductors.

   In addition, the bandwidth of the outer controllers such as the active power controller or the DC voltage controllers needs to be selected based on detailed studies involving both dynamic and steady state performance of the HVDC grid under the presence of large line inductors.
2. **The length of the DC lines**: The length of the DC Lines can have influence on the dynamic performance of the HVDC grid. The longer DC cables can lead to larger equivalent capacitances and resistances in the DC system, and can help improve the damping in the DC system.
3. **Power flow direction:** Power flow direction has influence on the stability of MMCs, and hence, the system stability needs to be verified by testing different power flow scenarios during the selection of suitable line inductor sizes.
4. **HVDC grid contingencies:** When lines are disconnected by a protective action, the equivalent impedance seen by each MMC changes, and hence might lead to instability. On the other hand, if converters are blocked or taken out of service, their participation in stabilizing the system after the disturbance is lost, and this can worsen the system stability.

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5. **The bandwidth of the MMC controls:** In cases where the MMC outer controls are tuned to have a high bandwidth, the use of larger DC line inductors in such systems can affect system stability, and hence the control bandwidth may need to be reduced in order to guarantee stability, unless additional controls such as damping controllers are employed to enhance system stability [4].

The above-mentioned factors can be studied by either small signal stability analysis of the HVDC grid, and performing the root locus stability analysis with variation of line inductor sizes, droop gains, etc. and or by checking the frequency response of the HVDC grid, based on impedance based analysis.

In general, the line inductors associated with DCCBs can influence the system stability and are very system specific, and hence, the selection of the DC line inductor sizes need to be coordinated with the design of the HVDC grid control and the selection of control bandwidth. In some cases, the use of additional damping controls might be required to stabilize the HVDC grid, which used large line inductors [46].

4.2.4 MULTIVENDOR INTEROPERABILITY REQUIREMENTS

All key components in a HVDC grid can be provided by multiple vendors. DCCBs are required to operate in such multivendor grids. When dimensioning a DCCB in a HVDC grid, it is necessary to take the allowed operation range/characteristics of these key components into consideration, as these operation ranges may have an impact on the fault responses seen by the DCCB.

- Other DCCBs in the network: When dimensioning a DCCB in an HVDC grid, it is necessary to take the allowed operation range of other DCCBs (in particular, opening speeds and series inductor sizes) into consideration, as these operation ranges may have an impact on the fault responses seen by the DCCB. Design margins may be required to fulfil multi-vendor interoperability requirements. Examples simulated in the PROMOTioN small impact network are given in Annex 8.3. The examples show that using mixed DCCB technologies in a HVDC grid is a feasible option, however, the performance of the HVDC grid and requirements on the DCCBs vary depending how the HVDC grid is designed. Replacing a fast DCCB with an ultra-fast one in a HVDC grid using all fast DCCBs can generally improve the performance of the HVDC grid during DC faults. However, the breaking current and energy requirement of the fast DCCB at the remote end may be increased due to the replacement.
- Converter DC fault response: As the DC fault responses of the converters play a key role in determining the overall fault current shape and level in a HVDC grid, it is necessary to represent the converters in an accurate manner when dimensioning a DCCB. Although specifications on converter behaviour are expected to be established for the future HVDC grid, differences such as arm inductances, availability of active DC fault control may still exist among different vendors [47]. DCCB dimensioning studies should be performed with preferably full knowledge of the converter behaviour or alternatively with the specified ranges.
- Pole rebalancing equipment limited to high-impedance grounded systems: both AC-side groundings and DC-side dynamic braking systems are demonstrated to be viable options for pole voltage rebalancing following a pole-to-ground fault in fully selective protection strategies [36]. These devices are likely to

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have an influence on the fault current seen by the DCCB. DCCBs (particularly Type-II DCCBs) should be dimensioned considering the choice of the pole rebalancing equipment and possible future refurbishment planning.

4.2.5 PROTECTION COORDINATION REQUIREMENTS OF HYBRID DCCBS

As described in section 3.3, some hybrid DCCBs are capable of providing auxiliary functions such as self-protection, driver-level and breaker failure internal detection. These auxiliary functions are required to be coordinated with the system-level protection by the IEDs to ensure a reliable protection system. A coordinated protection scheme has been investigated taking these DCCB-level protections into consideration by a joint work between WP4 and WP6 [38]. Although the analysis is carried out using one of the hybrid DCCB topologies, the approach is considered generally applicable for hybrid DCCBs with DCCB-level protection of the power electronic switches.

DCCB self-protection function can be treated as IED failure backup protection, in the case when the primary protection IEDs have failed. A safe operation margin should be designed to allow the system-level protection (main protection IEDs) to operate first, the DCCB will only be tripped by its self-protection function when the maximum expected IED time has elapsed. DCCB driver-level protection in principle should be avoided due to possible damage to the components, which entails additional safe operation margin for the breaker failure backup protection. As a consequence, additional series inductance may be required due to allowing for coordination between DCCB- and system-level protection functions, as compared to using the same DCCBs without enabling DCCB-level protection functions. Relevant results on DCCB requirements from [38] is summarized in Annex 8.4.

4.3 REQUIREMENTS FOR TYPE-I DCCB

Type-I DCCBs are required to deal with both pole-to-pole and pole-to-ground faults in a fully selective strategy, regardless the system configuration and grounding scheme. Fast DCCBs with short-circuit current interruption capability are required to clear the DC fault as soon as possible to minimize the impact on the overall HVDC grid. The exact values for the opening speed, breaking current, inductor size and energy absorption capability are system dependent and should be studied considering the generic requirements described in section 4.2.

From the relevant studies in D4.2, D4.2 and the public domain, the required opening speed for this application is typically less than 10 ms. The required inductance due to converter DC-FRT, selectivity and protection coordination with DCCB-level protection is summarized in Table 4-1. The required inductance is likely to be less than few hundreds mH considering the dynamic performance and stability of the HVDC grid.

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Table 4-1 Requirement of series inductance for Type-I DCCBs

	DC-FRTS1	DC-FRTS2	DC-FRTS3
Converter DC-FRT	Hundreds mH (Not practical)	Tens mH to hundreds mH (for $t_{br,o}$=1 ms to 10 ms; however it may not be practical for $t_{br,o}$> 5ms as the required large inductance)	~ 10 mH ($t_{br,o}$≤ 10 ms)
Selectivity	~tens mH		
Protection coordination with DCCB-level protection (specific for hybrid DCCBs)	~tens mH		

The breaking current and energy absorption requirements are closely dependent on the breaker opening speed and required inductance. The breaking current requirement is likely to be in the range of 10 kA to 25 kA, and the energy absorption requirement can range from few MJ to few tens of MJ.

4.4 REQUIREMENTS FOR TYPE-II DCCB (POLE-TO-GROUND FAULTS IN CABLED-BASED SYMMETRICAL MONOPOLAR SYSTEMS)

This section focuses on specifying general requirements for type-II DCCBs used in a high-impedance grounded cable-based HVDC grid. In cable-based symmetrical monopolar systems, the probability of occurrence of pole-to-pole faults is considered extremely low. This provides a possibility to design a cost-effective HVDC grid protection system using DCCBs to only deal with pole-to-ground faults. In such scenario, the DCCBs are placed at the both ends of a cable to form a fully selective strategy to handle pole-to-ground faults. Although the probability is extremely low, if a pole-to-pole fault occurs, ACCBs at the converter side can be used to clear the fault, yielding a non-selective fault clearing for pole-to-pole faults [36]. The key components and their locations are the same as illustrated in Figure 4-1. Differ to a low-impedance grounded system, pole rebalancing equipment (e.g. AC-side groundings or DC-side dynamic braking systems) is necessary in high-impedance grounded system to rebalance the pole voltages following a pole-to-ground fault.

As similar generic requirements as described in section 4.2 also apply to Type-II DCCBs, series inductances in the similar range (or less as pole-to-ground faults may result in less severe fault currents) as summarized in Table 4-1 are likely to be applicable to Type-II DCCBs, designed to only deal with pole-to-ground faults in cable-based symmetrical monopolar systems as well.

An example of the pole-to-ground fault response is given in Figure 4-5, considering three inductor sizes and six fault locations indicated in the PROMOTiON small impact test network. The DC line and bus surge arresters are put out of service in these simulations to show the prospective system response without protection. The fault current shows a damped oscillation through the arm resistance and inductance with large amplitudes due to cable and MMC submodule capacitors discharge. If fast breakers are only dimensioned for pole-to-ground faults, high interruption capabilities are still needed. However, if slow DC circuit breakers (≈ 20 ms) are used, the required

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breaking current capability is only a few kA, regardless of the series inductor size and fault location. The slow DCCBs are also required to withstand a high transient current before current interruption for a short time. The trade-off of employing slow DC circuit breakers is the complete discharge of the faulted pole, which imposes larger duties to the pole rebalancing equipment and DC side surge arresters, longer recovery time and higher overvoltage stress to the healthy pole cables.

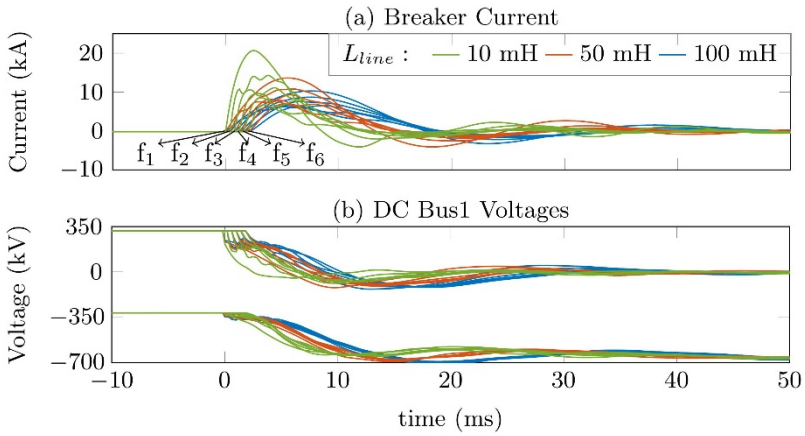

Figure 4-5 Fault current in Br_5 and bus voltage during pole-to-ground faults (fault location: f_1 to f_6 on cable L_3, DC line/bus surge arresters are put out of service to illustrate the overvoltage).

As an example, the impact of the line inductor is shown in Figure 4-6, for a pole-to-ground fault on cable L_3 applied at the cable terminal near DC busbar 1 in the PROMOTioN test network. The DCCB Br_5 will operate upon primary protection, while the DCCB Br_6 is disabled to emulate a breaker failure and the pole rebalancing equipment is implemented at the two assumed onshore station MMC1 and MMC2. For each study, only one of the options, DBS or AC grounding, is activated. The protection sequence is described in D4.3 [4, 36, 37].

For the primary protection DCCB (Br_5), the required breaking current capability is about 6 kA and is not significantly influenced by the inductor size. This indicates that a small inductor size can be used for a slow DCCB in this application. For the backup DCCBs (Br_7 and Br_{C2}), using smaller line inductor size is also preferable as the energy absorption requirements of the backup DCCBs are lower.

To summarize, for Type-II DCCBs used in a high-impedance grounded cable-based HVDC grid, the feasible ranges of breaker opening speed and breaking current capability are in the order of 20 ms and few kA, respectively. System studies are needed to specify the exact requirements for the DCCBs in a given HVDC system.

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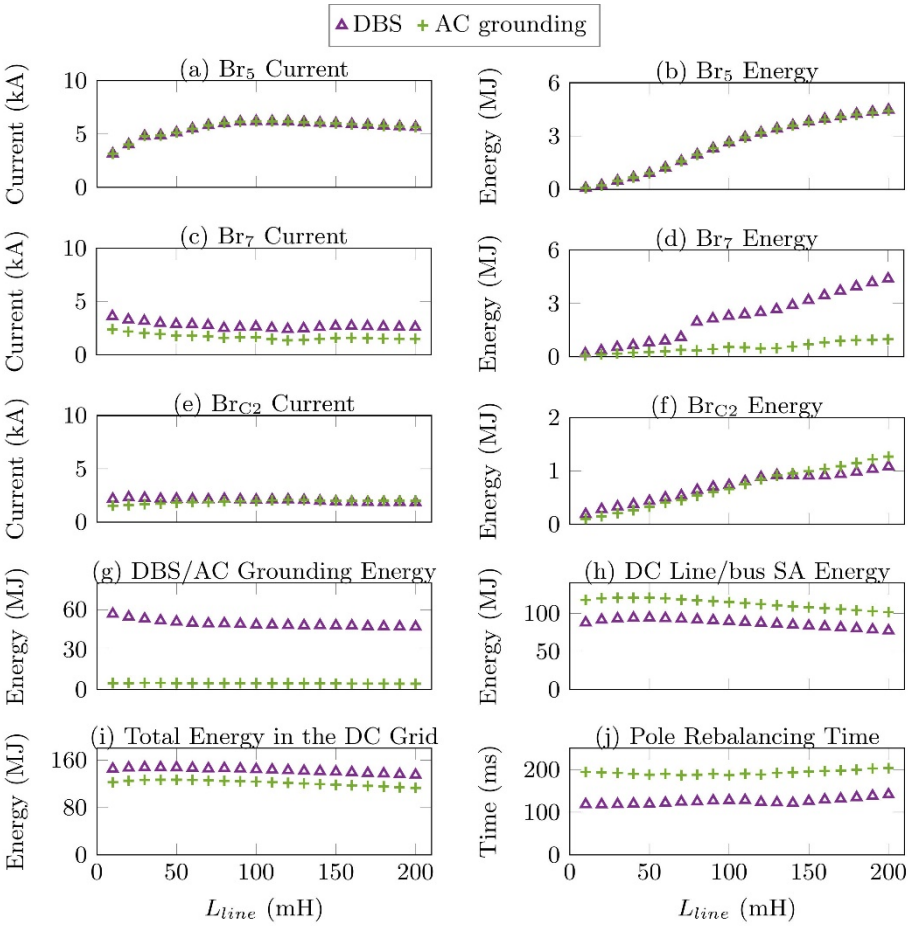

Figure 4-6 Impact of series inductor size on breaker requirement and pole rebalancing performance ($t_{br,o}$ = 20 ms).

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5 REQUIREMENTS OF DCCB IN A NON-SELECTIVE PROTECTION STRATEGY

5.1 DESCRIPTION OF THE STRATEGY

This chapter gives an overview of technical specification for the DC switchgear to be used in the non-selective fault clearing strategy named Converter Breaker Strategy. The protection strategy has been studied in depth in D4.2 [3], D4.3 [4] and results have also been presented in [26].

This non-selective fault clearing strategy uses Converter Breaking Modules (CBM) at each converter output and Line Breaking Modules (LBM) at each line end. Every CBM and LBM is equipped with a mechanical DC Circuit Breaker and a Residual Current Breaker (RCB). In addition, each CBM contains a Pre-Inserted Resistance (PIR) that assures a smooth voltage restoration and prevents a re-blocking of the MMC after reclosing. Figure 5-1 illustrates the location of the described components.

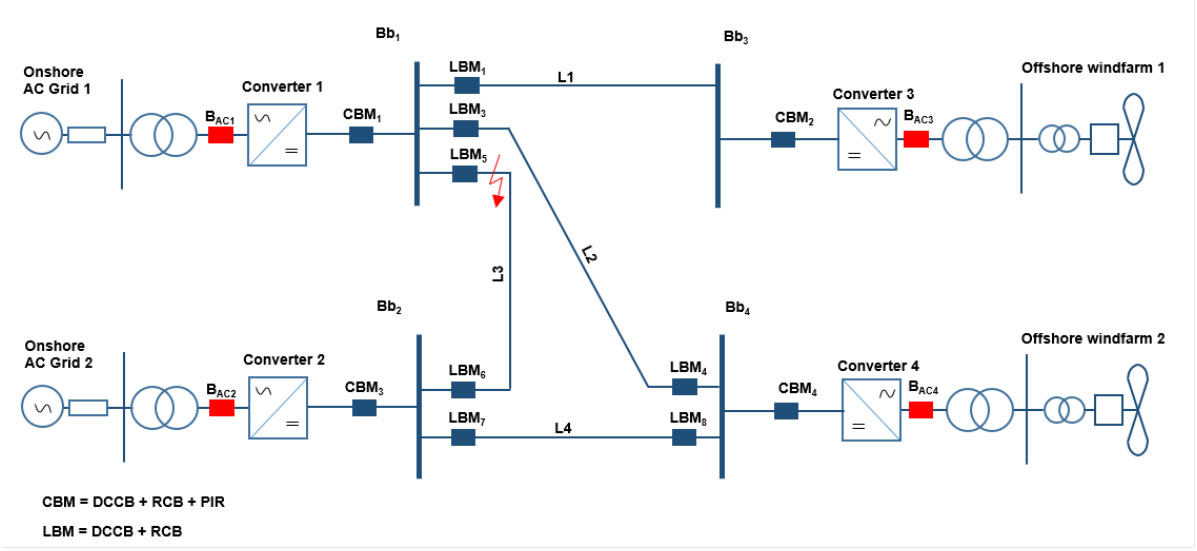

Figure 5-1 Illustration of key component locations in benchmark grid

The primary protection sequence involves the following steps

(1) fault detection by all the CBM relays
(2) block the MMCs and trip the associated DCCBs of all the CBM in order to suppress the fault current contribution from converters
(3) fault identification by the LBM of the faulty line
(4) trip of the DCCBs of the faulty line
(5) de-block the MMCs and reclosing of all the CBM
(6) Voltage and power restoring

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Because the primary protection strategy is an assembly of few protection sequences, it might be the case that some failures happen during the fault clearing or power grid restoration and a backup sequence providing an alternative to continue with the process need to be defined. In this document two main backups have been studied:

- converter breaker fails to open
- line breaker fails to open

In case of one converter breaker failure, its associated MMC remains blocked and maintains the contribution to the fault current until the isolation of the faulty line by the associated LBM. Indeed, because of the disconnection of all other converters stations, the line breakers of the faulty line can eliminate the fault since they are designed to clear the contribution coming from one converter. The sequence for the LBM and all the healthy CBMs is therefore the same as during primary sequence. Once the fault is eliminated, the faulty CBMs can open the RCB in order to isolate the converter from the DC grid.

In case of line breaker opening failure the sequence is the same as for the primary sequence. Indeed, even if a line breaker fails to open, the fault current is still cleared by the converter breaker. The RCB associated to the failed line breaker will open when the RCB opening conditions are ensured and it will isolate the faulty line.

The Converter Breaker Strategy can be applied for both symmetric monopolar and bipolar configurations as described in [4] and [48]. A Pole-to-Ground (PTG) fault in a bipolar system leads to high steady state fault currents and therefore it entails significant constraints on the DC circuit breakers. The behaviour of the fault current during a Pole-to-Pole (PTP) fault in a symmetric monopole is similar to the behaviour of a PTG fault in bipolar systems. Hence, for PTP faults in symmetric monopole configurations, a switchgear design similar to the protection strategy for bipolar configuration can be used. A PTG fault in a symmetric monopole involves sustained overvoltages on the healthy pole but will not lead to high steady state fault currents. For all these reasons the next chapter will present the switchgear technical specifications for a bipole configuration.

5.2 COMPONENT DESIGN

An example of possible components that can be used in a CBM and LBM is presented in Figure 5-2. In this case it is shown a current injection mechanical DCCB, but other technologies can be implemented.

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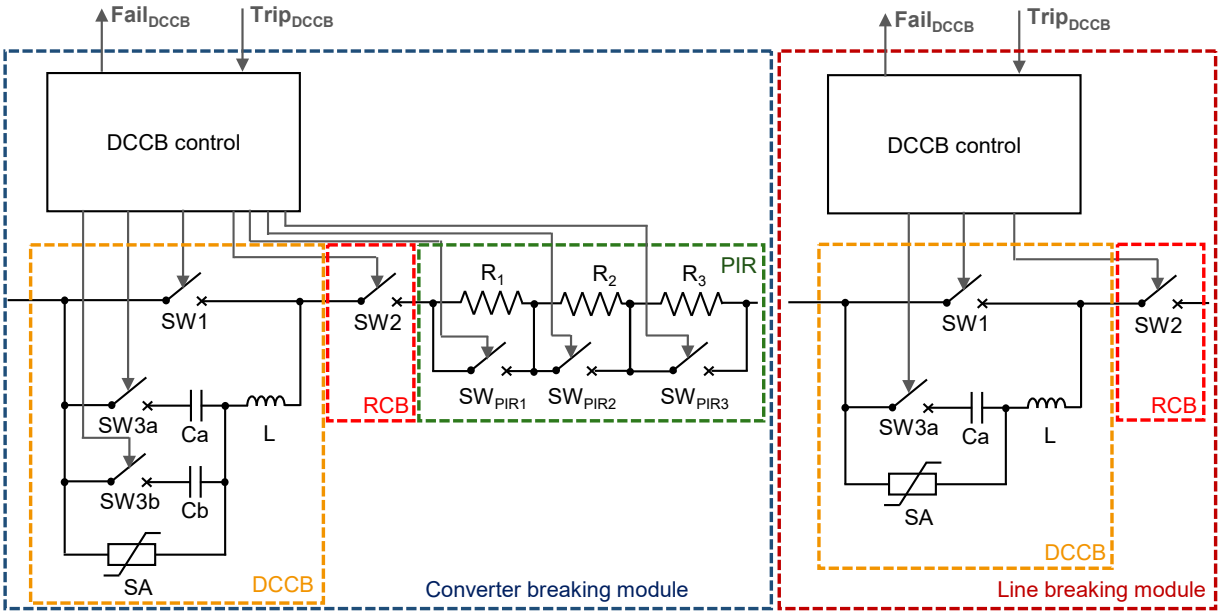

Figure 5-2 Schema of converter breaking module and line breaking module

5.2.1 CONVERT BREAKER AND LINE BREAKER (TYPE-III DCCB)

Table 5-1 shows the requirements for converter breakers and line breakers. Those values have been proposed in order to cope with primary and backup sequences in case of converter breaker failure and line breaker failure. The converter and line breakers need to be designed considering the maximum DC fault current contribution coming from a MMC converter when there is a short circuit at its terminals. The rated voltage and the arm inductance value are the main parameters that influence the peak fault current in case of a short circuit at the DC side of an MMC. Considering a design of MMC arm inductances that allows a maximum short circuit current of 20 kA, the breaking capability of DC breakers is defined at this value. Because the converter output fault current is intrinsically limited, the breaker operation time can be fixed to 20 ms without need of ultra-fast operation. It is worth to note that different values of breaker operation time (e.g. 10 ms or 30 ms) would also be acceptable. Faster breaker operation would accelerate the protection sequence but in turn would need more expensive breakers. An advantage associated with this strategy is that DC limiting reactors in series with the breakers are not necessary, which entails low energy absorption requirement for the surge arrester in parallel with the breaker.

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Table 5-1 Requirements for converter and line breakers in non-selective protection strategies

	Converter DCCB	Line DCCB
Breaking capability	20 kA	20 kA
Breaker operation time	20 ms	20 ms
DC limiting reactor	Not required	Not required
Short time withstand current	20 kA	40 kA
Transient interruption voltage	480kV (1.5pu)	480kV (1.5pu)
Surge arrester energy requirement	7 MJ	<1 MJ
Open-close operation	O - 50ms - CO	O - 150ms - CO

The Short Time Withstand Current (STC) is the let through current that the DC breaker has to withstand in closed position. This is an important input data for the design of the permanent contact of the breaker. For the converter breaker, in case of breaker failure or missing tripping order, the STC could reach up to 20kA. For the line breaker the STC can be higher than 20kA and two aspects have to be considered for the STC calculation: (i) the line stray capacitor discharge into the fault and (ii) the fault current contribution from the converter that lasts until the opening of the converter breakers. It is worth noting that the STC value strongly depends on the number of lines connected to a node and the number of converter terminals. For the PROMOTioN test benchmark shown in the maximum value for short time current has been set to 40kA.

The Transient Interruption Voltage (TIV) has been set to 1.5pu of the nominal system voltage. The optimum choice of TIV value is a compromise among several criteria, like voltage rating of the DCCB, energy to be dissipated by the surge arrester and insulation coordination of the cables. This analysis is however out of scope of WP4.

The converter breakers need to be designed to perform very quick auto-reclosing sequences. The time duration between the opening and reclosing tripping signal has to be equal to the reclosing time of the primary sequence, which has been set to 50ms. The reclosing delay needs to be long enough to ensure that the faulty line isolation has been performed. The choice of this time is related to the requirement coming from the primary and back-up sequences and has been explained in more detail in [4].

The breaker must be able to withstand reclosing on a permanent fault without damaging the pre-insertion resistor. The line breaker has to be designed for an O-C-O sequence as well. In this case the reclosing sequence is necessary for example after a busbar fault when considering reconfiguration aspects. As example the reclosing time for line breaker could be set to 150ms.

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The opening and reclosing sequence of a CBM is shown in Figure 5-3. The blue lines respect the physical state of the switches with the operation delays considered, whereas the grey lines demonstrate the actual signal sent to the switches.

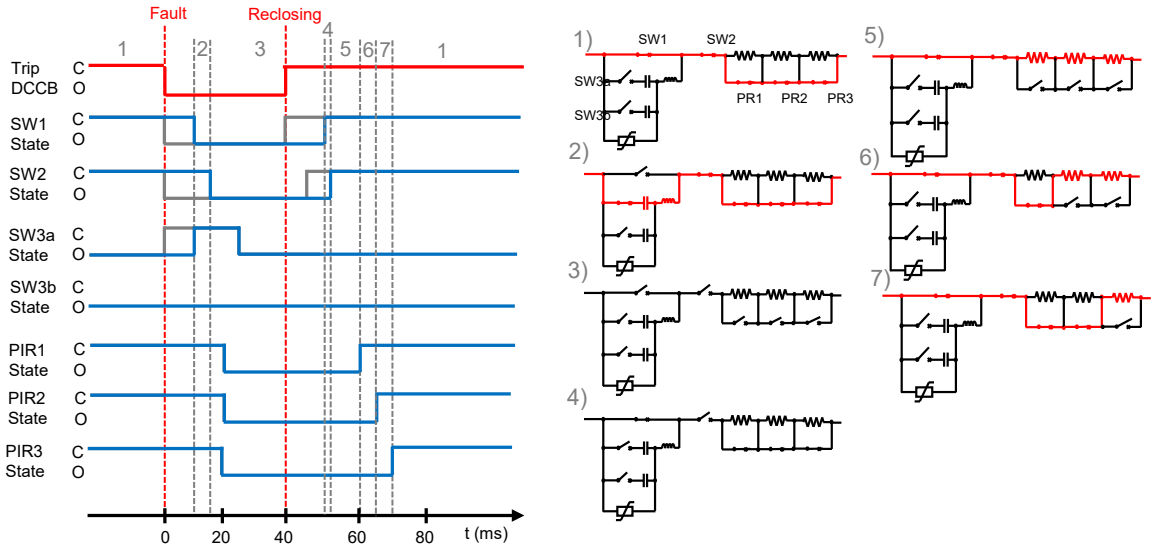

Figure 5-3 Opening and reclosing sequence for a CBM in a non-selective protection strategy (converter breaker)

5.2.2 RESIDUAL CURRENT BREAKER

In a mechanical DCCB the RCB of a breaking module has the aim to extinguish the oscillating current that appears after DC breaker opening and which is due to the oscillation between the system inductance and the circuit breaker capacitance [8]. The RCB has also the aim to physically isolate the breaker from the rest of the grid. A fast operating standard breaking chamber with low DC interruption capability could fit the requirements shown in Figure 5-2. It is worth noting that in this proposed sequence the RCB of CBM and LBM is tripped at the same time as the DCCB, see Figure 5-3. The requirements of the RCB for the CBM are shown in Table 5-2.

Table 5-2 Requirement for RCB of CBM for non-selective protection strategies

	RCB
DC Breaking capability	Few A
AC Breaking capability	Few kA
Short time withstand current	40 kA
Opening time	10 ms
Closing time	10 ms
Open-close operation	O - 50ms - CO

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5.2.3 PRE-INSERTION RESISTOR

The PIR can be designed with several resistances R_1, R_2..R_n with their parallel switches SW_1, SW_2 ..SW_n, as shown in Figure 5-4. It is a variable resistor composed of two or more resistances R_n that can be short-circuited by parallel switches SW_n. The optimized number of resistances is determined in order to ensure a rapid grid voltage restoration and meanwhile limiting the inrush current due to cable charging. The number of resistances to be used and the switching time depend on the total stray capacitance of the grid. The design of the PIR can be considered fixed for a particular benchmark grid. It should be noted that in case of change of topology configuration (e.g. one line out of service) the inrush current would be lower (due to less stray capacitance) and the voltage restoration time would be shorter. For the PROMOTioN benchmark the chosen resistances R_1, R_2 and R_3 are respectively of value 600Ω, 50Ω and 50 Ω while SW_1, SW_2 and SW3 are closed with a delay of 10ms, 15ms and 20ms respectively.

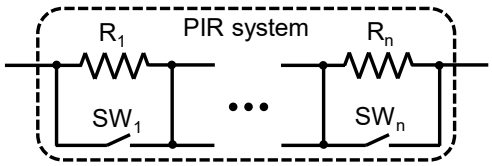

Figure 5-4 Topology of the PIR

It should be noted that line breakers could also need a PIR, in particular during switching-on of a discharged line to avoid inrush currents or transients wave propagation through the grid. The PIR for line breaker does not need to be very fast and could be designed with only one resistance.

5.3 SIMULATION RESULTS

This chapter presents the simulation results using the protection strategy virtual mock-up developed in [4]. More detailed explanation regarding these results can also be found in [4]. The following figures show the voltage and energy constraints across CBMs and LBMs. The fault is applied at line L3 close to Converter1. Three scenarios have been considered:

- Primary sequence, all breakers operate correctly
- Backup sequence when the CBM_1 fails to open
- Backup sequence when LBM_5 fails to open

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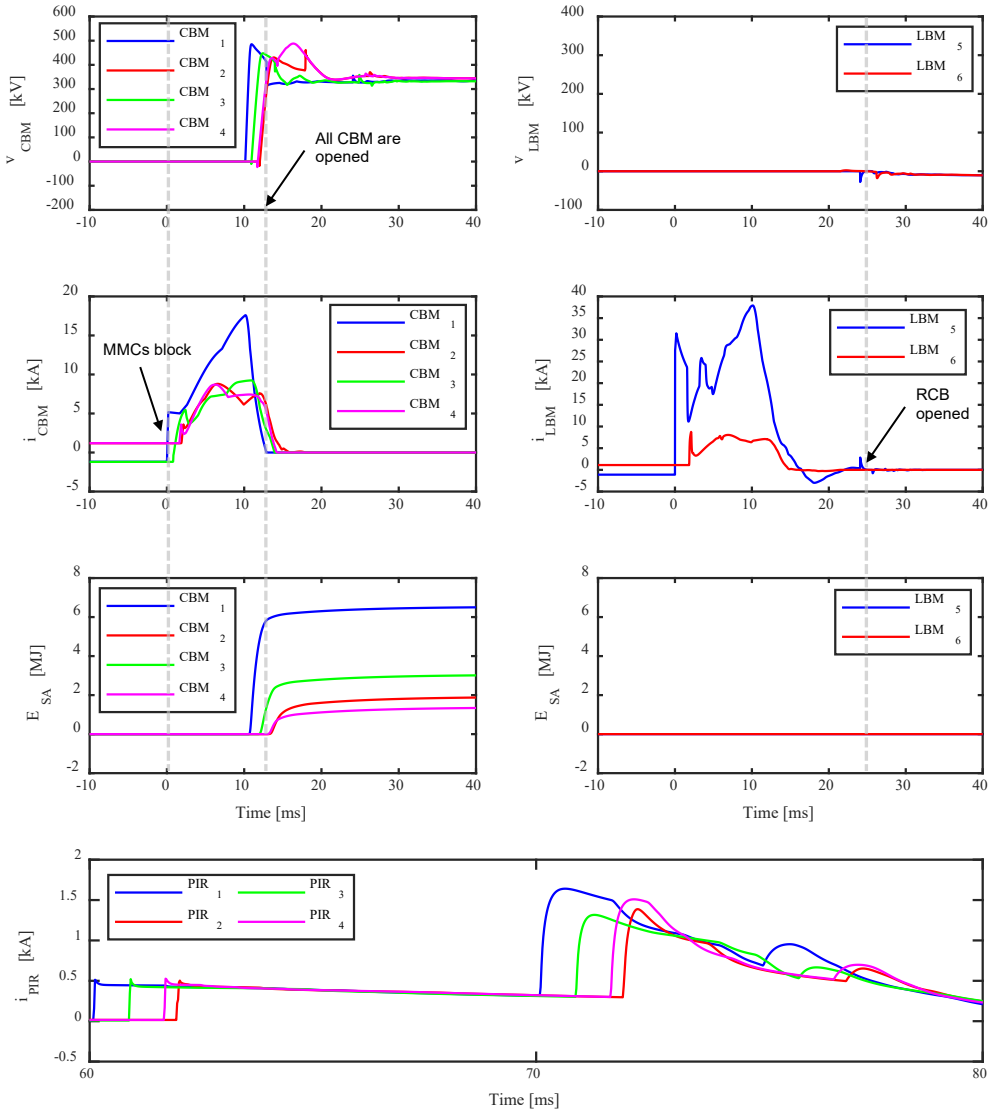

Figure 5-5 Simulation of primary sequence of the non-selective protection strategy using both CBM and LBM, for a fault on L3 close to converter 1 in the PROMOTioN 4-terminal test network.

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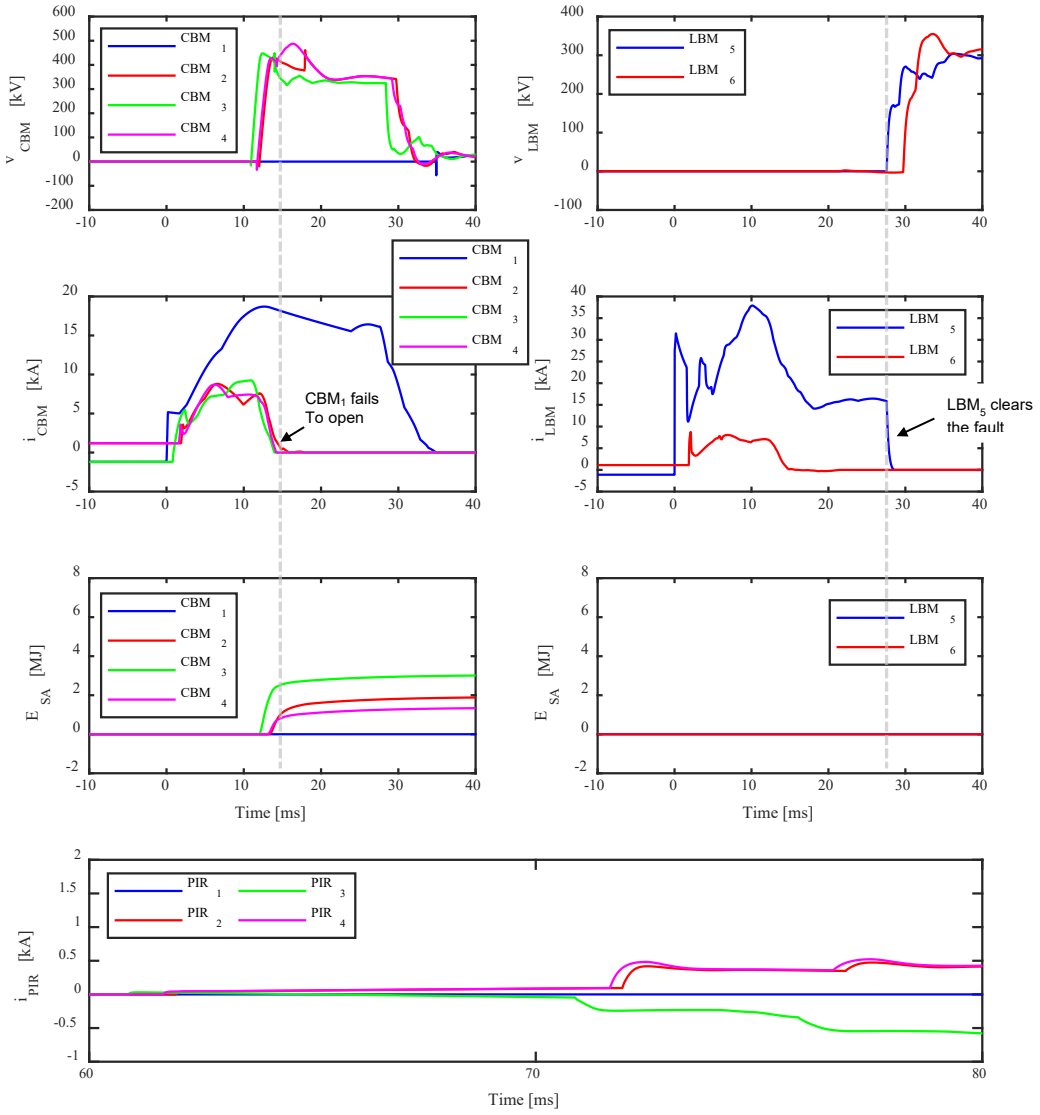

Figure 5-6 Simulation of backup sequence when the CBM1 fails to open, for a fault on L3 close to converter 1 in the PROMOTioN 4-terminal test network.

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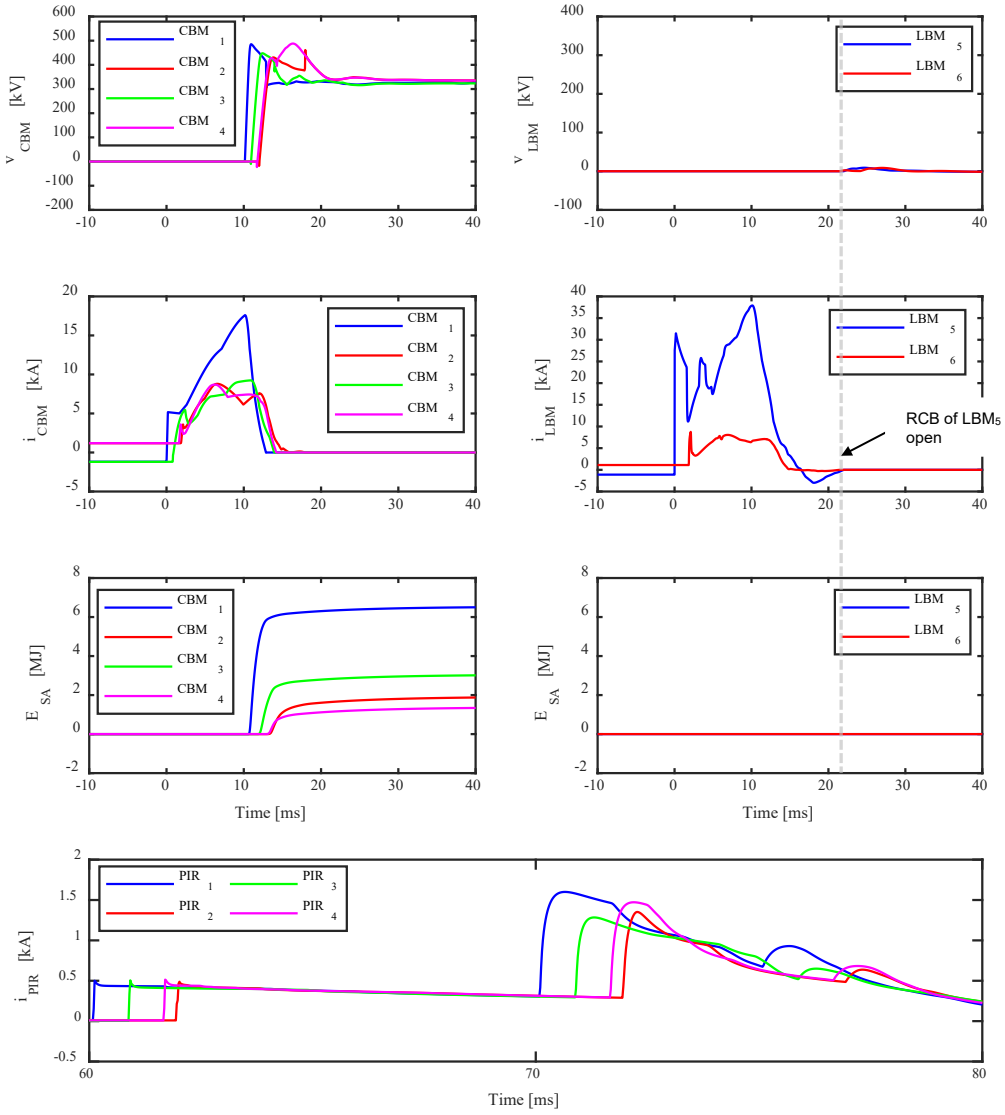

Figure 5-7 Simulation of backup sequence when the LBM5 fails to open, for a fault on L3 close to converter 1 in the PROMOTioN 4-terminal test network.

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6 SUMMARY

This deliverable classifies DCCBs into three types based on their distinctive application scenarios and requirements, and specifies the general requirements of each DCCB type considering constraints and requirements from the HVDC grid and its components. For the Type-I and Type-II DCCBs, a methodology to specify the general requirements, particularly the required series inductor value for the DCCBs is developed. The Type-I and Type-II DCCBs are required to be dimensioned considering the requirements from the converter DC-FRT, selectivity of the fault detection, protection coordination between system- and DCCB-level protection, multivendor interoperability and HVDC grid stability. For Type-III DCCBs, time domain simulations are used to specify their requirements.

The three types of DCCBs identified in this deliverable have different requirements, in terms of operation speed, breaking current capability, inductor size and energy absorption capability. The indicative ranges of these parameters are summarized in Table 6-1 based on studies performed on the PROMOTioN small impact test network. The exact ranges or values for each parameter are considered to be system dependent; therefore, system studies should be performed to specify the exact numbers for a specific HVDC grid, using the methodology/ types of studies presented this deliverable.

- Type-I DCCB: applicable to a fully selective strategy, requiring the DCCB to deal with both pole-to-pole and pole-to-ground faults regardless the transmission line types and HVDC grounding schemes. This type of DCCBs has high requirements on opening speed, breaking current and energy absorption capability, in order both to safely interrupt the associated high currents due to the constraints of the DCCBs and to minimize the impact of the DC fault on the overall HVDC grid.
- Type-II DCCB: applicable to a fully selective strategy, requiring the DCCB to deal with only pole-to-ground faults, limited to cable-based symmetrical monopolar HVDC systems. DCCBs with low speed and low breaking current capability can be used in this application due to the associated low steady-state fault current. Potentially medium/large series inductance is needed similar as the Type-I DCCBs. However, the required energy absorption capability is medium due to the low breaking current.
- Type-III DCCB: applicable to a non-selective protection strategy using both converter and line DCCBs, regardless the fault types, transmission line types and HVDC grounding schemes. The non-selective protection strategy is designed to use slow speed DCCBs with zero series inductance. Therefore, high breaking current and low/medium energy absorption capability is required due to the lack of fault current limiting inductors for this type of DCCB.

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Table 6-1 Summary of parameter ranges.

Application scenarios	DCCB types	Parameter ranges			
		Operation speed ($t_{br,o}$)	Breaking current ($I_{br,pk}$)	Inductor size (L_{line})	Energy absorption capability (E)
Fully selective protection strategy	Type-I	*Dealing with pole-to-pole and pole-to-ground faults*			
		High (≤ 10 ms)	High (> 10 kA)	High • DC-FRTS1: hundreds mH (not practical) • DC-FRTS2: tens mH – hundreds mH (for $t_{br,o}$> 5ms may not be practical due to the required large inductances) • DC-FRTS3: tens mH	High (few MJ to few tens of MJ)
Fully selective strategy (Cable-based symmetrical monopolar HVDC grids)[1]	Type-II	Only dealing with pole-to-ground faults			
		Slow (~ 20 ms)	Low (few kA)	Medium/high • DC-FRTS1: hundreds mH (not practical) • DC-FRTS2: tens mH – hundreds mH (for $t_{br,o}$> 5ms may not be practical due to the required large inductances) • DC-FRTS3: tens mH	Medium (few MJ)
Non-selective protection strategy (Converter + DCCB)	Type-III	Line/Converter DCCB			
		Slow (20 ms)	High (20 kA)	Zero	Low/medium (~ 1MJ/7MJ)

[1] In the scenario only dealing with pole-to-ground faults, the energy absorption is shared between the pole rebalancing equipment and the breaker. Slower breakers thus lead to higher requirements on pole rebalancing, and possibly long DC voltage restoration time.

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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

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8 ANNEX – EXAMPLES OF DCCB REQUIREMENTS IN A FULLY SELECTIVE STRATEGY

This annex presents relevant example results on generic requirements of DCCBs in a fully selective protection strategy. The simulation studies presented in this Annex are performed on the PROMOTioN small impact network. Relevant models and system parameters can be found in D4.2 [3] and D4.3 [4].

8.1 CONVERTER DCFRT REQUIREMENTS METHODOLOGY AND EXAMPLES

In the following sections the details of each FRTS will be examined. In each case, it is assumed that the converter station is only required to block on overcurrent events (and not on undervoltage, a detection method that is often used for converter stations in point-to-point systems). The examples shown below present results for a symmetrical monopolar system for which DCCBs are required to protect against – and therefore line inductors should be sized for – pole-to-pole faults. A similar design would be applicable to protect against pole-to-pole and pole-to-ground faults on bipolar systems.

8.1.1 DC-FRTS1

Method

The fault ride through scenario requires that no converter is blocked following a DC fault, therefore a very fast DCCB and/or a very large inductor is likely to be required such that no MMC arm current reaches the blocking condition. Here, the critical case is typically a fault at the cable end, which results in the highest fault current (excluding the first milliseconds following the fault, during which travelling wave effects can lead to a larger current than that observed from the terminal fault case). An analytical method, developed in [41], is used to determine the required inductor size for a particular fault. The method uses an analytical approximation of the converter fault current in the milliseconds following the arrival of the DC fault travelling wave at the DCCB terminal – based on quantities of the converter (apparent power (S), overcurrent capability (K)) and quantities of the breaker and network (the number of inductors in the fault current path (σ), the breaker operation time (t_{BRK}), the nominal AC and DC voltages (V_{ac} and V_{dc})) – and develops an expression for the minimum required inductance, (3).

$$\begin{cases} L_{dc}^{min} \approx \frac{\eta}{S} \\ where\ \eta = \frac{t_{BRK} V_0}{\frac{\sigma}{V_{ac}}\left[K\left(\frac{1}{\sqrt{3}}+1\right)-1\right]-\frac{\sigma}{V_{dc}}} - \frac{0.1 {v_{ac}}^2}{2\pi f \sigma} \end{cases} \quad (3)$$

Discussion and use case

This fault ride through scenario would likely be used in HVDC systems for which the converters are required to maintain real and reactive power transfer at all times; this could perhaps be due to a very weak AC system for which not even a momentary loss of real and reactive power support is acceptable.

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8.1.2 DC-FRTS2

Method

The fault ride through scenario requires that converter stations remote to the fault (i.e. not adjacent to the faulted line) do not block following the fault. The method for this FRTS is developed in reference [41] and summarised here. The converter stations adjacent to the faulted line may block following the fault. In order to size inductors to meet this condition, the most severe fault condition for a converter not to block is a converter connected to one full cable and two additional inductors between the converter and the critical fault. This condition is used to size the inductors, therefore the behaviour of the transmission line must also be taken into account. In addition to the representation of the converter station (as in DC-FRTS1), the line model must also be included. The assumption for the calculation of the line inductor size is that the network is configured in the worst case for the converter fault current – with only the radial path to the faulted line connected to the converter station bus. This scenario represents a case where the other lines have been taken out of service, and indicates a system design choice – that the network and protection strategy should still remain operable under any switching state.

Discussion and use case

This FRTS results in lower inductor sizes compared to DC-FRTS1, while still ensuring that power can be transferred through healthy areas of the network with minimal interruption. It could provide a good trade-off between continued operation of the remaining network without having very large additional inductances across the network.

8.1.3 DC-FRTS3

Method

Given that the strategy does not impose any blocking restrictions on the MMCs, there is no requirement for additional inductance to restrict blocking. The DCCBs, however, are constrained in the maximum current they can isolate, in a particular time. This time and maximum current varies depending on DCCB technology. In these simulations we assume that the converter stations have IGBTs that are rated to tolerate a DC short circuit fault that is cleared by the AC-side circuit breakers, therefore the inductors are only sized such that they allow successful DCCB operation. In this document the additional inductance for DC-FRTS3 is determined using time domain simulation.

Discussion and use case

This FRTS typically results in the smallest inductor sizes, at the expense of continuous operation of the healthy parts of the system. This provides the minimum cost for additional inductance, particularly useful in a power system for which it is acceptable to any or all of the converter stations to block following the fault.

8.2 SELECTIVITY REQUIREMENTS EXAMPLES

An example of voltages measured at the IED position during F1 and F2 in the PROMOTioN small impact network is shown in Figure 8-3. The voltages are almost overlapping each other during these two faults for a line

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inductance of 1mH. The larger the line inductance, the easier it is to discriminate an internal fault F1 from an external fault F2.

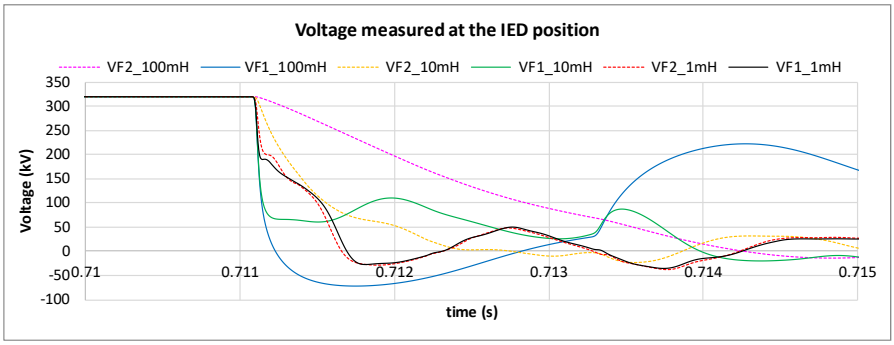

Figure 8-1 Example of voltage waveforms measured at the IED location during fault F_1 and F_2.

Figure 8-4 and Figure 8-5 compare the voltage waveforms during fault at F1 and F3 for a cable length of 200 km and 500 km, respectively. The maximum absolute value of the voltage derivative (dV_{MAX}) and the ratio of the maximum voltage derivatives between the internal and external faults (R_{dV}) are given in Table 8-1. With an inductor of 10 mH, the voltage derivative ratio is 3.8 between the internal fault F1 and external fault F3 for a 200 km cable; however, this ratio is only 0.57 for a 500 km cable. This implies that a 10 mH inductor is not sufficient to discriminate an internal fault from an external fault using voltage derivative criterion.

Table 8-1 Maximum voltage derivative (dV) and margin during internal (F1) and external (F3) faults

Inductor size / Fault location		1 mH	10 mH	100 mH
dV_{MAX} [kV]	F1 (200 km) cable	49,25289	60,85497	62,61475
	F1 (500 km) cable	5,945021	9,050046	9,900448
	F3	120,6368	15,88113	1,643932
$R_{dV}\left(\frac{dV_{MAX}\_F1}{dV_{MAX}\_F3}\right)$	200 km cable	0,408274	3,831904	38,08842
	500 km cable	0,049395	0,571215	6,039174

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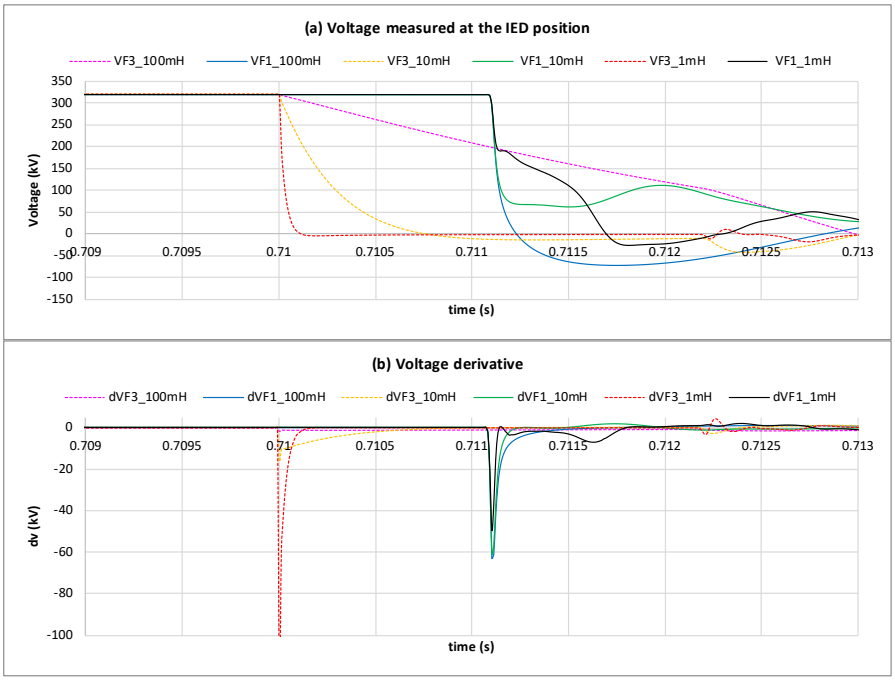

Figure 8-2 Example of voltage waveforms measured at the IED location during fault F_1 and F_3, cable length 200km.

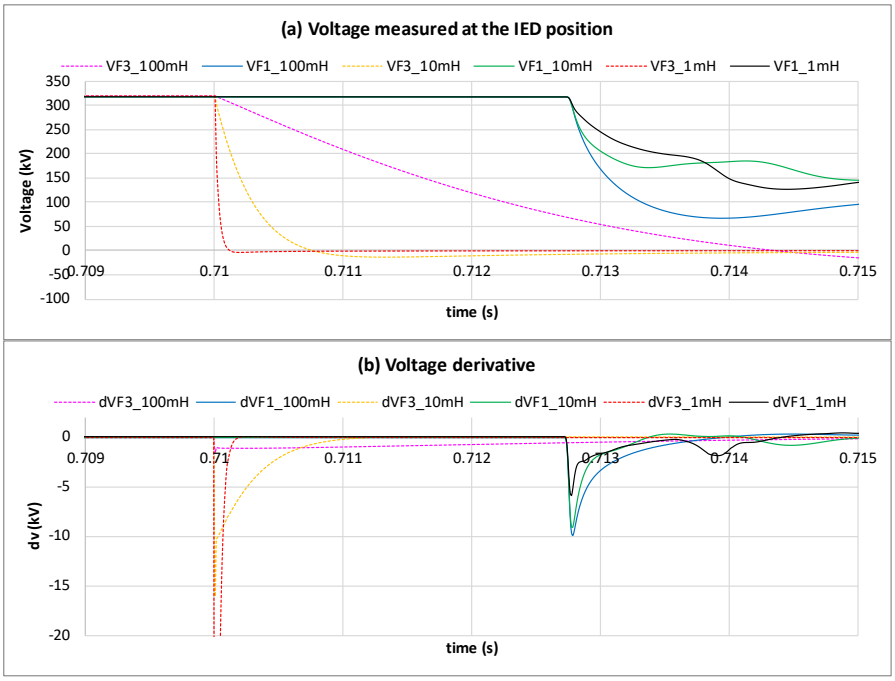

Figure 8-3 Example of voltage waveforms measured at the IED location during fault F_1 and F_3, cable length 500km.

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8.3 MULTIVENDOR INTEROPERABILITY REQUIREMENTS EXAMPLES

First, the influence of the main DCCB parameters is analysed using the PROMOTioN small impact network (Figure 4-1). Hybrid and mechanical DCCB technologies are considered when investigating the impact of using mixed DCCB technologies in a single HVDC grid. Then the requirements with regard to multivendor interoperability of mixed DCCB technologies are summarized.

The breaker opening time ($t_{br,o}$), peak breaking current ($I_{br,pk}$) and inductor size (L_{line}) are the most influential parameters on the HVDC system, in terms of HVDC grid stability and fault clearing.

- The breaker opening time is primarily limited by the speed of the actuators of the UFD or the vacuum interrupter, respectively for a hybrid or mechanical DCCB. Based on the state-of-the-art DCCB technology, the breaker opening time is in the range of 1.2 – 3 ms for hybrid DCCBs, and 5 – 10 ms for mechanical DCCBs [1].
- The main constraints for the breaking current capability are the interrupting capability of the semiconductors and the vacuum interrupters. In addition, it is possible to increase the breaking current capability by paralleling IGBTs or vacuum interrupters without improving the performance of these components. An example is the hybrid DCCBs used in the Zhangbei project, which uses two parallel IGBGTs to achieve a breaking current capability to 25 kA [17].
- The inductor size, on the other hand, is a design choice, which is primarily influenced by the converter fault-ride-through requirement, the breaker opening time and the breaking current capability.

Two scenarios are considered when studying the impact of mixed DCCB technologies, as the three parameters, breaker opening time, breaking current capability and inductor size are closely coupled with one another. In the first scenario, the impact of the breaker opening time is investigated with a fixed inductor size for both hybrid and mechanical DCCBs. In the second scenario, both the breaker opening time and the inductor size are varied for hybrid and mechanical DCCBs. The inductor sizes are chosen to comply with a pre-determined breaking current capability.

The impact of multivendor scheme on the DCCBs and three key performance indicators (fault clearing time, DC voltage restoration time, and active power restoration time) is evaluated using the PROMOTioN small impact test network, shown in Figure 4-1. Similar as in D4.3 [4], the restoration time is defined as recovery within ±15% tolerance band of the nominal DC voltage, and ±10% tolerance band of the post-fault steady-state value for the DC voltage and active power, respectively. As examples, pole-to-pole faults are applied in the network for demonstration.

8.3.1 BREAKER OPENING TIME

In this scenario, all line inductors are chosen as 50 mH regardless the DCCB technology. The aim is to analyse the impact on DCCB requirements of using mixed DCCB technologies in a HVDC grid, so the inductors are not dimensioned to limit the breaking current within certain values. The breaker opening time is 2 ms and 8 ms for

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ultra-fast and fast DCCBs, respectively. This condition entails that the required breaking current capability of a fast DCCB is likely to be higher than that of an ultra-fast DCCB, given the same fault and network conditions. Three cases with different combinations of breaker opening times (Table 8-2) are compared by applying six pole-to-pole faults along cable L_3 with a 70 km interval (Figure 4-1).

Table 8-2 Simulation cases and results: impact of breaker opening time.

Case				**a**	**b**	**c**
Simulation conditions	$DCCB_5$	$t_{br,o}$	[ms]	2	8	2
	$DCCB_6$	$t_{br,o}$	[ms]	2	8	8
Simulation results	$DCCB_5$	i_{int}	[kA]	8.5	19.5	8.5
		E_{SA}	[MJ]	4.8	17.9	4.8
	$DCCB_6$	i_{int}	[kA]	7.6	16.4	**16.5**
		E_{SA}	[MJ]	4.5	17.5	**20.4**
	MMC current	I_{MMC}	[kA]	4.2	8.9	8.9
	fault clearing time	t_{cl}	[ms]	12.7	17.2	32.2
	DC voltage restoration time	$t_{U_{DC}}$	[ms]	33.2	66.7	55.6
	Active power restoration time	$t_{P_{AC}}$	[ms]	135.4	273.1	272.1

Each case is simulated with six fault locations. The results are worst cases of the six fault locations.

Simulation waveforms of breaker current, breaker energy, MMC current, DC busbar 1 voltages and active power of MMC_2 at fault location 210 km away from DC busbar 1 are given as examples in Figure 8-6. Peak breaking current (i_{int}) and maximum energy (E_{SA}) of DCCBs, maximum current of all four MMCs (I_{MMC}) and the three key performance indicators ($t_{cl}, t_{U_{DC}}$ and $t_{P_{AC}}$) of all six fault locations are summarized in Table 8-2.

Compared with the mixed DCCB case-c, the maximum current and energy experienced by the ultra-fast $DCCB_5$ are effectively the same in case-a with two ultra-fast DCCBs. This implies that the requirements of an ultra-fast DCCB are not impacted by the DCCB technology of the remote line end (Figure 8-6 (a), (c) and Figure 8-7 (a) - (b)). However, the maximum current and energy experienced by the fast $DCCB_6$ increase in the mixed DCCB case-c as comparing to the case-b with two fast DCCBs (Figure 8-6 (b), (d) and Figure 8-7 (a) - (b)). The reason is that in the ultra-fast DCCB case-a, fault currents from MMC1 and MMC3 are mainly contributed to $DCCB_5$, and fault currents from MMC2 and MMC4 are mainly contributed to $DCCB_6$. However, in the mixed DCCB case-c, once the ultra-fast $DCCB_5$ has opened, fault currents from all branches contribute to the fast $DCCB_6$. This essentially means that when dimensioning a fast DCCB, the breaker opening time of the DCCB at the remote line end has to be taken into account.

The fault current contributions from the MMCs are the highest if both DCCBs are of fast type (Figure 8-7 (e) and (c)). The case-a with two ultra-fast DCCBs have the shortest fault clearing time, DC voltage restoration time and active power restoration time (Figure 8-7 (d) - (f)). Using mixed DCCB technologies have similar performance in terms of the three key performance indicators as the case-b with two fast DCCBs as summarized in Table 8-2.

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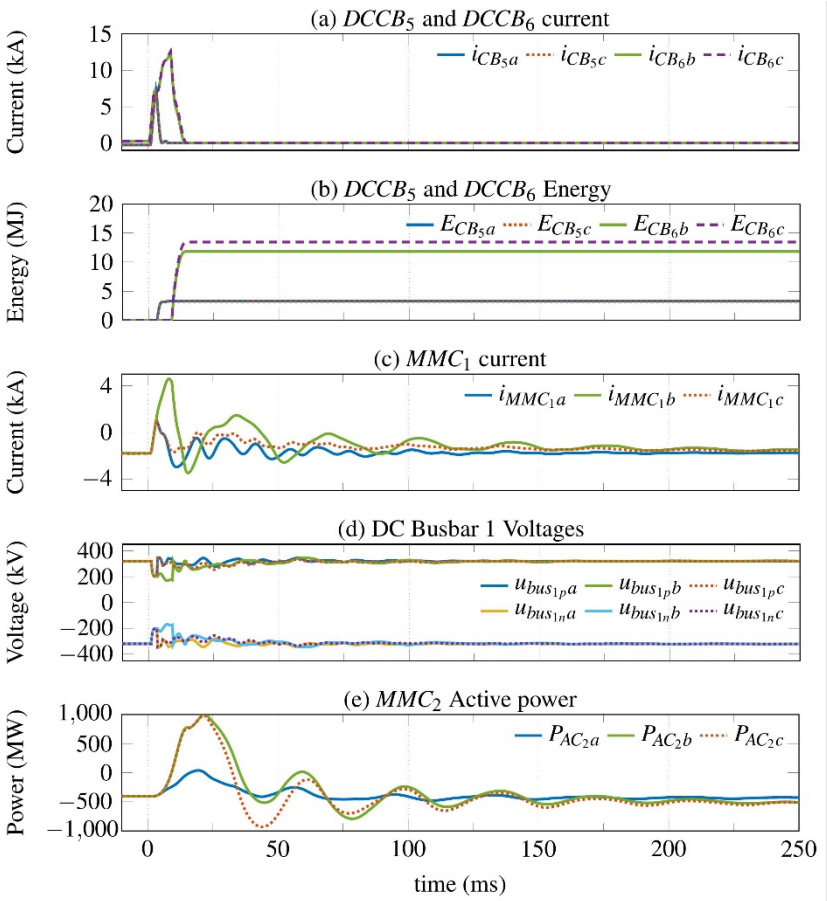

Figure 8-4 Impact of using mixed DCCB technologies (breaker opening time). Subscript a: two ultra-fast DCCBs, subscript b: two fast DCCBs, and subscript c: mixed ultra-fast and fast DCCBs, fault location: 210 km away from DC busbar 1.

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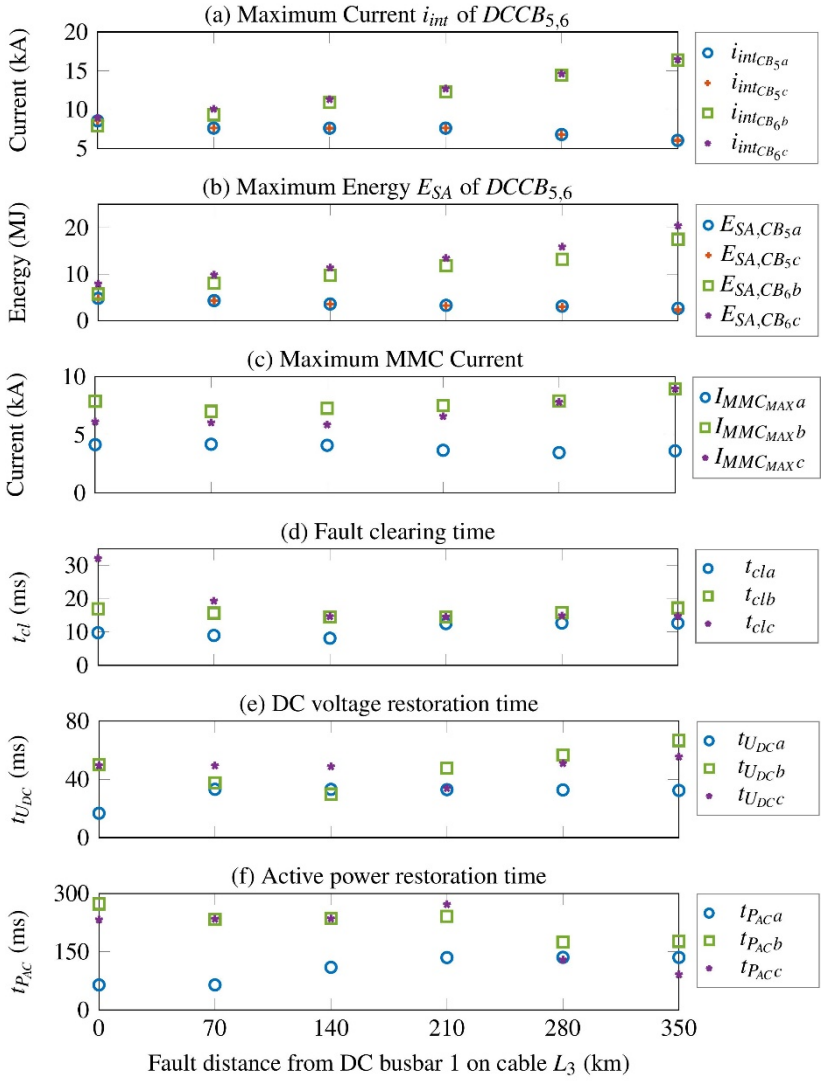

Figure 8-5 Impact of using mixed DCCB technologies (breaker opening time). Subscript a: two ultra-fast DCCBs, subscript b: two fast DCCBs, and subscript c: mixed ultra-fast and fast DCCBs.

8.3.2 SERIES INDUCTOR SIZE

In this scenario, the required breaking current capabilities of both ultra-fast and fast DCCBs are assumed to be 16 kA. The inductor size is selected considering the worst fault condition such that the fault current level falls within the assumed breaking current capability of each DCCB type. As a result, an inductor size of 50 mH is chosen for an ultra-fast DCCB with breaker opening time of 2 ms, and 100 mH is chosen for a fast DCCB with breaker opening time of 8 ms. For the sake of simplicity, the same inductor size is chosen for all DCCBs in the reference cases, namely, all inductors are 50 mH in case-a with ultra-fast DCCBs, and 100 mH in case-c with fast DCCBs. In case-c and case-d, the $DCCB_6$ is replaced with a fast or ultra-fast type compared with the reference case-a and case-c, respectively. Simulation cases and conditions are summarized in Table 8-3.

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Table 8-3 Simulation cases and results: impact of inductor size.

Case				Faults	a	b	c	d
Simulation conditions	DCCB$_5$	$t_{br,o}$	[ms]	f_1 to f_{24} as indicated in Figure 4-1	2	2	8	8
		L_{line}	[mH]		50	50	100	100
	DCCB$_6$	$t_{br,o}$	[ms]		2	8	8	2
		L_{line}	[mH]		50	100	100	50
	Other DCCBs	$t_{br,o}$	[ms]		2	2	8	8
		L_{line}	[mH]		50	50	100	100
Simulation results	DCCB$_5$	i_{int}	[kA]	f_1 to f_6 on cable L$_3$	8.5	8.5	13.3	13.3
		E_{SA}	[MJ]		4.8	4.8	18	**19.0**
	DCCB$_6$	i_{int}	[kA]		7.6	14.1	11.9	6.3
		E_{SA}	[MJ]		4.5	20.4	17.5	3.8
	MMC current	I_{MMC}	[kA]		4.2	**7.6**	7.0	**5.1**
	fault clearing time	t_{cl}	[ms]		12.7	**19.4**	19.1	**18.7**
	DC voltage restoration time	$t_{U_{DC}}$	[ms]		33.2	**49.9**	81.1	**63.5**
	Active power restoration time	$t_{P_{AC}}$	[ms]		135.9	**415.7**	400.7	**255.5**
	MMC current	I_{MMC}	[kA]	f_7 to f_{12} on cable L$_1$	9.5	9.5	10	10
	fault clearing time	t_{cl}	[ms]		6.4	6.4	14.8	14.8
	DC voltage restoration time	$t_{U_{DC}}$	[ms]		5.3	3.6	67	66.7
	Active power restoration time	$t_{P_{AC}}$	[ms]		219.5	**184.4**	393.9	396.5
	MMC current	I_{MMC}	[kA]	f_{13} to f_{18} on cable L$_2$	5.8	5.8	8.3	8.3
	fault clearing time	t_{cl}	[ms]		12.7	**14**	18.8	18.8
	DC voltage restoration time	$t_{U_{DC}}$	[ms]		33.5	**46.8**	83.2	**63.6**

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	Active power restoration time	$t_{P_{AC}}$	[ms]		73.7	74.1	307.9	308.4
	MMC current	I_{MMC}	[kA]	f_{19} to f_{24} on cable L_4	5.7	5.7	8.6	8.6
	fault clearing time	t_{cl}	[ms]		6.0	6.1	15.7	15.6
	DC voltage restoration time	$t_{U_{DC}}$	[ms]		7.2	7.8	84.9	83.8
	Active power restoration time	$t_{P_{AC}}$	[ms]		136.9	**143.3**	468.8	466.2

The results are worst cases of the six fault locations along a cable.

Similarly, simulation waveforms at fault 210 km away from DC busbar 1 on cable L_3 are given as examples in Figure 8-8 and Figure 8-9. Figure 8-10 compares the impact on the DCCBs, MMCs and the three key performance indicators of six faults along cable L_3. The impact of using both different $t_{br,o}$ and L_{line} on DCCB dimensioning is similar to the first scenario with only different breaker opening times. Comparing case-a and case-b, the impact on the ultra-fast $DCCB_5$ is negligible when the $DCCB_6$ at the remote line end is replaced with a fast DCCB (Figure 8-8 (a) - (b) and Figure 8-10 (a) - (b)). On the contrary, comparing case-c and case-d, the requirements of breaking current and energy of the fast DCCB slightly increases, when the fast DCCB at the remote line end is replaced with an ultra-fast one (Figure 8-9 (a) - (b) and Figure 8-10 (a) - (b)). The performance, in terms of MMC currents and the three key performance indicators, worsens when an ultra-fast DCCB is replaced with a fast DCCB in a HVDC grid using all ultra-fast DCCBs (Figure 8-10). In particular, the maximum active power restoration time of the six fault locations on cable L_3 increases from 135.9 ms in case-a to 415.7 ms in case-b (Table 8-3). On the contrary, the performance improves when a fast DCCB is replaced with an ultra-fast DCCB in a HVDC grid using all fast DCCBs (Figure 8-10). For instance, the maximum active power restoration time of the six fault locations on cable L_3 reduces from 400.7 ms in case-c to 255.5 ms in case-d (Table 8-3).

The impact of changing one DCCB on the overall HVDC grid performance is evaluated by performing faults on the rest cables in the system. Maximum MMC currents and the three key performance indicators of faults on cable L_1 are given as an example in Figure 8-11. Results of the maximum values on all cables are summarized in Table 8-3. Changing one inductor size on cable L_3 has insignificant impact on the maximum MMC currents and fault clearing time during faults on the rest cables in the system. However, DC Voltage and active power restoration time during faults on the rest cables of the system are influenced due to changing the inductor of $DCCB_6$ on cable L_3. An example of MMC_2 active power during a fault at 0 km from DC busbar 1 on cable L_1 is shown in Figure 8-12, where the active power restoration time is reduced from 219.5 ms in the case-a with all ultra-fast DCCBs to 184.4 ms in the case-b with $DCCB_6$ replaced with a fast DCCB.

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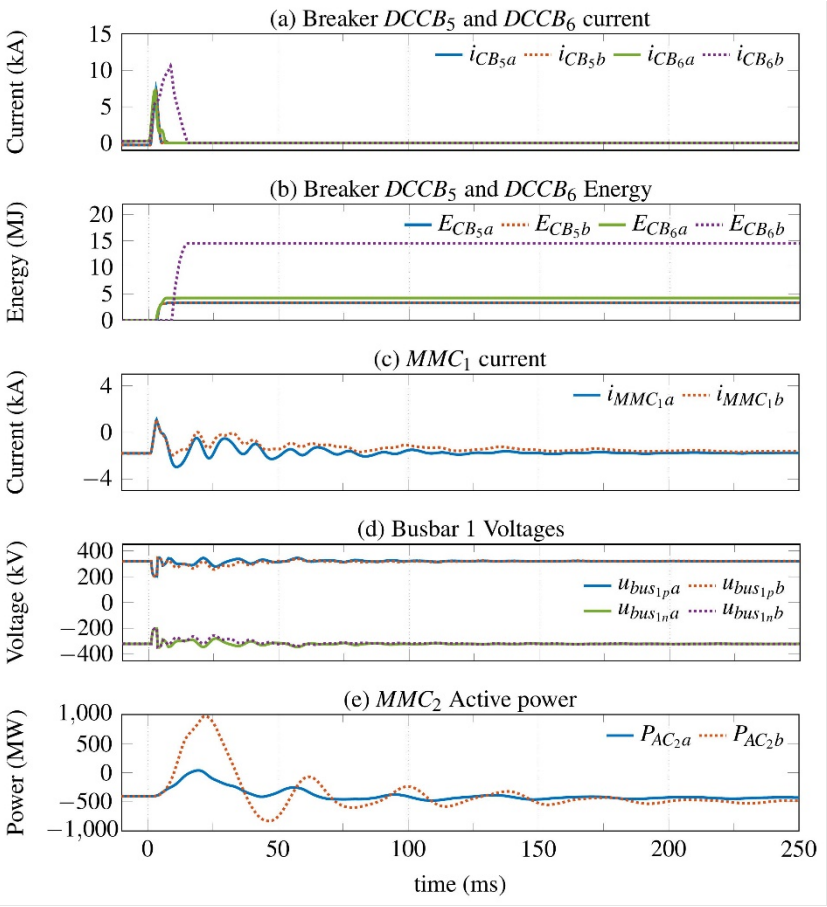

Figure 8-6 Impact of using mixed DCCB technologies (inductor size). Subscript a: all ultra-fast DCCBs, and subscript b: all ultra-fast DCCBs except for $DCCB_6$ with a fast one, fault location: 210 km away from DC busbar 1 on cable L_3.

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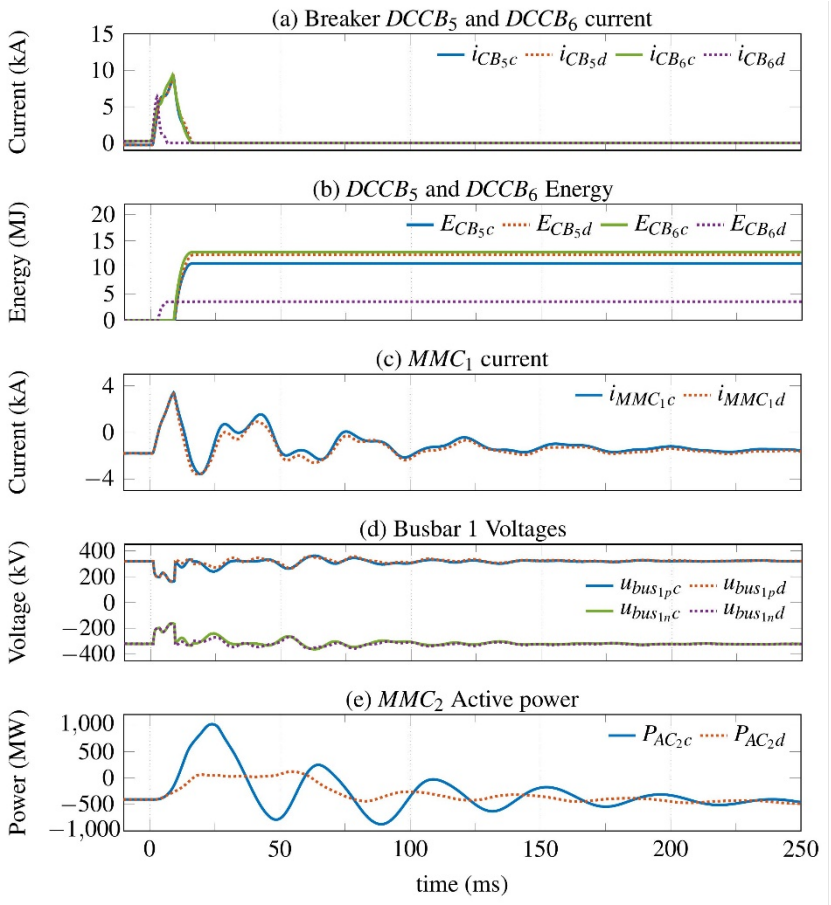

Figure 8-7 Impact of using mixed DCCB technologies (inductor size). Subscript c: all fast DCCBs, and subscript d: all fast DCCBs except for $DCCB_6$ with an ultra-fast one, fault location: 210 km away from DC busbar 1 on cable L_3.

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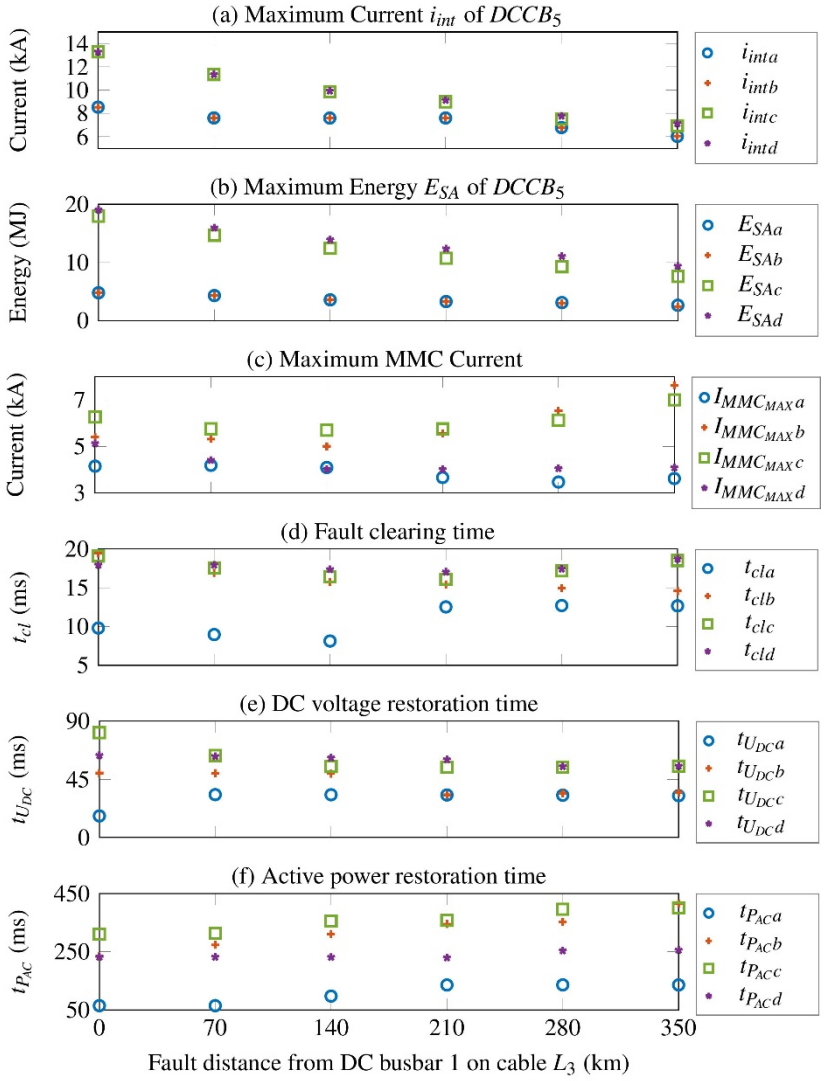

Figure 8-8 Impact of using mixed DCCB technologies (inductor size), pole-to-pole faults along cable L_3.

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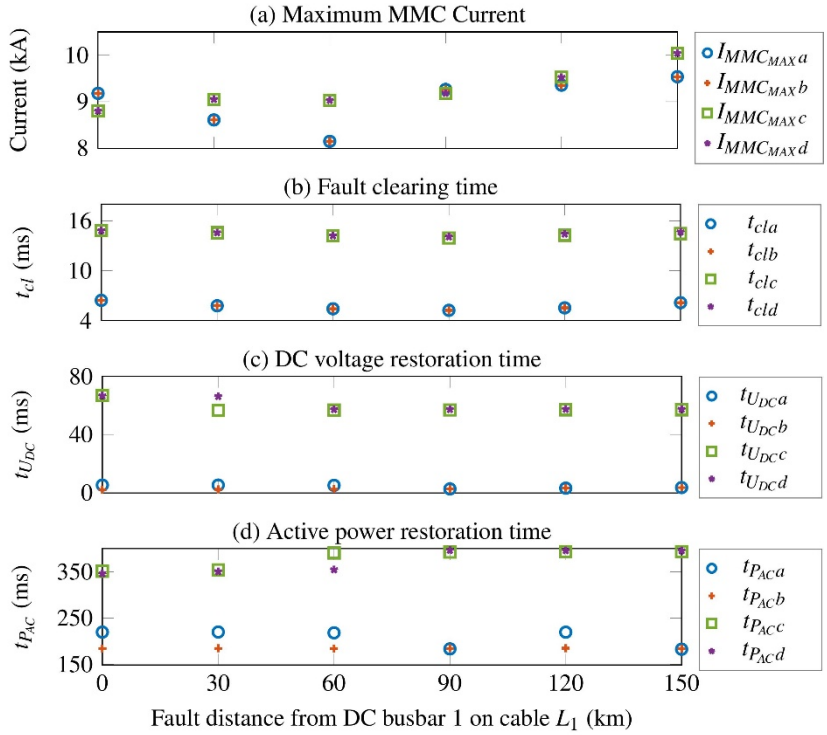

Figure 8-9 Impact of using mixed DCCB technologies (inductor size), pole-to-pole faults along cable L_1.

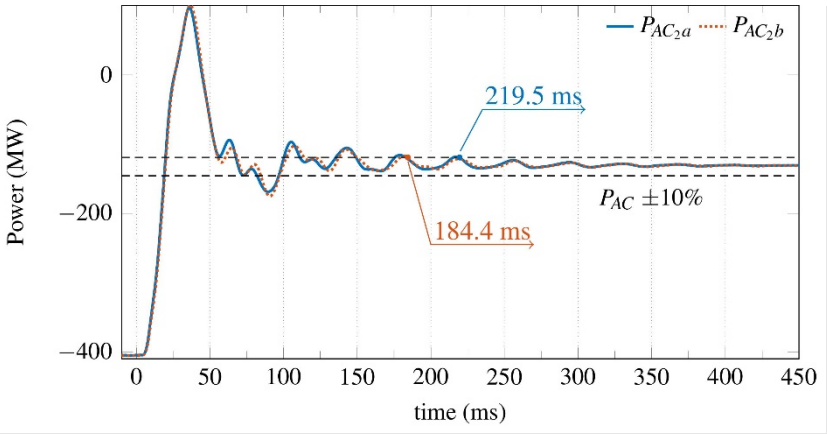

Figure 8-10 Impact of using mixed DCCB technologies (inductor size): active power of MMC_2. Subscript a: all ulta-fast DCCBs, and subscript b: all ultra-fast DCCBs except for $DCCB_6$ with a fast one, fault location: 0 km away from DC busbar 1 on cable L_1.

8.3.3 SUMMARY

The simulation results demonstrate that it is possible to use mixed DCCB technologies in a single HVDC grid, although the performance of the HVDC grid and requirements on the components vary depending how the HVDC grid is designed. Replacing a fast DCCB with an ultra-fast one in a HVDC grid using fast DCCBs can generally improve the performance of the HVDC grid during DC faults. However, the breaking current and energy requirement of the fast DCCB at the remote end may be increased due to the replacement. On the contrary, the performance of the HVDC grid in terms of fault clearing, DC voltage restoration and active power restoration speed, during DC faults tends to worsen if an ultra-fast DCCB is replaced with a fast one in a HVDC using ultra-

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fast DCCBs. Although the requirements on the ultra-fast DCCB at the remote end are not likely to be significantly influenced due to the replacement. Therefore, at the design stage, it is important to dimension the DCCBs with the knowledge of the main parameters of the whole grid, and reasonable ranges of parameters ($t_{br,o}$ and L_{line}) of the grid should be specified particularly if future replacements are planned. Furthermore, the series inductor of a DCCB is considered a system parameter as the overall system dynamic is likely to be influenced by the inductor size. Relevant system studies should be carried out to ensure that no violation of component and system constraints is made due to the change of the DCCB and its series inductor size.

8.4 PROTECTION COORDINATION REQUIREMENTS OF HYBRID DCCBS

8.4.1 MAIN COMPONENTS AND FUNCTIONS OF HYBRID DCCBS

The main circuit of the hybrid DCCB discussed in this section is shown in Figure 8-13. The dimension of the DCCB is considered for a 320 kV/2 kA HVDC system, using 4.5kV/3kA BIGT modules for the LCS and MB valves [18].

- LCS: the safe operation area (SOA) of the LCS is considered similar to those in the VSC applications, with $i_{LCS} \leq 2I_{LCS,n} = 2 \times 3 \times I_C$, using a 3x3 matrix configuration.
- MB: Series connected BIGTs are used to build up the voltage withstandability in the MB. For example, the total number of BIGTs is $N_{BIGT} = 4cells \times 4stacks \times 10\ BIGT\ module = 160$ modules for current interruption in one direction for a 320 kV DCCB [49]. As saturation region of the BIGT is used for current interruption, the peak interrupting current in the MB is defined by $i_{int} \leq I_{br,pk}$, rather than the typical SOA used in VSC applications.
- Surge arresters (SA) in the MB: the SAs are dimensioned to absorb the required energy considering the worst-case scenario, such as repeated O-C-O on an overhead line section and breaker failure backup operation in a cable-based system.

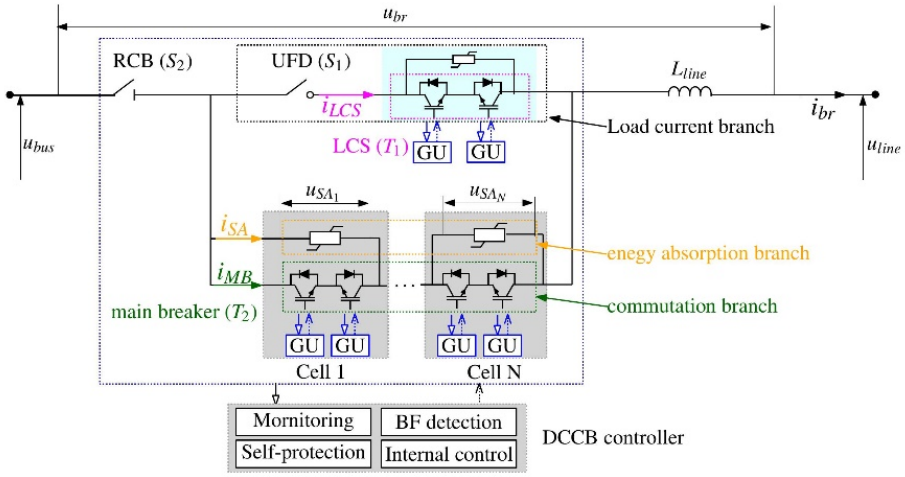

Figure 8-11 Main circuit of a hybrid DCCB.

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The hybrid DCCB is controlled and monitored by a dedicated DCCB controller, which consists of internal control (open/close the DCCB upon an IED command), breaker failure internal detection (BF detection), self-protection and monitoring functions (Figure 8-13).

Self-protection (trip without an IED command): the self-protection function will issue a trip order to the DCCB upon detecting an overcurrent in the LCS, when the line protection IEDs fail to detect a fault or issue a trip order.

$$TP_{sp} = 1, if\ TP_{IED} = 0\ \&\ i_{LCS} > I_{sp} \quad (4)$$

Where I_{sp} is the overcurrent threshold, and is the overcurrent threshold; and TP_{sp} and TP_{IED} are the trip orders from the self-protection function and the IED(s), respectively.

The self-protection overcurrent threshold should be selected considering the breaking current capability and coordination with line protection IEDs and the adjacent DCCBs as described in equation (5).

$$\begin{cases} I_{sp,i} \le I_{spH,i} = K_{OC} I_{br,pk} - t_{br,o}\tau_{eq,i} \\ I_{sp,i} > I_{spL,i} = \max\limits_{1 \le j \le N_{brch}-1} I_{spL,ij} \\ I_{spL,ij} = \tau_{ij}\left(\dfrac{I_{spH,j} - I_{DC,n}}{\tau_{eq,j}} + t_{br,o}\right) + I_{DC,n} \\ I_{sp,i} > \tau_{eq,i} t_{IED,p} + I_{DC,n} \end{cases} \quad (5)$$

where $I_{spH,i}$and $I_{spL,i}$ are the high and low threshold limits of branch i; $I_{spL,ij}$ is the low limit of branch i during faults on branch j ; $\tau_{eq,i}$ is the approximate rate-of-rise (ROR) of the fault current for a fault on branch i ; τ_{ij} is the approximate ROR of the current contribution from branch i to the adjacent branch j during a fault on branch j; K_{OC} is the overcurrent coefficient; $I_{DC,n}$ is the rated DC current; and $t_{IED,p}$ is the operating time of the primary protection IED(s).

To coordinate with the adjacent DCCBs, I_{sp} should be set for each line DCCB individually considering two limits, (1) the high limit I_{spH}: the DCCB is still able to interrupt the fault current considering a breaker opening time $t_{br,o}$ given the worst internal fault; and (2) the low limit I_{spL}: the threshold should be high enough so that the DCCB is not tripped on self-protection due to external faults on the adjacent lines.

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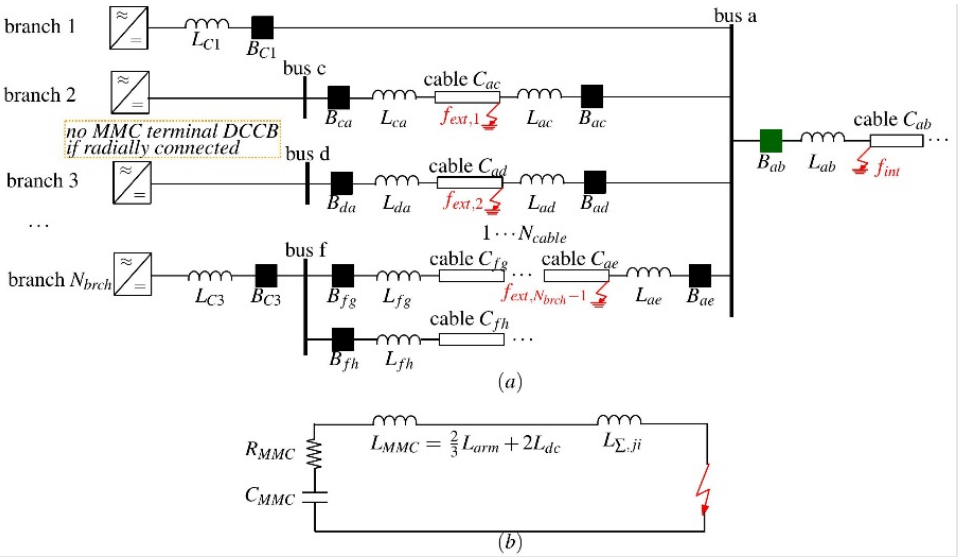

Figure 8-12 Fault current contributions from multiple adjacent branches for DCCB B_{ab}, (a) example circuit, and (b) equivalent circuit for estimating current contribution from an adjacent branch.

These two limits can be calculated per DC bus, considering terminal faults on each line connected to the DC bus. An example is given to estimate $I_{spH,i}$ for DCCB B_{ab} and $I_{spL,ji}$ for the adjacent DCCBs shown in Figure 8-14 (a). An adjacent branch can be directly connected to or via one to multiple cables to a modular multilevel converter (MMC). The equivalent circuit for estimating current contribution from an adjacent branch j during a pole-to-pole fault at the terminal of cable C_{ab} can be simplified as shown in Figure 8-14 (b), neglecting the impedances of the cables. The MMC is represented by its equivalent RLC model. The total series line inductance $L_{\Sigma,\mathrm{ji}} = (2N_{cable} + 1 + \sigma) \times 2L_{line}$, assuming the same line inductor sizes throughout the network, and N_{cable} series-connected cables in the adjacent branch. For a radially connected converter (Figure 8-14 (a) branch 2), as it is not necessary to install DCCBs at the converter, $\sigma = 0$, or else $\sigma = 1$. The ROR of the fault current contribution from branch j is approximately $\tau_{ji} = \frac{K_{OV}U_{DC,n}}{L_{ji}}$, $L_{ji} = L_{MMC} + L_{\Sigma,\mathrm{ij}}$, where K_{OV} is the overvoltage coefficient and $U_{DC,n}$ is the rated DC voltage. Thus, the ROR of the total fault current $\tau_{eq,i} = \sum_{j=1}^{N_{brch}} \tau_{ji}$, with N_{brch} adjacent branches. The low threshold limit $I_{spL,ji}$ of the adjacent branch j during a fault on branch i, is $\tau_{ji}\left(\frac{I_{spH,i}-I_{DC,n}}{\tau_{eq,i}} + t_{br,o}\right) + I_{DC,n}$.

Driver-level protection: is usually implemented at the gate driver units (GUs) to protect an individual switch from overvoltage and overcurrent, without receiving a tripping command from the upper level DCCB controller. The error message from the GU is sent to the upper level DCCB controller for further analysis and action. The activation of driver-level protection will disable the DCCB and may lead to destruction of protective surge arresters [35].

The protection settings of BIGT modules in the LCS are thus set within the maximum allowed current and voltage. However, the BIGT modules in the MB can be set much higher, considering an operating and design margin K_{MB} from the rated breaking current. For instance, the maximum breaking current of 19~kA has been successfully tested for a rated breaking current of 16 kA [18].

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$$\begin{cases} i_{LCS,BIGT} < I_{LCS,dp} = 2I_C \\ i_{MB,BIGT} < I_{MB,dp} = K_{MB} I_{br,pk} \end{cases} \quad (6)$$

8.4.2 PROTECTION COORDINATION

In a fully selective protection philosophy, each line is protected by DCCBs at both ends with their associated IEDs. Typically, two fully redundant protective relaying systems are required for high or extra-high voltage AC transmission lines to ensure high dependability. Similar degree of redundancy is likely to be required for HVDC grid protection, using different protection schemes to achieve the desired reliability and speed. An example scheme of HVDC grid protection is given in Figure 8-15, adopting a dual redundant protection scheme. The protection functions of each main IED include primary fault detection, local backup protection in case of breaker failure, and coordination with the associated DCCB and adjacent IEDs.

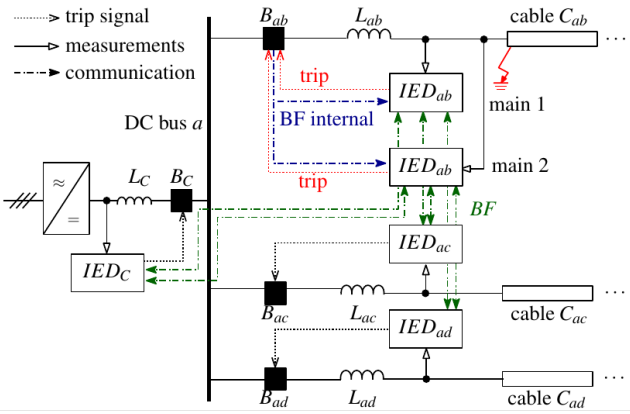

Figure 8-13 An example of HVDC grid protection with details indicated for breaker B_{ab}.

For primary protection of a DC fault, the trip signal can be issued by the main IEDs or by self-protection function of the breaker in case both the main IEDs fail. A breaker failure can be detected at the DCCB by the internal detection function or at the main IEDs by local backup protection. Then the breaker failure signal is sent to the adjacent IEDs to trip the backup DCCBs.

The principle to coordinate the different levels of protections is to allow the system-level protection to activate before triggering DCCB-level protections, as illustrated in Figure 8-16. The IEDs of the faulty line should detect a fault and send a trip order prior to the fault current in the associated DCCB reaches to its self-protection level. This defines the maximum time available for the primary protection IEDs to send a trip signal, $t_{IED} = \frac{(I_{sp,i} - I_{DC,n})}{\tau_{eq,i}}$. As the self-protection thresholds can be set between I_{spH} and I_{spL}, the lower the self-protection threshold, the less time is available for the primary IEDs to operate.

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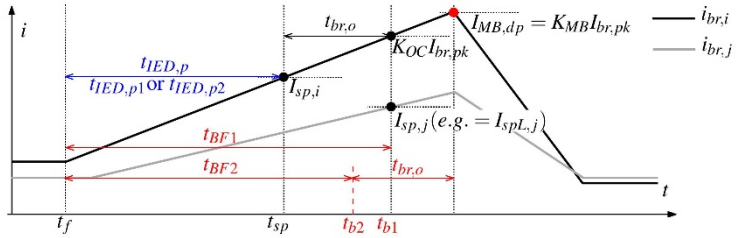

Figure 8-14 Protection coordination between IEDs and DCCB-level protection.

In case of a breaker failure, the backup protection IEDs should send a trip signal to the backup DCCBs before they are tripped by their internal self-protections (noted as t_{BF1} in Figure 8-16), and the backup DCCBs should open before triggering the driver-level protection of the failed breaker (noted as t_{BF2} in Figure 8-16). The total available time for the breaker failure backup protection can be calculated by (7).

$$\begin{cases} t_{BF} = \min(t_{BF1}, t_{BF2}) \\ t_{BF1} = \dfrac{\left(I_{sp,j} - I_{DC,n}\right)}{\tau_{ji}} \\ t_{BF2} = \dfrac{\left(I_{MB,dp} - I_{DC,n}\right)}{\tau_{eq,i}} - t_{br,o} \end{cases} \quad (7)$$

In a scenario where self-protection and driver-level protection of the DCCB are not required, the inductance of the DCCB can be dimensioned to fulfil (1) the converter DCFRT requirements and (2) the IED and breaker operation time requirements, described by equation (8).

$$\begin{cases} i_{MMC} < I_{diode,MAX}\ (DCFRTS3) \\ \tau_{eq,i}\left(t_{IED,p} + t_{br,o}\right) + I_{DC,n} \leq I_{br,pk} \end{cases} \quad (8)$$

However, in a scenario where self-protection and driver-level protection of the DCCB are considered, the inductance of the DCCB needs to be dimensioned to allow for coordination between DCCB-level and system-level protection:

$$\begin{cases} \tau_{eq,i}\left(t_{IED,p} + t_{br,o} + t_{mgn,sp}\right) + I_{DC,n} \leq I_{br,pk} \\ \tau_{eq,i}\left(t_{BF2} + t_{br,o} + t_{mgn,dp}\right) + I_{DC,n} \leq I_{MB,dp} \end{cases} \quad (9)$$

where $t_{mgn,sp}$ and $t_{mgn,dp}$ are the margins for self-protection and driver-level protection. Essentially, a larger inductor is needed compared to the scenario without DCCB-level protection functions.

8.4.3 EXAMPLE CASE

An example of the total available operating times for the primary and backup IEDs is given in Figure 8-17, for the IED associated with the breaker DCCB5 in the PROMOTioN small impact test network shown in Figure 4-1. A high and low settings, I_{spH} and I_{spL}, are considered for the self-protection thresholds, with K_{OC}:0.5 ~ 0.95 and K_{OV}: 1 ~ 1.05.

The high limit of the self-protection threshold I_{spH} first increases as the line inductance increases, and then approaches to its limit, $K_{OC}I_{br,pk}$ (Figure 8-17 (a)). The low limit of the self-protection threshold I_{spL} is

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predominantly determined by the ROR ratio between the different branches, and less influenced by the line inductance.

The available time for the IED operations are calculated considering both high and low limits of the self-protection settings (Figure 8-17 (b)). For instance, to allow for $t_{IED,p}$ = 1 ms, the minimum required line inductance is approximately 30 mH and 50 mH for $I_{sp,i} = I_{spH,i}$ and $I_{sp,i} = I_{spL,i}$, respectively. In this particular example, the backup IED operation time is determined by the driver-level protection setting of the failed DCCB rather than the self-protection settings of the backup DCCBs. To allow for $t_{BF} = t_{IED,p} + t_{br,o} + 1\ ms$, the minimum required line inductance is approximately 65 mH, considering a breaker opening time of 2 ms.

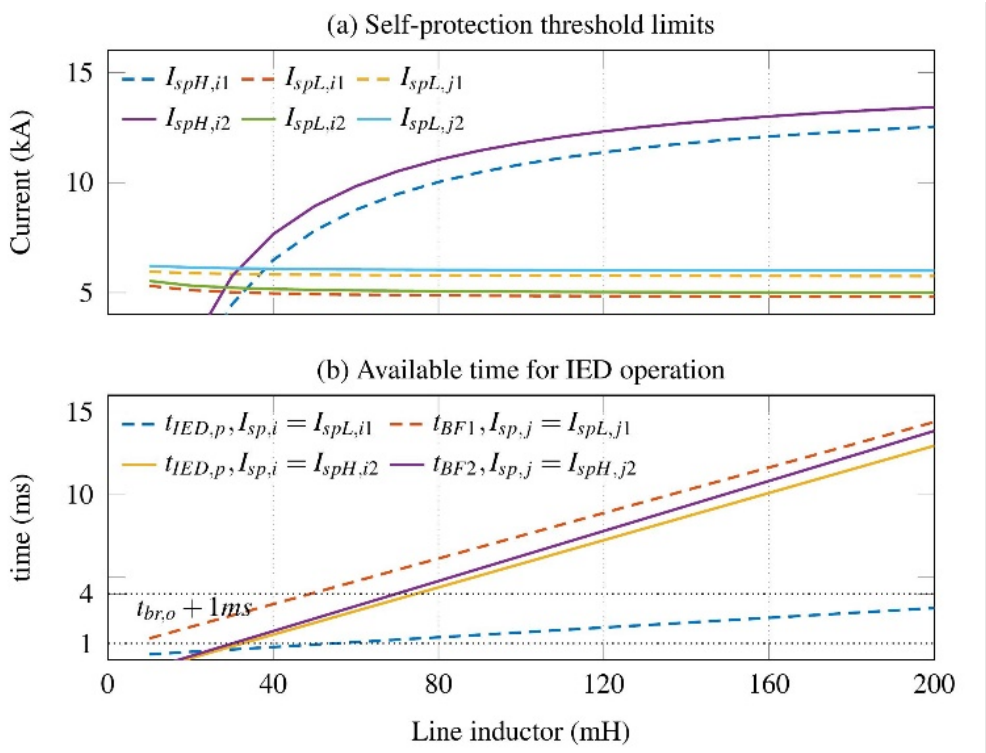

Figure 8-15 Example of self-protection limits and total available operating times of IEDs, assuming three parallel branches. Dashed line (subscript 1): K_{OC} = 0.95, K_{OV} = 1, solid line (subscript 2): K_{OC} = 0.9, K_{OV} = 1.05.

For the same example with three parallel branches, the required inductance in the scenario without DCCB-level protection functions is about 30 mH, considering $t_{IED,p} = 1\ ms$ and $t_{br,o} = 2\ ms$. This inductance is significantly smaller than 65 mH in the scenario with DCCB-level protection functions.

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9 ANNEX – PROTECTION MATRICES FOR DC FAULT RIDE THROUGH SCENARIOS

As an extension to the Continuous Operation (CO), Temporary Stop (TS) and Permanent Stop (PS) concepts, the fault ride through scenarios have been introduced in Section 4.2.1. In order to align the fault ride through scenarios with the protection matrix method of protection system definition, protection matrices are defined here such that the fault ride through concepts can be defined in a standardised manner.

Table 9-1: Protection matrix indicating minimally required states for DC fault ride through scenario 1 on the small impact network (Figure 2-1).

Protection zone		C1	C2	C3	C4
1	F_{L1}	CO	CO	PS	CO
2	F_{L2}	CO	CO	CO	CO
3	F_{L3}	CO	CO	CO	CO
4	F_{L4}	CO	CO	CO	CO

Table 9-2: Protection matrix indicating minimally required states for DC fault ride through scenario 2 on the small impact network (Figure 2-1).

Protection zone		C1	C2	C3	C4
1	F_{L1}	TS	CO	PS	CO
2	F_{L2}	TS	CO	CO	TS
3	F_{L3}	TS	TS	CO	CO
4	F_{L4}	CO	TS	CO	TS

Table 9-3: Protection matrix indicating minimally required states for DC fault ride through scenario 3 on the small impact network (Figure 2-1).

Protection zone		C1	C2	C3	C4
1	F_{L1}	TS	TS	PS	TS
2	F_{L2}	TS	TS	TS	TS
3	F_{L3}	TS	TS	TS	TS
4	F_{L4}	TS	TS	TS	TS

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