PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

D5.1 HVDC Network Fault Analysis

PROMOTioN – Progress on Meshed HVDC Offshore Transmission Networks
Mail info@promotion-offshore.net
Web www.promotion-offshore.net

This result is part of a project that has received funding form the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

CONTACT

DOCUMENT INFO SHEET

Document Name:	HVDC Network Fault Analysis
Responsible partner:	DNV GL
Work Package:	WP 5
Work Package leader:	Cornelis Plet
Task:	5.1
Task lead:	Nadew Belda

DISTRIBUTION LIST

APPROVALS

	Name	Company
Validated by:	Yash Audichya	SHE Transmission
	Dragan Jovcic	University of Aberdeen
Task leader:	Nadew Belda	DNV GL
WP Leader:	Cornelis Plet	DNV GL

DOCUMENT HISTORY

Version	Date	Main modification	Author
1.0	01-09-2016	DNV GL	Nadew Belda, Cornelis Plet, Claudia Spallarosa, Kazuyori Tahata
2.0	03-10-2016	DNV GL	Nadew Belda, Cornelis Plet

WP Number	WP Title	Person months	Start month	End month
5	Test Environment for HVDC Circuit Breakers	49	1	24

Deliverable Number	Deliverable Title	Type	Dissemination level	Due Date
5.1	HVDC Network Fault Analysis	Report	Public	M9

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

LIST OF CONTRIBUTORS

Work Package and deliverable involve a large number of partners and contributors. The names of the partners, who contributed to the present deliverable, are presented in the following table.

PARTNER	NAME
DNV GL	Nadew Belda
DNV GL	Cornelis Plet
MEU	Claudia Spallarossa
MELCO	Tahata Kazuyori

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

Content

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

EXECUTIVE SUMMARY

Several manufacturers have proposed and developed HVDC circuit breaker technologies and built prototypes. The behaviour of these prototypes has been verified internally through a range of development tests in the manufacturer's own labs. Testing of HVDC circuit breakers is fundamentally different from that of AC circuit breakers as both voltage across and current through the circuit breaker exist at the same time, leading to an energy absorption requirement. One of the goals of PROMOTioN is to demonstrate the performances of the proposed HVDC circuit breaker technologies with full power testing at an independent short-circuit laboratory.

Meaningful demonstration of HVDC circuit breaker technology is achieved when the applied tests accurately reflect realistic fault conditions in multi-terminal HVDC networks. The goal of Work Package 5 is to, based on fault analysis of multi-terminal HVDC networks, develop suitable test requirements and a test programme, as well as to realize a test circuit based on AC short-circuit generators.

Identifying the factors determining the fault currents in meshed multi-terminal HVDC networks is the goal of task 1. Existing technical literature on HVDC network fault behaviour and analytical fault analysis techniques were reviewed and simulation studies on a benchmark study network were carried out. Fault analysis has been carried out by means of PSCAD simulations on a multi-terminal HVDC benchmark study network fed by half bridge modular multi-level voltage source converters to study the various fault current contributions and their characteristics. The effects of network topology, series reactors, fault location, converter blocking logic, AC network strength and line type on the rate of rise and the magnitude of the fault current have been analysed qualitatively. Based on the results the following concluding remarks can be made:

C1 A fault is characterised by a breakdown of the insulation system, which results in a voltage transient which travels along the cable away from the fault location and invokes, first, the discharge of any charged capacitances resulting in a current limited only by any series impedance in the cable. These discharges result in the first transients that last only for few milliseconds. Then, the AC sources start feeding the short circuit current limited by AC side impedance and DC side resistance.

C2 At impedance boundaries, a part of the negative voltage wave is transmitted and the rest is reflected. At HB MMC VSC terminals, the voltage transient triggers the discharge of the submodule capacitors leading to a (near linear) rise in current limited only by the converter arm reactor.

C3 In order to protect internal circuitry, an HB MMC VSC converter blocks based on a logic combination combining arm and output overcurrent and DC under-voltage thresholds, turning the converter essentially into an uncontrolled diode rectifier. Prior to blocking, the increasing DC output current of the converter has no impact on the AC current, so all energy is supplied by the submodule capacitors.

C4 Due to the different arrival times of the voltage transient at various points in the network, converters at different distances block at different times.

C5 After blocking, the DC output current of the converter is determined by the DC resistance between the fault, the converter resistance, the converter transformer impedance and the AC network strength.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

C6 The insertion of series reactors at the ends of cables reduces/limits the rate of rise of fault currents. The higher the inductance of the reactor, the slower the rate of rise of current.

C7 Due to the insertion of series reactors, the time until converter blocking is increased and the converters are enabled to regulate their terminal voltage. The higher the inductance of the reactor, the smaller the voltage drop at the converter terminal before it blocks.

C8 As long as a converter can regulate its output voltage (in the presence of series reactors), the discharge of adjacent feeders is very limited.

C9 The moment a converter blocks, the terminal voltage collapses inducing discharge of adjacent cables

C10 Rate of rise of current in adjacent cables is suppressed because of multiple series reactors in the fault current path.

C11 The rate of rise of fault current through a HVDC circuit breaker increases with increasing numbers of adjacent cables (or converter stations) being connected to its bus.

C12 The phenomenon of reflecting waves causes periodic voltage swings at the cable ends of both positive and negative polarity.

C13 Depending on the length of the cable and the location of the fault, the reflection of a positive voltage transient may increase the average voltage at the cable end and reduce the rate of rise of fault current.

C14 Due to the reactive nature of overhead lines, their presence in a DC network has a similar effect to that of a series reactor and decreases the rate of rise of fault current.

It is noted that these qualitative descriptions may be used to predict the worst case fault condition in a given HVDC network. The worst case conditions are always network specific and must under all circumstances be less severe than the maximum ratings of a HVDC circuit breaker. From the analysis it follows that the value of the series reactor may be adjusted in order to change the stresses or demands placed on converter stations and/or prospective HVDC circuit breakers.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

ABBREVIATIONS

ABBREVIATION	EXPLANATION
AAC	Alternating Arm Converter
AC	Alternating Current
CB	Circuit Breaker
DCCB	Direct Current Circuit Breaker
DCL	DC Current Limiting Reactor
EMI	Electro-Magnetic Interference
FB	Full Bridge
HB	Half Bridge
HVAC	High voltage AC
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line Commutated Converter
MMC	Modular Multi-Level Converter
MTDC	Multi-Terminal HVDC
NLC	Nearest Level Control
OHL	Overhead Line
PCC	Point of Common Coupling
PWM	Pulse Width Modulation
SHE	Selective Harmonic Elimination
VSC	Voltage Sourced Converter
WP	Work Package

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

1 INTRODUCTION

As part of the Energy Union initiative, the European Union has set out ambitious goals to source 20% of all consumed electrical energy from renewable power sources and provide at least 10% interconnection capacity between member states by 2020. A substantial share of this renewable energy target can be realized as offshore wind energy in the North and Baltic seas. The generated energy will be transmitted back to shore using submarine cables. Likewise, a substantial share of interconnectors is envisaged to be realized as submarine cables. Due to the capacitive nature of cables, HVAC is not suitable for the transmission of large amounts of power across long distances. HVDC technology, however, imposes no limit on the length of the cable and is thus considered as the technology of choice to connect distant windfarms or achieve high power interconnection.

Especially given the long repair times for submarine cables, the increasing reliance on offshore wind generators and interconnectors requires higher reliability of HVDC systems. In AC systems, reliability is typically improved by providing redundancy so that, in case of an outage, one or more parallel paths can be used to guarantee continuity of supply. A protection system based on the characteristics of the AC generators in power plants and the AC impedance of networks, identifies the presence and location of the failure and sends a command to the nearest AC circuit breakers, which subsequently remove the smallest possible faulty section of the network.

To date, no such parallel paths, or meshed networks, have been realized in HVDC systems partly due to the absence of a proven protection strategy and DC circuit breaker technology. As a result, when a fault occurs in an HVDC system, it can only be removed from the network by allowing the system voltage to collapse and using HVDC switchgear to reconfigure the system, leading to an interruption in the supply of power.

Several manufacturers have proposed and developed HVDC circuit breaker technologies and built prototypes. The behaviour of these prototypes has been verified internally through a range of development tests in the manufacturer's own labs. Testing of HVDC circuit breakers is fundamentally different from that of AC circuit breakers as both voltage across and current through the circuit breaker exist at the same time, leading to an energy absorption requirement. One of the goals of PROMOTioN is to demonstrate the performance of the proposed HVDC circuit breaker technologies with full power testing at an independent short-circuit laboratory.

Meaningful demonstration of HVDC circuit breaker technology is achieved when the applied tests accurately reflect realistic fault conditions in multi-terminal HVDC networks. The goal of Work Package 5 is to, based on fault analysis of multi-terminal HVDC networks, develop suitable test requirements and a test programme, as well as to realize a test circuit based on AC short-circuit generators.

Identifying the factors determining the fault currents in meshed multi-terminal HVDC networks is the goal of task 5.1. Existing analytical fault analysis techniques were reviewed and simulation studies on a benchmark study

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

network were carried out. The various fault current contributions and the impact of the AC network, the converter stations and fault characteristics were studied for a range of different types of fault situations.

1.1 MOTIVATION

To date no HVDC circuit breakers have been applied in real HVDC systems. Due to an absence of practical experience with such devices, discussions about their implementation mostly remain an academic affair, and are not part of network strategists' vocabulary. As a result, the state-of-development, abilities and limitations of HVDC circuit breakers and the impact of their operation on an HVDC network, both adverse and beneficially, are not well understood by their prospective end-users. This uncertainty, along with economic considerations, impedes the uptake of HVDC circuit breakers and thus, in part, prevents the realisation of meshed multi-terminal networks.

By independently and publicly demonstrating the performance and operation of the proposed HVDC circuit breaker technologies through full-power testing, risk associated with the viability of the technologies is effectively reduced. The results of such tests can be used to independently validate academic studies and thus serve as a starting point for the dialogue between manufacturers and end-users to formulate requirements for this type of device.

Test requirements can be determined in two ways; they can be based on the ratings provided by the manufacturer or, they can be based on the worst case fault conditions that occur in the HVDC system in which the circuit breaker is placed (provided that its ratings are sufficient). The latter will serve to instil the required confidence in the devices' readiness to deal with realistic stresses.

1.2 DOCUMENT OVERVIEW

The remainder of this document is organized as follows. In Chapter 2, a compact overview of HVDC technologies is provided. Brief introduction of distinguishing features of various converter technologies including the pros and cons associated with each converter technology is presented. In addition, several converter configurations and topologies are illustrated in this chapter. Chapter 3 provides a review of the technical literature on HVDC fault studies and proposes a benchmark study network which will be used as a test case in the ensuing simulation work. The results of the simulations are presented in chapter 4 along with a descriptive explanation of the characteristics of the presented curves. The outcomes of the analysis of the simulation results are discussed in chapter 5 to draw some more generic conclusions, which are presented in chapter 6. Finally, further details regarding the adopted modelling approach can be found in the appendix.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

2 HVDC TRANSMISSION

Introduction of HVDC into existing, large, heavily loaded AC systems can relieve some of the issues that AC networks suffer from: congestion management, system stability issues and black-out risks due to cascading effects, for example [1], [2]. Break-even distances, where HVDC becomes favourable, for point-to-point connections are typically in the range of 500-600 km for overhead line and 50-100 km cables (submarine or subterranean) [3].

Locating wind farms further from shore is appealing as wind speed tends to be higher on average, as well as more stable. However, long AC cables require reactive compensation, which is difficult to locate in a submarine environment, making connection from the wind farm to shore challenging, therefore HVDC link appear as a viable solution. HVDC allows connection of asynchronous AC networks, over long subsea cables, with precise control of power flow, fitting these requirements of an interconnected system. Therefore, it received an increased interest for offshore wind application and a number of point-to-point connections have now been constructed and are in operation, connecting large offshore wind resources in the North Sea to the European mainland. Expansion into a multi-terminal network is seen as a way to smooth power output, improve reliability, share capacity and interconnect various national networks.

Nevertheless, HVDC faces technical challenges which must be addressed: DC breakers are required for larger networks, which are likely to be more expensive than AC counter-parts; converter control is typically complex; AC-DC converters results in energy loss, have a high capital cost and may introduce additional harmonics to the system [4].

2.1 CONVERTER TECHNOLOGIES

HVDC transmission can be grouped by converter type: LCC (line-commutated converters) and VSC (voltage source converters). The type of converter technology has a significant impact on the capabilities and performance of the system.

LCC is a mature technology, with more than 60 years of operational experience. Its low losses and high capacity make it appropriate for long distance, bulk power transmission.

VSC is a newer, more flexible technology. A number of VSC converter topologies have been developed and are in operation, each with its own advantages. Maximum power ratings are typically lower than for LCC and losses higher (although efficiency has significantly improved with the introduction of the modular multi-level converter). The capability to connect to passive loads/weak networks combined with being readily used in a multi-terminal network make it especially applicable to offshore wind applications.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

Although PROMOTioN is concerned with the study of MTDC networks built from VSC technology, for completeness, in the following sections a brief overview of the operating principles and merits and applications of both LCC and several VSC topologies are discussed.

2.1.1 LINE COMMUTATED CONVERTER (LCC)

Line Commutated Converters (LCC) are a mature HVDC technology that has been exploited for more than 60 years in projects worldwide. The basic form of the converter is the six-pulse Graetz-bridge, shown in Figure 1. In the earliest systems, each of the arms (numbers T1-T6 in Figure 1) consisted of a mercury-arc valve. Modern installations utilize thyristors in their place, with many connected in series to attain the required blocking capability.

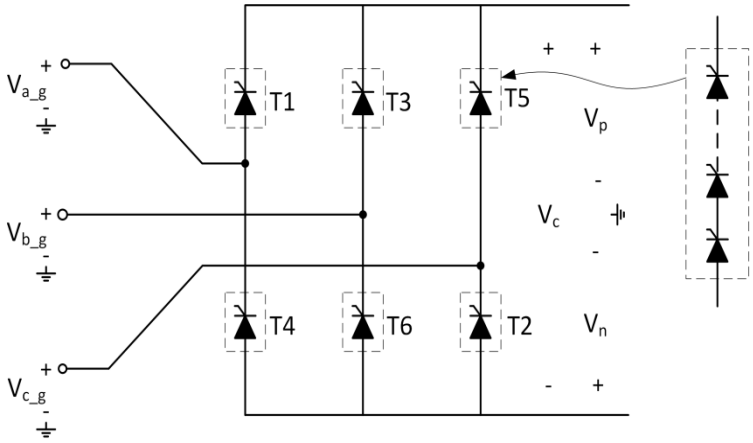

Figure 1: Basic LCC converter topology of three-phase, six-pulse Graetz-bridge used in line-commutated converters. A number of each thyristors are connected in series to form a valve

A thyristor is a three-terminal, semi-controllable semi-conductor device: it can be turned-on through control, but cannot be turned off. A short current injection into the third terminal 'latches' the device into a conducting state, termed 'firing' or 'triggering' the thyristor. Current must be forced through zero by the external circuit before the device transitions back to a blocking state.

LCC offers very high power throughput, with the largest systems in the range of 6 GW and up to 10 GW in planning (in comparison, VSC technology is currently limited to approximately 1GW). The development of high capacity thyristor devices has assisted in decreasing losses to approximately 0.7% per converter station [5], making LCC very desirable for long distance, bulk power transmission applications. Current through the converter is unidirectional and changes in power flow direction require voltage polarity to be reversed. In point-to-point systems, this can be achieved by adjustment of the firing angle of each converter, although the rate of change of voltage must be limited to ensure cables are not overstressed [6], [7]. It is more common that a converter's connection to the DC side is reconfigured by switchgear in multi-terminal networks. This significantly restricts the ability of the network to change power flows rapidly. The converter requires a strong AC network to force current to commutate from one valve to the next. As such, it is unable to interface with weak or passive AC systems like offshore wind farms, for example. Table 1 lists the advantages and disadvantages in the use of LCC.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

Table 1: pros and cons of LCC HVDC technology

Pros	Cons
• Very high capacity • Robust against DC faults • Simple control structure (when compared to VSC) • Thyristors have significant short-term overload capability (when compared to IGBTs)	• Large filters – increasing footprint (unrealistic for offshore platform) • Constant reactive compensation required • Poor AC fault performance • Difficulty operating in multi-terminal network

2.1.2 VOLTAGE SOURCE CONVERTER (VSC)

The VSC technology was developed in the 1980's thanks to the advent of Insulated Gate Bipolar Transistors (IGBTs) to the electrical conversion domain. It is now well established for medium and large power ratings and used in a wide range of applications. VSC is based on IGBT switches, which allow the independent control of both active and reactive power injections at the terminal buses.

Voltage Source Converters (VSC) are able to manipulate the output voltage freely: in magnitude, phase and frequency. As such, they have independent control of both real and reactive power flow between the converter and the AC network. This also allows them to interface with weak networks or passive loads – vital for offshore wind applications. Table 2 summarizes the advantages and disadvantages in the use of VSC [8], [9].

Table 2: Pros and cons of VSC HVDC technology

Pros	Cons
• Independent control of active and reactive power, as the power reversal is executed by reversing the DC current • Small/no filter as AC current has low harmonics content due to high switching frequency. • Black start capability, indicated for offshore wind farm applications • Applicable to multi-terminal DC network and weak network • Smaller footprint	• the appearance of unwanted Electro-Magnetic Interferences (EMI) [8]; • low power rating limited due to the voltage and current rating of the IGBT technology • Poor DC fault performance (two-level and half bridge) • Complex control structure

In 1999 the first industrial application which used VSC was the connection of Gotland island using two 70 km long cables operated at ± 80 kV to transmit 50 MW. The use of VSC technology was motivated by the weakness of the

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

islanded AC network, which was principally powered by local wind turbines [10]. Since then an increasing number of VSC-based projects have emerged [11], mainly considering submarine cables and offshore wind farms.

VSC topologies can be split into two-level and multi-level categories. The first generation of VSC converters was of two-level type. Although its functionality improved on that of line-commutated converters, they were restricted in capacity to around 400 MW and losses were considerably higher at approximately 2-3% per converter. A number of VSC topologies have been developed since the inception of the first commercial VSC system in the late 1990s. These have reduced conversion losses and brought additional capabilities. Multi-level converters have improved on these two key areas, as well as providing additional benefits, and have come to dominate the market for new installations. A brief background of these converters is given in the proceeding sections.

2.1.2.1 VSC CONVETER TOPOLOGIES

I. TWO-LEVEL CONVERTER

The two-level converter has the same circuit topology as the basic line commutated converter – the Graetz-bridge. In place of thyristors, fully switched devices (typically IGBTs) are used to form each valve, consisting of an IGBT and a freewheeling diode. In each phase of the converter the valves are operated in anti-phase to generate a rectangular voltage output, fluctuating between the positive and negative DC voltage rails. The IGBT switches are used alternatively to connect the positive and negative DC terminals to the AC inductor, in order to generate a square voltage waveform at frequency of the AC network. The anti-parallel diode allows the current to flow in the other direction with minimal conduction losses, thanks to its lower junction voltage drop. This ensures the four-quadrant operation of the converter. However, the arrangement between the IGBT and the freewheeling diode implies that the complete valve will start conducting uncontrollably through the reversed diode if a negative voltage is applied across it. The DC capacitor, present on the DC side, holds the voltage and acts as a harmonic filter [8].

Pulse width modulation (PWM) is used to adjust the duty cycle, and thus average voltage, over a switching period, allowing the converter complete control over AC output voltage. To remove harmonics generated through PWM, tuned filters are placed on the AC and a capacitor on the DC side. High frequency switching, typically in the range of 1-2 kHz, helps to minimize the filtering required [12] but increases switching losses.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

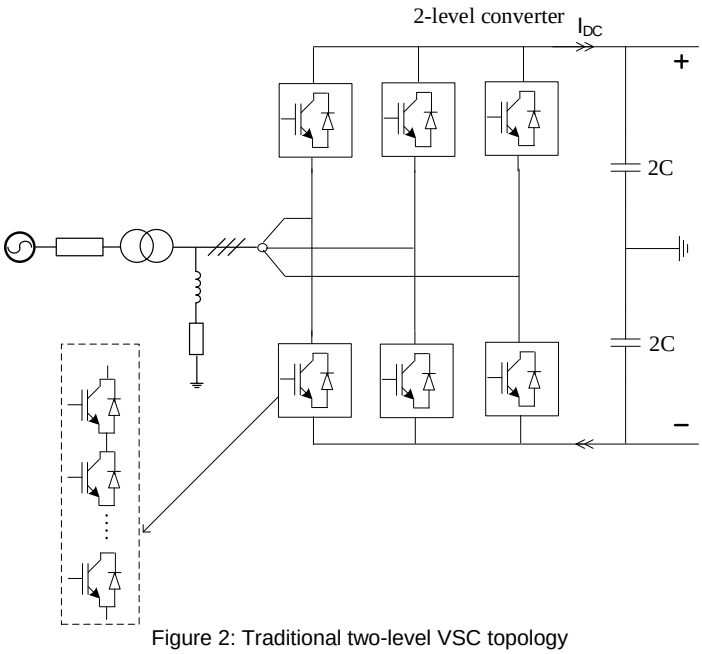

Figure 2: Traditional two-level VSC topology

Two-level converters were used for first generation VSC systems. However, several technological challenges restricted their use: ensuring adequate voltage sharing between devices becomes challenging as more are connected in series (in higher voltage/power applications); EMI generated by high dv/dt can be difficult to contain; and switching loss is also relatively large, due to high frequency PWM, making conversion losses significantly larger than a comparable LCC system. These challenges limited capacity to approximately 400 MW, restricting the range of applications [13].

When a fault occurs on the DC side, the anti-parallel diodes of the IGBTs are forward biased and start to conduct and rectify AC fault current, essentially turning the converter into a diode rectifier.

II. MULTI-LEVEL CONVERTER

Multilevel converters have improved on the two-level converter topology and allowed significant increase in power throughput, combined with reduced losses. Generally, they are defined as any VSC with three or more output levels. The modular approach using a large number of sub-modules allows achieving higher rating, easy scalability, as well as increased reliability. With a greater number of output voltage levels, harmonics generated from switching decreases and less filtering is required.

There are a number of multilevel converter topologies, each with associated functionalities. The range of these and the complexity of their operation preclude a detailed explanation within this document; however, a basic description will be given of the general principle.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

A) HALF-BRIDGE MMC

Half-Bridge MMC (HB-MMC) and its variants are seen as the main contenders for future multi-terminal HVDC applications. In place of a series connection of devices, as in LCC or 2-level converters, the MMC is constructed from a series connection of cells or 'sub-modules' (SM), see Figure 3. The modular design consists of three phases, each of them including an upper and lower arm (also named stack), as shown in Figure 3. Every arm contains an inductor (arm reactor) and a series of sub-modules, each with a capacitor regulated around an average voltage. The number of SMs varies according to the converter rating required [14]. In this case the sub-module consists of an HB valve, shown in Figure 3. In the ON-state the capacitor voltage is projected between the sub-module's power terminals; in the OFF-state the sub-module is bypassed. By varying the number of sub-modules in the upper and lower arms of a phase the AC output voltage of the converter can be controlled.

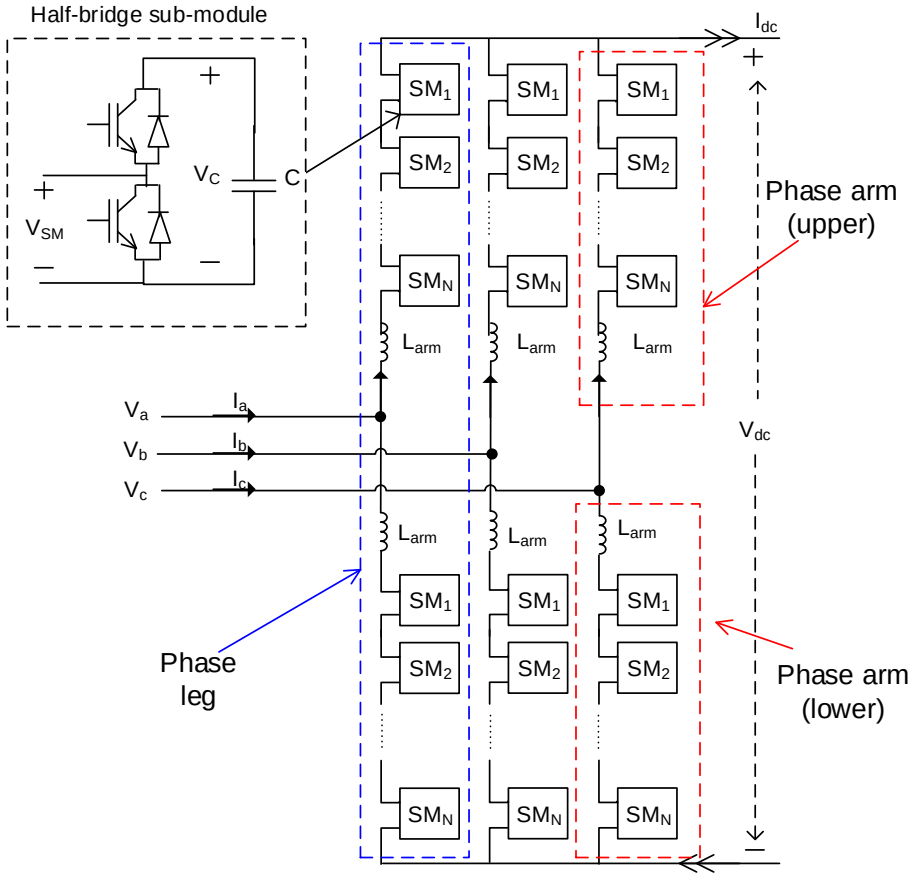

Figure 3: MMC topology based on half-bridge sub-modules

Nominal capacitor voltage is V_{DC}/N, where N is the number of sub-modules in each arm. As such, the number of voltage levels the converter can generate is directly related to the number of sub-modules used. A typically converter has in the region of 200-400 modules, allowing fine control over the output waveform, with low harmonics. Generally, harmonic requirements are met with approximately 20 output voltage levels. As such, AC filtering is generally not required, saving space. Submodule switching frequency is in the range of 100-200 Hz:

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

significantly lower than in two-level systems. Typical losses for a multilevel converter are in the region of 1% compared to 2-3% for two-level [15], allowing them to encroach on the efficiency levels attained by LCC systems.

As is the case for a two-level VSC, in an HB-MMC the antiparallel body diodes of the IGBTS are forward biased whenever the DC voltage drops below the AC voltage, i.e. during a DC fault. In this case, the HB-MMC converter essentially turns into an uncontrolled diode rectifier, rectifying AC fault current.

A number of variants of the HB-MMC have been proposed. These all operate in a similar fashion (altering the output voltage of series connected sub-modules to control the AC voltage) but with different sub-module structures. Examples such as the alternate arm converter (AAC) merge elements of the two-level converter and MMC with the use of a 'director switch' [16]. Some topologies have additional features such as fault blocking.

B) FAULT CURRENT BLOCKING CONVERTERS

In case of DC disturbances, the conventional HB-MMC is not able to block fault. Normally, increasing arm inductance is a common way to reduce over-current before blocking the converter as well as implementing high current capacity bypass thyristors to protect the semi-conductor after blocking the converter [17]. On the other hand, to counter the vulnerability of VSC to DC faults, multi-level VSC topologies with the capability of blocking fault currents have been developed. Most of these are variations on the HB-MMC topology, with SM topologies such as the full bridge, double clamped and three-level sub-module [18]. Alternative converter topologies are also possible: The Alternate Arm Converter (AAC)), for example as in [16]. However, a full description of their operation is out of scope.

Please note that the word 'blocking' is used in two different ways here which should not be confused:

- When blocking is used to describe something the converter does i.e. 'the converter blocks', 'the IGBTs are blocked', etc. the word 'blocking' refers to an action which the converter takes to protect its IGBTs (or other semi-conductor devices) from over-currents by no longer sending the turn-on commands. This means the IGBTs go into a high resistance state and no more current flows through them.
- When blocking is used to describe a property of a converter or sub-module topology i.e. a fault blocking converter, or a fault blocking sub-module, etc. it refers to the converter's ability to synthesize an opposite voltage and block DC fault current.

The full-bridge sub-module (FB-SM) is a mirrored arrangement of the half-bridge sub-module and therefore contains four pair of switches (IGBTs and diodes), names T1, T2, T3 and T4, and a capacitor C as shown in Figure 4. In the event of a DC fault in the network, VSC MMC FB is able to produce the rated AC waveform up to a complete reversal of the DC-Link voltage, thus providing DC fault blocking response [19]. It operates like a STATCOM when DC short circuit fault occurs and rides through the fault. The FB option offers a greater reliability at higher costs, larger volumes and higher conduction losses.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

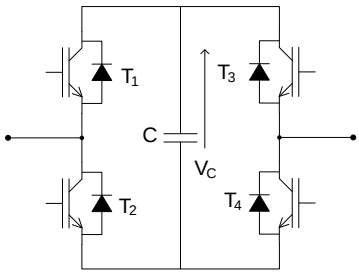

Figure 4: structure of a sub-module using full bridge sub-module (FB-SM)

For specific applications, such as point-to-point systems with long sections of overhead lines, blocking converters may be applicable. However, for large, multi-terminal networks losses become a significant deciding factor in technology choice. The increased converter losses of blocking converters make them unlikely to be used for multi-terminal systems at this stage. With lower losses, half-bridge MMC appears more appropriate at this stage.

There are other multi-level converters such as Neutral-point Clamped (NPC) and Flying Capacitor topologies can generate three or more voltage levels. However, both are somewhat restricted beyond three levels as capacitor balancing becomes complex [20]. Therefore, these converter topologies are generally limited to medium voltage applications, where a large number of voltage levels are not required. As the focus of this study is HVDC applications, they are not considered here.

2.2 CONVERTER CONFIGURATION

HVDC systems can be configured, broadly, in three ways: symmetrical monopole, asymmetric monopole and bi-pole. These terms have been carried over from LCC systems, where they referred to the pole (cable or overhead line) voltage polarity. For VSC systems the definition is less clear: monopole schemes can have positive and negative pole polarities (see symmetric monopole configuration). In fact, for VSC schemes mono/bi-pole refers to the number of converters within a station. The following sections give a brief description of the configurations possible.

2.2.1 ASYMMETRIC MONOPOLE (GROUND OR METALLIC RETURN) CONVERTER CONFIGURATION

Figure 5 shows the basic layout of an asymmetric monopolar link. One pole of the converter is earthed and the other supports full DC voltage. The return path can be provided by a metallic return or ground return type; however, the use of ground returns on a permanent basis is generally restricted. If earth return is permitted, this configuration can provide a cost efficient option, as only a single conductor is required. However, converter transformers must be designed to withstand a continuous DC voltage offset, increasing their cost [21].

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

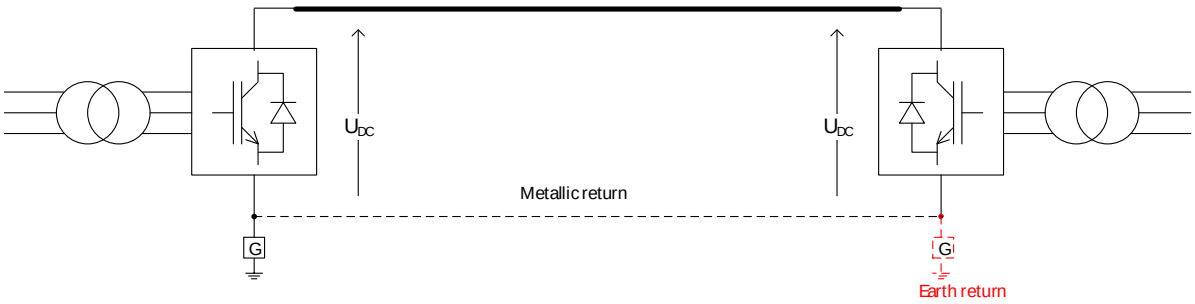

Figure 5: Schematic diagram of an asymmetrical monopolar HVDC link

The configuration has been used extensively for LCC systems, where overhead line schemes are common. (Regular, temporary faults are much more likely with overhead line, but can be readily cleared with LCC.) However, given the vulnerability of VSC to DC side faults, overhead line schemes are uncommon [22] and cable systems more prevalent. Asymmetric monopole schemes are therefore uncommon for VSC instillations, as double the power capability can be achieved with symmetrical monopole (for a given cable insulation). They can, however, be implemented as the first stage of a bipolar scheme [23].

2.2.2 SYMMETRIC MONOPOLE CONVERTER CONFIGURATION

Figure 6 shows the layout of a symmetric monopolar link. Typically, a high impedance ground is used on the secondary side of the converter transformer, with no hard grounding on the DC side. During normal operation, the two poles support equal voltage (half the rated DC voltage of the converter). Pole-to-ground faults result in healthy pole voltage increasing. In a completely ungrounded system this would result in the full system voltage being applied to the healthy cable (double nominal cable voltage). However, grounding apparatus and surge arresters used to protect the system would constrain the maximum voltage the healthy cable could reach. Transformers and other system equipment would also be placed under severe stress by the DC offset imposed. However, current stress from faults is less severe than in an asymmetric configuration [21]. Faults, in general, will result in shut-down of the effected converter/system, as no redundancy is provided (as is the case with bipole schemes).

For a given cable rating, the system can transmit two times the power of the asymmetrical configuration (assuming converters of twice the capacity are available). For this reason, the symmetrical configuration has been the preferred choice for most VSC based systems to this point, as they are predominantly cable based.

Figure 6: schematic diagram of a symmetrical monopolar HVDC link

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

2.2.3 BIPOLAR (GROUND OR METALLIC RETURN) CONVERTER CONFIGURATION

Figure 7 illustrates the bipolar converter configuration. It consists of a combination of two asymmetric monopolar systems, one with positive and the other with negative polarity, and a shared neutral point. Pole-to-ground faults in a bi-pole configuration system are similar to a pole-to-ground fault in asymmetric monopole system. Similarly, although very unlikely to occur, a pole-to-pole fault in bi-pole system resembles a pole-to-pole fault in symmetric monopole configuration.

The configuration improves system reliability compared to a monopolar scheme: a failure of a major component (converter, transformer, cable, etc.) does not result in a complete power loss. Typically, potential power throughput is reduced by half. The higher reliability provided by such arrangement comes at higher costs of transformers equipment and duplication of much of the control. The neutral return path can be provided by ground electrodes or a dedicated metallic return. The addition of a third cable allows the system to operate at 50% capacity continuously following a fault, but requires higher capital expenditure. Ground returns remove this cabling cost but, typically, it is only possible to pass current through ground for short-term periods.
Bipole configurations are commonplace in LCC based systems, where overhead lines are commonly used, as it doubles the power capacity of the converter terminal. However, cable technology is still a constraining factor on maximum system voltage (modular multi-level converters are fully scalable, and not constraining in maximum voltage).

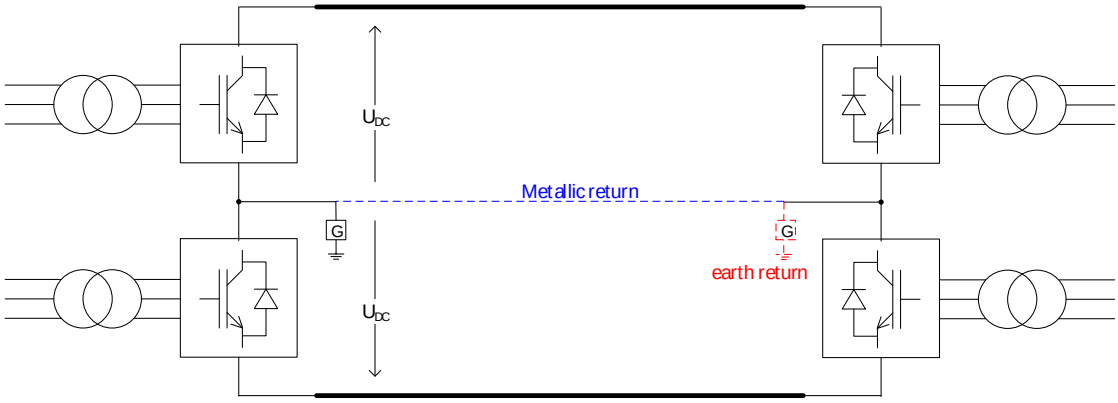

Figure 7: schematic diagram of a bipolar HVDC link [21]

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

3 MULTI-TERMINAL HVDC NETWORKS

Multi-terminal HVDC (MTDC) network is the next logical step in the evolution of HVDC power transmission. The VSC HVDC technology is preferable for building MTDC networks because of its several advantages compared to LCC HVDC technology. For instance, it does not require voltage polarity reversal in order to change power flow direction. At the moment, most of the VSC HVDC projects in operation are point-to-point interconnections with the exceptions of the recently commissioned projects in China [24], [25].

Compared to building multiple point-to-point connections, development of MTDC network offers several techno-economic advantages such as increased security of supply, optimal use of resources including existing infrastructures, increased flexibility of power trading between countries, etc. However, one of the main challenges hindering the deployment of such a network is the lack of well proven protection system that is able to clear DC side faults without leading to the collapse of the entire DC network.

In this chapter, a brief review of the background information necessary to carryout simulation studies in Chapter 4 is provided. Faults in HVDC networks, the main contributors to fault currents in different types of converter topologies and large fault current mitigation techniques currently under consideration for MTDC network are briefly discussed. A few of MTDC networks used in the literature for system transient studies are also reviewed. Finally, the chapter describes the benchmark network used for simulation studies in Chapter 4.

3.1 FAULTS IN HVDC SYSTEMS

Line-commutated converters are able to limit DC fault currents through control of the firing angle. Two-level and HB-MMC contain anti-parallel diodes in each arm which allow fault current to flow from the AC to DC side during faults (see Figure 8), making them vulnerable to DC faults. The high current can cause serious damage to internal components; namely, the freewheeling diodes that are in conduction during this period [26]. In the absence of HVDC circuit breakers, the AC circuit breaker at each converter need to open in order to prevent further infeed from AC side. This will lead the de-energization of the whole DC network and this is not acceptable from system operation point of view as this will result in significant power loss and also the system restoration time will become too long [27]. Full bridge converter topologies, which are able to block the AC current infeed into the DC fault (see Section 2.1.2.1 B), have been proposed in order to avoid such a delay in system restoration. However, this require up to twice the number of power electronic components used in the HB-MMC, and thus resulting in increased cost and power loss.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

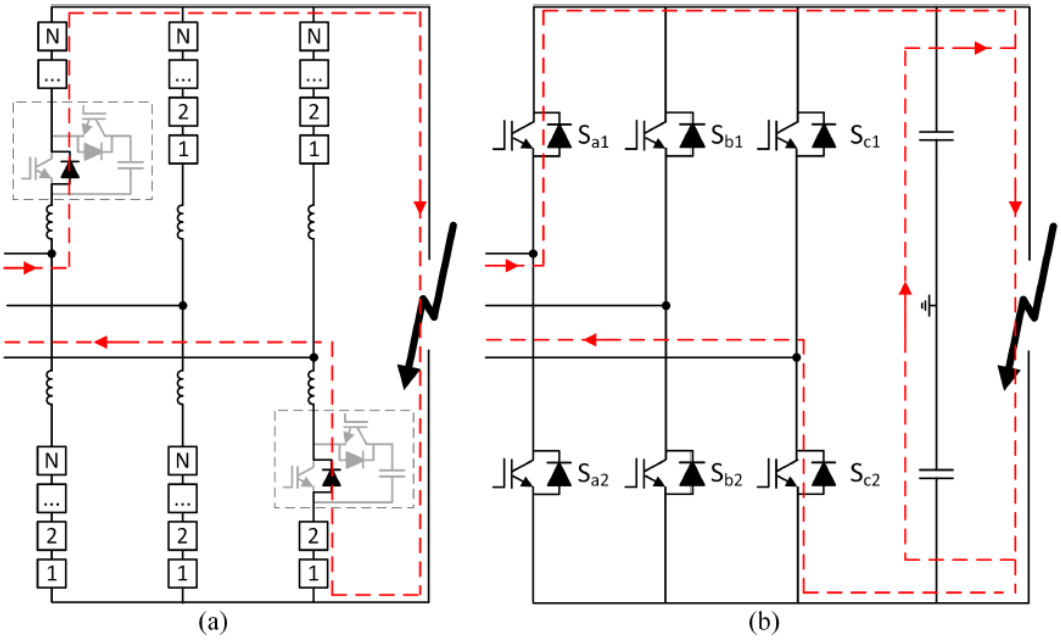

Figure 8: VSC fault current paths through free-wheeling diodes in (a) HB-MMC, (b) 2-Level converter

3.1.1 FAULT CURRENT CONTRIBUTIONS

Depending on the type converter topology, the fault currents in MTDC networks can be decomposed into contributions from various sources. In a network built from 2-level VSC converters, the first few milliseconds are dominated by the discharge of DC side filter capacitors. This is followed by the discharge of adjacent feeder cables in the system. After the discharge period of the capacitive elements is over, the AC side infeed starts. On the other hand, MMC VSC converters, there are no inherent DC side filter capacitors. Hence, the fault current is mainly contributed by the neighbouring cable connections and the converter submodule capacitor discharges. The converter submodule capacitor discharges can be prevented by blocking each of the submodules in a converter. After a converter blocks, the fault current is fed from the AC side of the nearby converters and from the other converters at remote terminals. The fault current sources in multi-terminal HVDC network have been investigated in [28].

3.1.2 FAULT CURRENT LIMITERS

A few techniques to bridge the gap between the magnitude of the prospective fault currents in HVDC networks and the speed and the maximum current breaking capabilities of the state-of-the-art HVDC circuit breakers have been proposed. One of such a method is by using DC side current limiting reactors [29], [30]. These reactors reduce the rate of rise of fault currents, thus providing more time for HVDC circuit breakers to act before the fault current exceeds the maximum limit. However, if the HVDC circuit breakers do not clear the fault current rapidly, the DC reactors have limited impact on the steady state value of the fault current in DC networks.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

The other technique is through the use of superconducting fault current limiters [31], [32]. The superconducting fault current limiters limit the peak value of fault current by increasing the resistance in the DC fault path when the fault current exceeds certain threshold. However, although it has limited impact during normal operation, the practicality of this method is still under investigation.

In addition, certain HVDC circuit breakers specifically a hybrid type HVDC circuit breaker can be operated in current limiting mode prior to current interruption [33], [34]. The main breaker of hybrid HVDC circuit breaker controls the voltage drop across the DC reactor to zero to prevent a further rise of the line current. Pulse mode operation of the main DC breaker or sectionalizing of the main DC breaker will allow adapting the voltage across the breaker to the instantaneous DC voltage level of the DC grid [34].

3.2 BENCHMARK NETWORKS FOR SYSTEM STUDIES

Because of the lack of practical MTDC VSC network in operation, the research on multi-terminal HVDC networks has been limited to simulation studies. A few of the major objectives of these studies are power flow control and dispatch, protection system studies, analysis of system transients such as magnitude and rate of rise of fault current and impacts of various types of fault conditions on system components. In this section a brief review MTDC networks used in various simulation studies is provided. Then, the description of the MTDC network used in WP5 is presented towards the end of the section.

3.2.1 REVIEW OF BENCHMARK SYSTEMS USED IN THE LITERATURE

The important aspects of multi-terminal HVDC network that have significant impact on the requirements of HVDC circuit breakers are the network topology and converter configuration. The responses of different converter configurations to various fault conditions have been studied in [35]. Several system configurations, from simple radial multi-terminal networks to densely meshed networks, under various assumptions and fault conditions have been investigated in the literature. Some research shows that the design of HVDC network topology must not only consider the optimal power flow during the normal operation, but also the resulting transient fault current during short circuit as well as the resulting post fault power flow in the system in case a fault is successfully removed [36]. The impacts of network topology on various system aspects during both steady state and transient state have been investigated in [36]. Various prospective network topologies in the North Sea, developed considering the existing high voltage substations and expansion plans of the surrounding countries, have been evaluated by simulations in order to compare the losses during normal operating condition, the maximum transient fault current and post fault contingencies. It is shown that as the level of meshing increases the transient fault current becomes large, although the densely meshed networks result in more optimal steady state power flow. However, the main limitation in this study is that only two-level VSC converters, which are currently less preferred to modular multi-level converters (MMC), have been considered. Thus the transient fault currents obtained may not be realistic for the future multi-terminal HVDC network. Even for two-level converters the accuracy is limited to the first few milliseconds which are dominated by DC capacitor and cable discharges.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

In other work, different HVDC network topologies for integration of large offshore wind farms are compared in terms of network features such as flexibility, redundancy, line lengths and ratings, the need for communication as well as the number of HVDC circuit breakers required in networks [27]. Several circuit topologies such as radial, ring, star and combination of these configurations along with various control approaches have been compared. In general, it has been determined that the requirements of HVDC circuit breakers such as speed, maximum current interruption and the amount of energy it needs to absorb depend considerably on the network topology.

In the literature, several HVDC network topologies along with various converter configurations have been used as benchmark networks depending on the specific purposes of study. For instance, in order to investigate fault current contributions of various elements in multi-terminal HVDC networks, a three-terminal radial HVDC network is considered as a benchmark in [37] and the same system is used to study the impacts of different grounding schemes [38]. In this case a bipolar converter is represented by a simple diode rectifier assuming a blocked converter during fault. A system before fault is represented by an ideal DC source connected in parallel to the six pulse diode rectifier and is used for initial charging of the cable links. This assumption allows a clear insight of fault current contributions under blocked converter condition. Besides, a four terminal meshed HVDC network developed based on the same assumption is used for investigation of current interruption capability of various HVDC circuit breaker technologies [39]. However, the fact that all converters are represented as blocked converters during a pole-to-ground fault is not realistic since in practice only the converters on the faulted pole and only stations located close to the fault are affected. In addition, the transition from normal operation to fault condition cannot be represented accurately because of the lack of a control system in this simplified assumption. In general, this approach cannot be used to represent the system when the number of nodes is large.

A four terminal meshed symmetric mono-polar network, simulated using an EMT program, is proposed as a benchmark network in [40]. Two of the converters are located offshore while the other two converters are situated onshore. From a DC circuit breaker perspective, this is suitable for pole-to-pole fault studies. A similar network topology but at reduced power and with bipolar converter configuration is considered in [41]. Another four-terminal radial network topology is defined in [30]. This system is used to simulate the benefits of DC current limiting reactors for suppressing DC fault currents. The relationship between the circuit breaker requirements and the stable operation of VSC converters in the presence of various values of DC reactor is studied.

Acknowledging the importance of having a unified benchmark system for harmonizing the research related to multi-terminal HVDC networks, CIGRÉ WG B4-57 and WG B4-58 have developed an 11-terminal HVDC system that can be split into three sub-systems [42]. Detailed data and control parameters for steady state power flow have been provided. The system can also be split into three DC systems: namely; DCS1, DC2 and DCS3, where, DCS1 is a point-to-point symmetric monopole system, DCS2 is a four terminal symmetric monopole system with one offshore load station and DCS3 is a five terminal bipolar system having both cable and overhead line links. The system also contains DC/DC converters which are yet to be realized. Part of CIGRÉ benchmark network, especially DCS3, is used as a test network in several studies [43].

It can be concluded that the choice of network topology as well as converter configuration in the technical literature is mainly driven by the purpose of the study. In most of the studies it is intended to keep the network as simple as

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

possible while maintaining the minimum requirements of meshed network. Most of the point-to-point offshore projects in operation as well as those under construction are based on symmetric monopole configuration. However, the issue of which network topology is suitable for offshore multi-terminal network remains open and needs further techno-economic analysis. For instance, a pole-to-ground fault in a network built from symmetric monopole converter results in an overvoltage as high as twice the nominal voltage. This requires the system components to be rated for such an overvoltage, which especially for the cable can be associated with a prohibitively high cost. In addition, even though the rating issue can be technically handled, the problem is the doubled floating voltage after a fault since there is no grounding point. This implies, the whole DC grid will have to be shut down, the un-faulted pole discharged, and then re-energized every time a pole-to-ground fault occur. In a bipolar network, a pole-to-ground fault results in a very large current flowing in the system, thus such a system requires very fast HVDC circuit breakers to clear the fault before the entire system collapses and continuity of supply is lost. In any converter configuration a pole-to-pole fault is the most severe, resulting in a rapidly rising fault current that can damage the system components. Also such a fault results in a rapid collapse of converter terminal voltage which is not desirable for converter control.

3.2.2 BENCHMARK SYSTEM FOR WP5 STUDY

The main objective in this study is not to compare various converter configurations, rather define a suitable benchmark network that enables the study of the impacts of DC faults on HVDC circuit breaker and hence, later defines requirements of their test circuits.

3.2.2.1 SYSTEM DESCRIPTION

In order to determine the requirements of HVDC circuit breakers (HVDC CB), knowledge of system transients during DC faults to which the HVDC CBs are subjected is necessary. As previously described in the technical literature, the expected stresses are, indeed, dependent on various system aspects such as network topology, converter configuration, system grounding, etc. Hence, a benchmark system that is both generic and sufficiently complex to understand system transients during fault as well as that enables investigation of several system design aspects is required. In this section a description of such a system is provided. The chosen system must allow sufficient study of the intended characteristics under various fault conditions. The main objective here, therefore, is to define a generic HVDC benchmark network for DC fault studies that is sufficiently large that HVDC CBs can be embedded in various locations so that a DC fault can be cleared without de-energization of the entire DC network. The number of converter terminals, converter configurations along with their technologies that enable investigation of HVDC circuit breaker requirements are selected.

The hypothetical five terminal meshed offshore HVDC network shown in Figure 9 is used as a benchmark network for the study of various fault conditions in this project. The system data for this network is adopted and modified from the DC test network developed by CIGRE WG B4-57 and WG B4-58 [42]. Three of the five terminals namely, C2, D1 and D2 are assumed to be located offshore and are interconnected via submarine cables with radial arrangement. Two converter terminals, namely, A1 and B1 are located onshore and receive power from the

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

offshore network via three DC cables as shown in the Figure 9. All converters are of the modular multi-level (MMC) type with half bridge submodules.

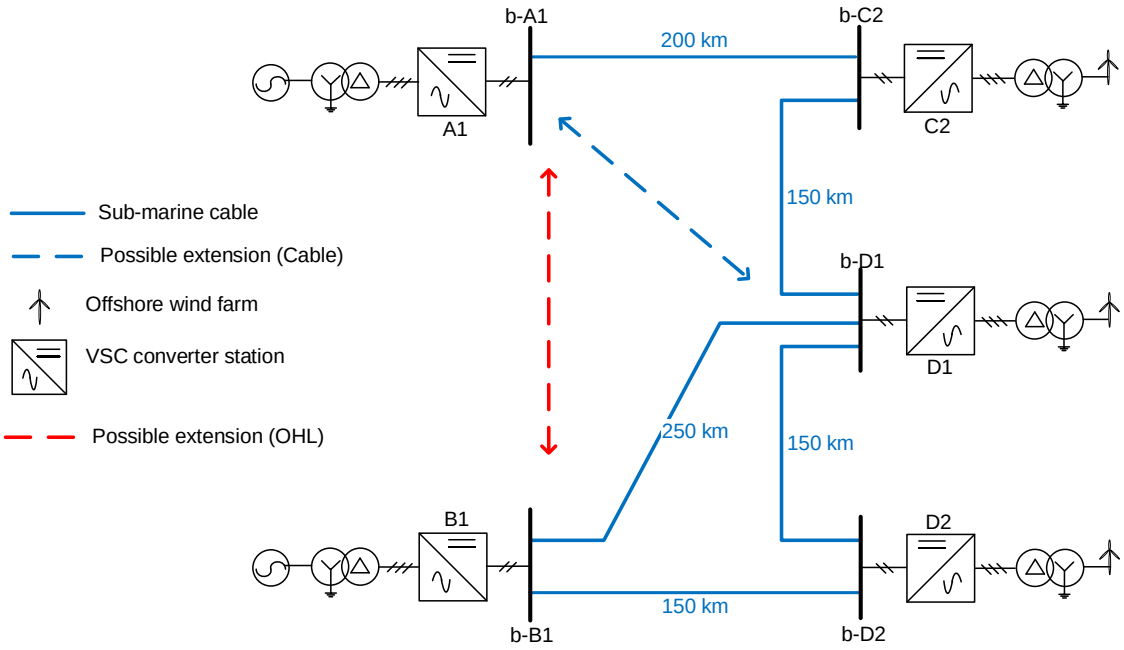

Figure 9: Five terminals meshed bipole HVDC Network. C2, D1 and D2 are offshore bipole converters

Network meshing is applied in order to provide more reliability by ensuring availability of alternative transmission paths of sufficient ampacity in case of a fault in any of the offshore DC links. In other words, unless the fault is within one of the offshore converters itself, a fault on any one of the DC links must not result in the shutdown of one or more of the offshore wind farms. Additional cable links (shown by the blue dotted arrow), and an additional overhead line (shown by the red dotted arrow), can also be connected for further reliability and network expansion. Table 3 and Table 4 show the details of the converter parameters for the network topology of Figure 9. In this network a disconnection of any of the links does not result in overloading of the healthy links.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

Table 3: Converter parameters

Parameter	C-A1	C-B1	C-C2	C-D1	C-D2
DC Voltage (kV)	±320	±320	±320	±320	±320
Converter capacity (MVA per pole)	800	800	400	800	600
AC short circuit power (GVA at PCC)	30	30	3.8	3.8	3.8
Converter transformer primary voltage (kV)	380	380	145	145	145
Converter transformer secondary voltage (kV)	220	220	220	220	220
Transformer leakage reactance	18%	18%	18%	18%	18%
Transformer series resistance	0.6%	0.6%	0.6%	0.6%	0.6%
Conduction losses in arm reactor and converter valves	0.3%	0.3%	0.3%	0.3%	0.3%
Arm reactance	15 %	15 %	15 %	15 %	15 %
Control mode	DC and AC voltage	PV droop	Active and reactive power	Active and reactive power	Active and reactive power

Table 4: Converter and system configuration

Converter Type	VSC
Converter Topology	HB-MMC
Number of SMs per arm	160
Converter Model	Detailed Equivalent Model
Modulation technique	NLC (Nearest level control)
Converter Configuration	Bipole (low impedance grounded)
DC reactor	50 to 150 mH

3.2.2.2 CONVERTER CONFIGURATION

For studying various fault conditions which may occur in multi-terminal HVDC networks, a bipole converter configuration offers diverse possibilities to investigate. Hence, a bipole converter configuration with earth return and solid earthing is mainly considered for investigation in this work.

3.2.2.3 CONVERTER TOPOLOGY, CONTROL AND MODEL

Since the main interest in this work is fault analysis on the DC side of the network, the AC network is represented by voltage source behind impedance, where the impedance is determined from the desired short circuit power at the point of common coupling (PCC). In the above MTDC network, the short-circuit power of the offshore AC is 3.8 GVA (to represent a weak network), while the short-circuit power of the onshore network is much higher (30 GVA)

CONVERTER TOPOLOGY

Nowadays, voltage source modular multilevel converters (VSC-MMC) has become the preferred converter topology because it offers several advantages such as modularity, voltage scalability, lower switching losses, better harmonic performance and fault tolerance compared to other VSC converter topologies. Besides, contrary

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

to other converter topologies, there is no inherent DC bus filter capacitor required in MMC technology. Examples of practical MMC projects include Trans Bay Cable project in USA, INELFE from France to Spain, etc. Only VSC-MMC converters are studied in the task. Thorough studies regarding the fault currents in HVDC networks using other converter topologies such as two-level and three-level technologies are available in the literature [44].

CONTROL

A hierarchical (upper level and lower level) control strategy is employed as it can be used independent of converter technology.

Upper level control: The most commonly used upper level control techniques are power-angle control and vector-current control methods. Vector-current control allows independent control of active and reactive power and has become the dominant technique in use. Upper level control consists of two control loops; namely, outer and inner controls. Outer control loop controls active power or DC voltage or droop control based on the d-component of the current and reactive power or AC voltage at point of common coupling using q-component of the current. Detailed description of different control schemes is available in the literature [42], [45].

For DC network shown in Figure 9, converter C-A1 serves as slack bus; thus, it controls the DC voltage. The control mode of C-B1 converter is PV droop control. The offshore converters operate as rectifier and control active power injected into the DC network. For simplicity, the windfarm is modelled as a voltage source behind impedance taking into account its weak short circuit power.

The inner current control produces the reference values for converter AC voltages, which is used by lower lower-level control.

Lower level control: includes algorithms for controlling circulating current suppression, modulation technique and capacitor voltage balancing.

Modulation (switching) of SMs based on NLC (Nearest Level Control) is preferred for its simplicity and suitability especially for large number of SMs. NLC uses the reference value of the voltage obtained from upper level control to determine the number of submodules to be inserted at a given simulation step. The other modulation techniques such as phase-shifted PWM (PS-PWM), space vector PWM (SV-PWM) and selective harmonic elimination (SHE) techniques become computationally cumbersome as the number of SMs increase [45] [46].

CONVERTER MODEL

A PSCAD model of MMC based on enhanced equivalent model (Detailed equivalent model with blocked operation capability), developed by Manitoba HVDC research centre (PSCAD/EMTDC™) is used with a slight modification to suit the multi-terminal HVDC network considered in this report [47] [48]. The general block diagram of converter control is provided in appendix C).

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

4 SIMULATION RESULTS

In order to address the challenges of fault current interruption in HVDC networks, it is necessary to investigate the behaviour of multi-terminal HVDC (MTDC) networks under various fault conditions. Because of a lack of practical experience related to MTDC network, the studies are carried out by simulation. The main aim of this chapter is the investigation of system transient conditions to which the HVDC circuit breakers are expected to be subjected during a fault. In other words, the prospective fault currents in a multi-terminal HVDC network under different fault conditions which the HVDC circuit breakers are expected to clear are investigated. Therefore, the impacts of various system configurations and settings including network topology, the current limiting reactors, distance and location of a fault in the network, the strength of the connected AC network and various grounding schemes are simulated in the absence of any protection system and hence, no HVDC circuit breakers either. Indeed, the ultimate intention is that at a later stage (in Deliverable 5.3) the models of HVDC circuit breakers based on the concepts proposed by various manufacturers are inserted into the benchmark network to determine the fault stresses seen by circuit breakers during DC current interruption in such a network. Eventually, the resulting stresses are used to define the requirements of test circuits to be realized in a high power laboratory where the actual HVDC CBs are expected to be tested as part of the Horizon 2020, PROMOTioN project.

4.1 TYPES OF FAULTS

The envisaged offshore MTDC network in the North Sea is mainly interconnected via submarine and/or underground cables. Although faults in cables rarely occur compared to faults in overhead lines, the former types of faults are normally permanent in their behaviour. This requires a very fast fault detection and isolation mechanism in order to avoid subsequent damages to the network's components and to avoid an interruption of supply in the healthy part of the system. Cable faults occur due to manufacturing or installation mistakes, aging or accidents due to anchors snatching cables in the seabed, etc. The most commonly considered types of faults in HVDC networks are pole-to-ground and pole-to-pole faults. Depending on the converter configuration, the pole-to-pole type of fault is the most onerous compared to the pole-to ground type although it has very low probability of occurrence. In the simulation study of this chapter, mainly a pole-to-ground fault is considered partly because of its relative high probability of occurrence and partly because the difference between the two types of faults is not very significant for the bipole converter configuration; compared to the difference in case a symmetric monopole converter configuration is studied. In this case a multi-terminal network comprising bipolar converters with solid grounding and earth return (as this results in the worst-case fault current) is simulated under various fault conditions. Towards the end of the chapter, a study results using another network built from monopole converters is provided.

4.2 IMPACT OF NETWORK TOPOLOGY

Multitudes of publications have been published regarding the influence of HVDC network topology on the magnitude and rate of rise of fault current and other aspects such as network reliability, power flow and control

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

efficiency, post fault contingency, etc. In this section, the impacts of network topology and the main contributing factors to the fault current during DC side faults are identified. In this section, two multi-terminal networks, namely, a simple radial network and a meshed network obtained by extension of the radial network are compared by keeping the same fault location in both cases. Keeping the same fault location in both systems simplifies the analysis of the impact of additional converters and their associated cable links using simulations. Moreover, for simplicity, a fault current on one side a faulted cable that is closer to the fault location is considered. The impact of the distance of the fault location from a converter is analysed in Section 4.4.

4.2.1 FAULT IN RADIAL MULTI-TERMINAL NETWORK

A four terminal radial network derived from the benchmark network defined in Section 3.2 is shown in Figure 10. This HVDC network is used for the study of fault currents in radial systems. The system is obtained by removing one of the converters (converter B1) and its interconnection from the benchmark network. In order to keep current flow in the network within cable ampacity limits of each link, power reference for converter D2 is changed. Thus, instead of injecting 900 MW power into the DC side, converter D2 is set to receive the same power from the network by changing the sign of its power reference value. The remaining power flow imbalance is adjusted by converter B1 which serves as slack bus in the system.

When a system reaches steady state power flow, a pole-to-ground fault is applied (on a positive pole) at 20 km from converter D1 on a link between converters D1 and D2. Note that, a fault is applied at 1 ms since the simulations are performed on snapshot saved after the system has reached a steady state condition. Also in this simulation case, there is no current limiting reactor put on the DC side of the system. The magenta circles in Figure 10 show the location of measurement points (also these are locations HVDC circuit breakers are expected to be installed). Focusing on CB5 of Figure 10, which is the circuit breaker closest to the fault location, the simulation results of this fault condition are shown in Figure 11. Assuming fast protection and the availability of an HVDC circuit breaker, CB5 would be the first to clear the fault if the healthy part of the system is to stay in operation.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

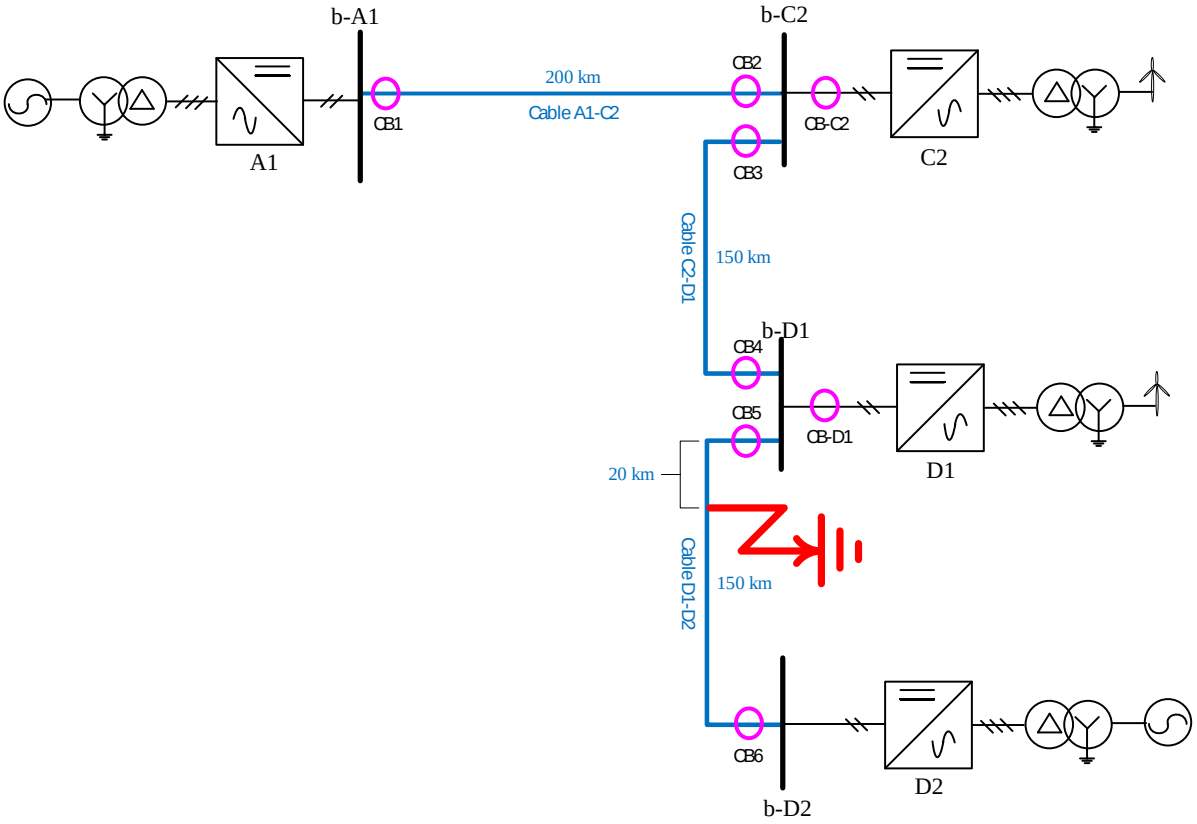

Figure 10: Fault study in radial MTDC network topology

Considering Figure 11, the top graph shows current at CB5 (red curve) and the contributions from cable discharges. The phenomena following the occurrence of the fault are described as follows. The moment a fault is applied, a ~~negative~~ travelling voltage wave travels along the cable in either direction away from the fault location. Considering only the propagation in the direction of CB5, when this wave arrives at DC bus b-D1 connected to converter D1, the bus voltage collapses as a result (see the red curve in the bottom graph of Figure 11) which has two consequences. The first consequence is that the wave partly propagates along cable C2-D1 and hence inducing the discharge of this cable shown by the blue curve of the top graph in Figure 11. The other consequence is that part of the wave travels into converter D1 which results in the discharge of the submodule capacitors of this converter shown by the red curve in the middle graph of Figure 11. Thus, until the travelling voltage wave reaches the next nearest DC bus (b-C2), the fault current is composed of these two discharges. Note that, the cable discharge results in an abrupt increase in current whose rate of rise is only determined by the negligible cable inductance up to the fault location. However, the discharge from the submodule capacitors is not as steep as the discharge from cable C2-D1 because of the presence of arm reactors (0.15 p.u.) in each phase arms of the converter.

When the converter DC current reaches the threshold value (6 kA in this case [42]), the gate signals of the IGBTs are blocked. The discharge from the submodule capacitors is inhibited by converter blocking in order to protect the converter IGBTs from the subsequent overcurrent. This can be seen as the first peak of the red curve in the

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

middle graph of Figure 11. However, as discussed in Chapter 3, since the modelled converter uses half bridge MMC technology, the fault current continues to flow from the AC side via the freewheeling diodes associated with each IGBT. The converter now essentially behaves as a diode rectifier. Similar phenomena occur at the other two converter terminals C2 and A1 but shifted in time by the time it takes for the voltage transient to propagate through the network. The magnitude of AC infeed is determined by the impedance from the converter to the fault location, the power rating of the converter and strength of AC network.

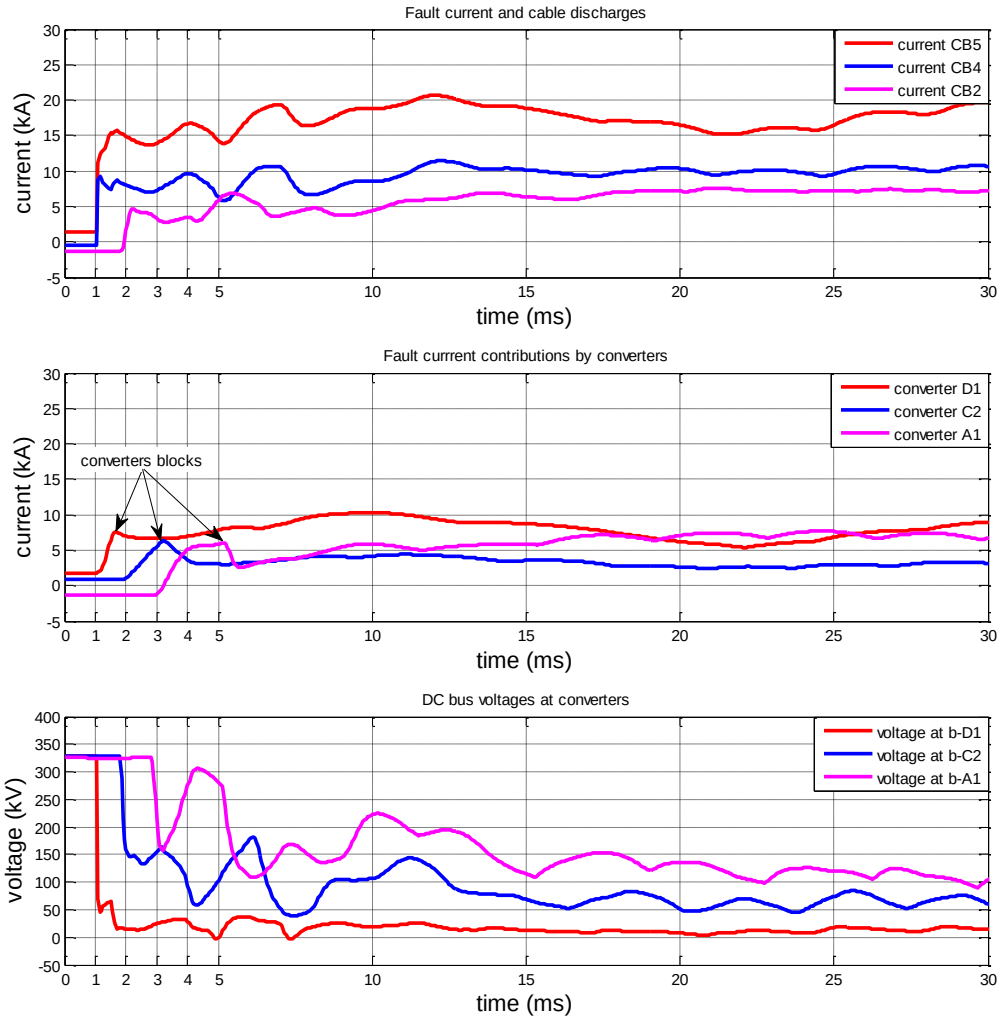

Figure 11: Simulation results of four terminal radial network topology

The plots in the bottom graph of Figure 11 shows the voltage waveforms at converters' DC buses. Depending on the distance of the fault location from the converters, the voltage drop is seen at different times at each converter. Converter controls do not function properly when the terminal voltage drops considerably; for instance, in some cases it is suggested that 80% of the nominal voltage is the minimum threshold with which the converter controls operate properly. Note that the voltage at the converter terminals drops rapidly and that the converter may not wait for the overcurrent threshold to be exceed but block on under voltage. This is taken into account in the

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

proceeding sections where the converter blocks not only based on DC overcurrent, but also based on DC under-voltage.

4.2.2 FAULT IN MESHED NETWORK

Here a five terminal benchmark network described in Section 3.2 is used to study the impact of an additional converter and its associated cable links on the fault current. Similar phenomena as described in the previous section for multi-terminal radial network take place. Considering the first 3 milliseconds, it can be seen from Figure 13 that the fault current measured at CB5 is higher than the corresponding fault current in radial network (shown by red dashed curve for comparison). The difference is due to the discharge from the additional cable link between converter D1 and B1 (cable B1-D1).

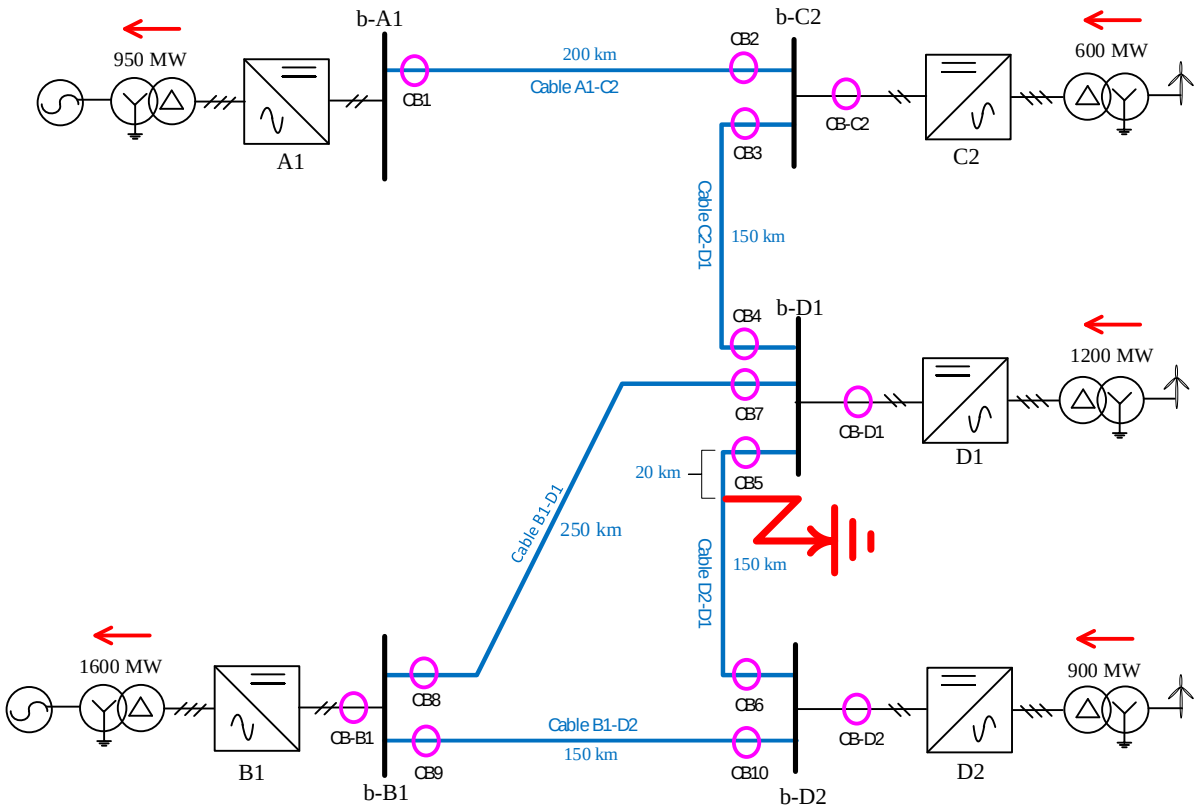

Figure 12: Fault study in five terminal meshed HVDC network

The discharge from the cable B1-D1 is shown in top graph of Figure 13 (see the black curve). As can be seen from the figure, the difference in magnitude of fault currents between the two systems is exactly the discharge of the cable B1-D1 during the first 2 ms after the fault. After the cable discharge is over, the negative travelling voltage wave arrives at converter B1. In a similar way as described in the previous section this will lead to the discharge of submodule capacitors until the blocking signal is triggered. Besides, since the distance from converter B1 to the fault location along cable B1-D1 is 270 km and along cable B1-D2 is 280 km, the travelling waves from both directions of the fault point reach this converter almost at the same time (circa. 50 µs time

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

difference). Hence, the discharge from submodule capacitors until blocking and the subsequent AC infeed from converter B1 are split into the two directions. This can be seen from the current measured at CB-B1 (the bottom graph in Figure 13) where it is not entirely reflected in the current measured at CB5 (top graph). From this, it can be deduced that the worst case for the fault current through CB5 would be if converter B1 is connected to the rest of the system only via cable B1-D1.

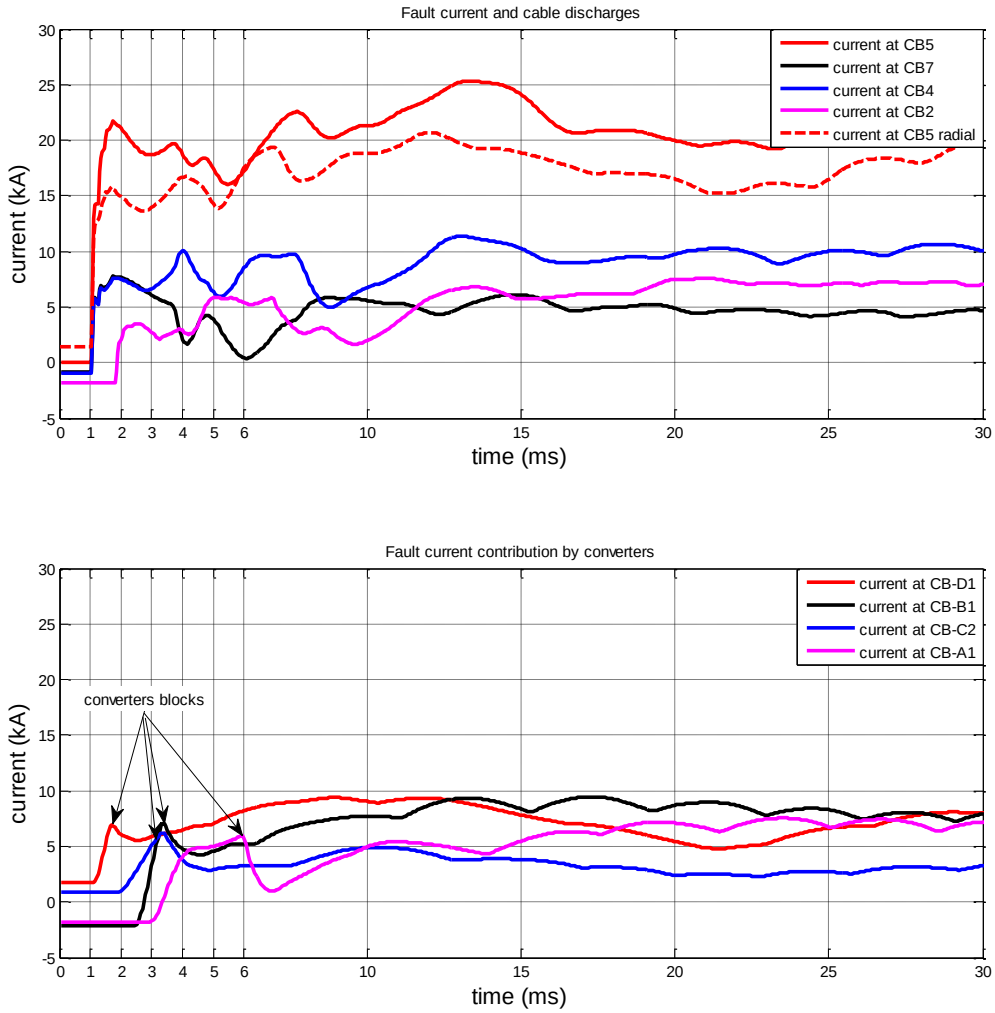

Figure 13: Simulation results of five terminal meshed HVDC network

From the bottom graph of Figure 13, it can be seen that after converter blocking the fault current is fed from the AC side through the six pulse rectifiers. Under this condition, the important factors that determine the magnitude of AC current infeed from each converter are; the distance of the fault location from the corresponding converter which is directly related to the cable resistance and more importantly the strength of the connected AC network which determines the AC side impedance. This can be observed from Figure 13 (bottom graph) where the magnitudes of the AC side contribution from the converters A1 and B1 are higher than the infeed from the other

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

remaining converters albeit these converters are located farther from the fault location. Converters A1 and B1 are connected to an AC network with short circuit capacity of 30 GVA at the point of common coupling (PCC) whereas the remaining converters (C2, D1 and D2) are connected to wind farms represented by an AC network with a low of short circuit capacity of about 3.8 GVA. The impact of AC network strength is described in detail in Section 4.6. Besides, the converter transformer leakage reactance (for instance, set as 0.18 p.u.) as well as the size of arm reactors (for instance, set as 0.15 p.u.) which are inversely related with converter power rating (see Section 3.2.2) limit the magnitude of the AC infeed.

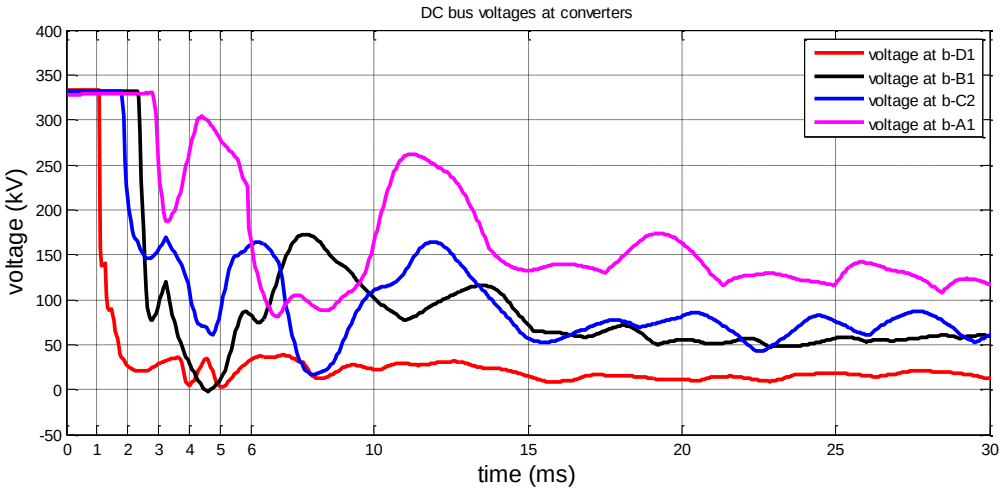

Figure 14: DC bus voltages at converters terminals during fault

Figure 14 shows the DC bus voltage at each converter terminal. It can be observed from the plots in this figure that the voltage at each converter drops instantly the moment the travelling waves from the fault location arrive at the converter terminals, leading to the collapse of the voltage of the entire DC network within 2-3 ms after fault occurrence. The travelling waves are reflected and, travel back and forth between the converter terminals and the fault location; thus, resulting in multiple peaks with a frequency depending on the distance of the converter from the fault location. Unless otherwise, the fault is cleared and the system is put back to operation rapidly, this will induce undesirable disturbances to the connected AC systems.

4.3 IMPACT OF CURRENT LIMITING REACTOR

One of the methods proposed in the literature to limit the rate of rise of DC fault current is the use of current limiting reactors on the DC side. Figure 15 shows simulation results when a 100 mH reactor (chosen for the purpose of example) is inserted at the ends of each cable in the network. The DC current limiting reactors not only reduce the rate of rise of current coming from the converters but also significantly reduce the discharge current from the neighbouring feeder cables.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

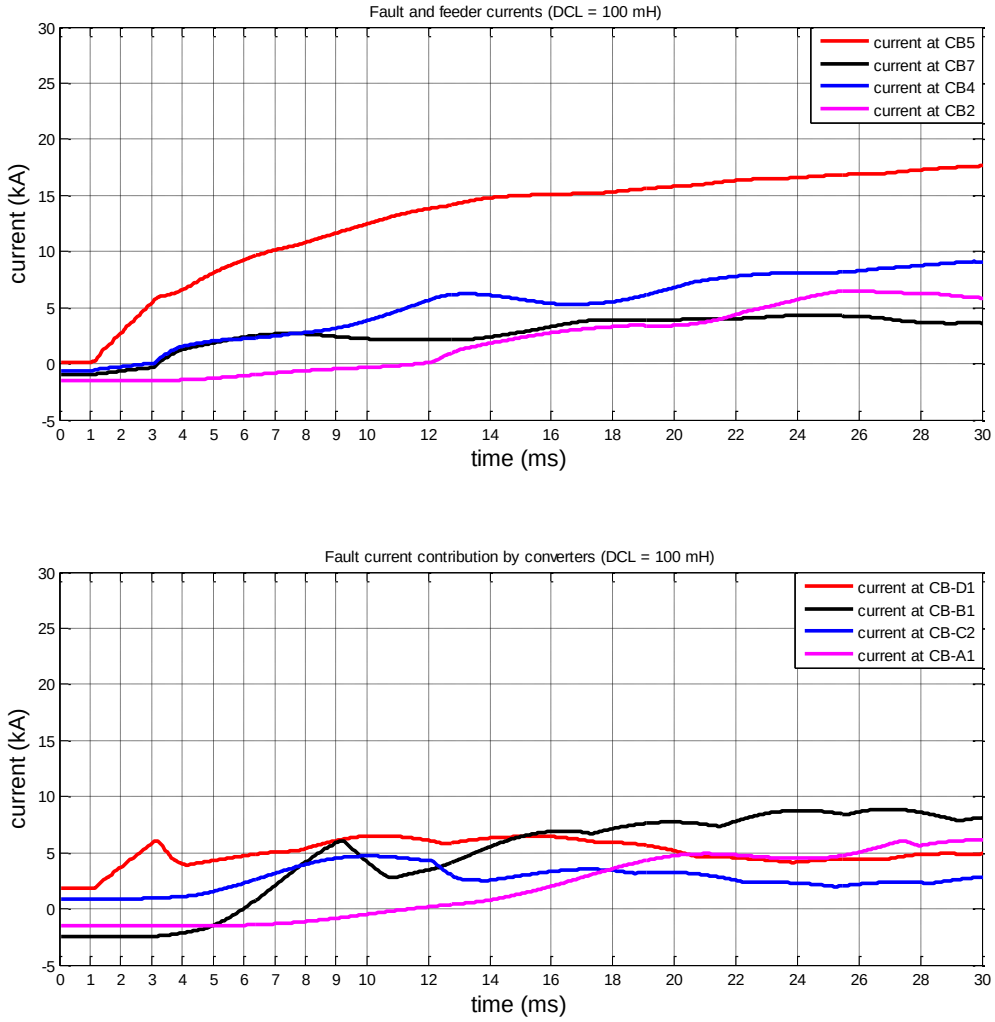

Figure 15: Impact of DC current limiting reactors on magnitude and rate of rise of fault current

Considering only converter D1, the fault current coming from this converter rises relatively slowly (see red curve in the Figure 15, bottom graph) compared to the system without DC fault current limiting reactors described in Section 4.2.2. Similarly, the DC bus voltage of this converter does not fall instantly instead decreases steadily until converter blocks (see Figure 16).

Moreover, the slow rate of reduction of the DC bus voltage at converter D1 (until blocking) suppresses the discharge current from the cables connected to bus b-D1. However, the moment converter D1 blocks (just after 3 ms in Figure 15 top graph), the terminal voltage drops suddenly and; consequently, the discharge from the feeder cables increase although the DC reactors significantly reduce the rate of discharge. By putting DC current limiting reactors at the end of each cable, the discharge of the neighbouring feeder cables is suppressed by two reactors in series; first by the current limiting reactor on the feeder cable itself and second by the current limiting

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

reactor on the faulted cable. This is observed from the blue and black curves in the top graph of Figure 15 where the rate of rise of current slightly increases following the blocking of converter D1.

In Figure 16, the DC bus voltages at converters' terminals are shown when a DC side reactor of 100 mH is used at each cable end. As mentioned earlier, in the presence of current (di/dt) limiting reactors the voltage drops gradually until the converter blocks because of overcurrent and/or under voltage. It can be seen that the converters' blocking times are much longer compared to when no DC side current limiting reactor is used in the system (e.g. see Figure 14). Except for the converters located at either ends of the faulted link which block within 2-3 ms after fault occurrence, the other converters do not block until 8 ms after the fault. The blocking time of a converter is actually dependent on its distance from the fault location and the power rating of the converter, which translates to the size of submodule capacitor.

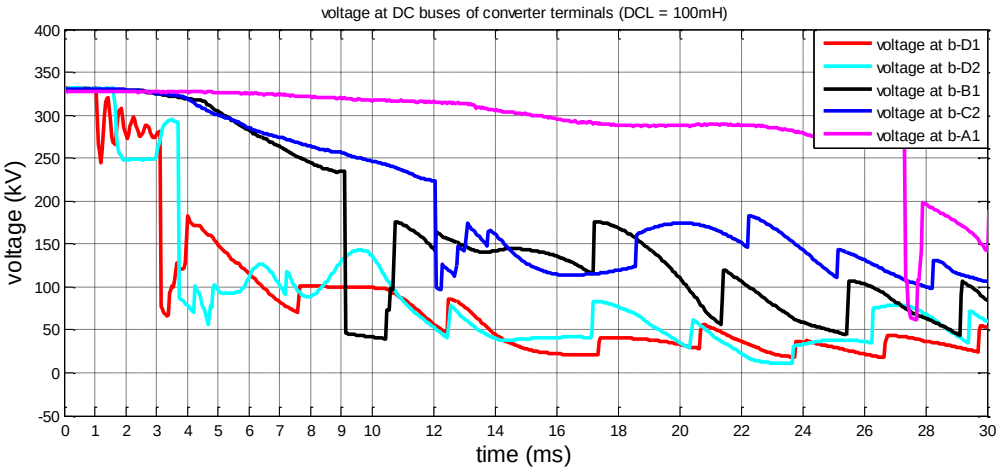

Figure 16: Converter voltage during fault when 100 mH DC side reactor is used

The impact of the size of DC current limiting reactors is described in Section 4.7.

4.4 IMPACT OF FAULT LOCATION

The position of a fault in a multi-terminal HVDC network is another key factor that determines magnitude and the rate of rise of fault current. The location of the most severe fault condition is determined by several factors such as whether overhead line or cables are used in the network, the distance of fault from the node with multiple connections, power rating of the closest converter terminal, etc.

In order to study the impacts of a fault location within a network as well as its distance from a converter station, multiple simulations are performed each time applying a fault at 10 km from a given converter station. Figure 17 and Figure 18 show the fault current measured at the ends of the faulted link where circuit breakers are expected to be installed (as depicted in Figure 12). The top graphs show current measured when a fault is applied at 10 km from the measurement point. The bottom graphs show the current measured at the same location but when the fault is applied at 10 km from the opposite end of the same cable.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

The phenomena following fault occurrence are illustrated by considering two time intervals; the time interval until converter blocking and the time interval after converter blocking. Considering the time until converter blocking, the following is observed;

- For very long cables a fault closer to a converter terminal results in low initial rate of rise of current compared to when the fault is on the remote end of the same cable. This is due to the travelling waves between the fault location and the converter DC terminal, which slightly increases the average DC voltage upon travelling back and forth when a fault occurs close to the DC bus. Thus, on average the voltage dip when a fault is close to a converter is smaller than when a fault is at the remote position on the same cable. This is because of the fact that the part of the incident wave arriving at the DCL is reflected back and has to travel back to the fault location and travel back again. By the time the reflected travelling waves from the fault location arrive at converter terminal the second time (now positive wave front), the converter submodule capacitors discharges significantly in the meantime. This effect is more visible when the length of the cable increases and also when the speed of the travelling wave is low. Hence, this is the reason why compared to the top graphs showing the fault current for a fault at 10 km, the rate of discharge of submodule capacitors (until blocking) is higher in the bottom graphs of Figure 17 and Figure 18, especially for the faults on cable A1-C2 and cable B1-D1. These two cables are the longest cables in the network with lengths of 200 km and 250 km, respectively.
- The magnitude and direction the load current flowing through the faulted link prior to the inception of fault has also impact. If a large load current is initially flowing before the inception of fault in the same direction as fault current would be, the converter blocks in a relatively shorter time compared to if the load current is flowing in the opposite direction of the fault current, because in this case the current threshold is reached relatively faster.
- Keeping the same energy per submodule capacitors for all converter stations, the higher the power rating of a converter the higher the rate of rise of the fault current is until converter blocking due to larger submodule capacitors. This is also related with the size of the arm reactor which is, for instance, chosen to be 15% of the base impedance as shown in Section 3.2.2.3. Thus, given the same AC side voltage, the arm reactor gets smaller with increasing converter power rating, which in turn means the rate of discharge of submodule capacitors increase until converter blocking. The magnitude of the arm reactor also affects the AC infeed at later stage as it provides impedance.

After converter blocking,

- Because of the half bridge submodules, the fault current is coming from the AC side through a six-pulse rectifier. Although very much depends on the converter parameters related to its power rating, the faults located closer to a converter station result in higher AC infeed fault currents. This is mainly due to increasing DC resistance of a DC cable with the distance of the fault location.
- A fault located close to a DC node with multiple connections results in large fault current due to contributions from the multiple connections.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

- The leakage reactance of the converter transformer limits the magnitude of the AC infeed current. Depending on short-circuit impedance specifications, the transformer leakage reactance (usually expressed as percentage of base impedance 10-20%) decreases for higher power ratings.

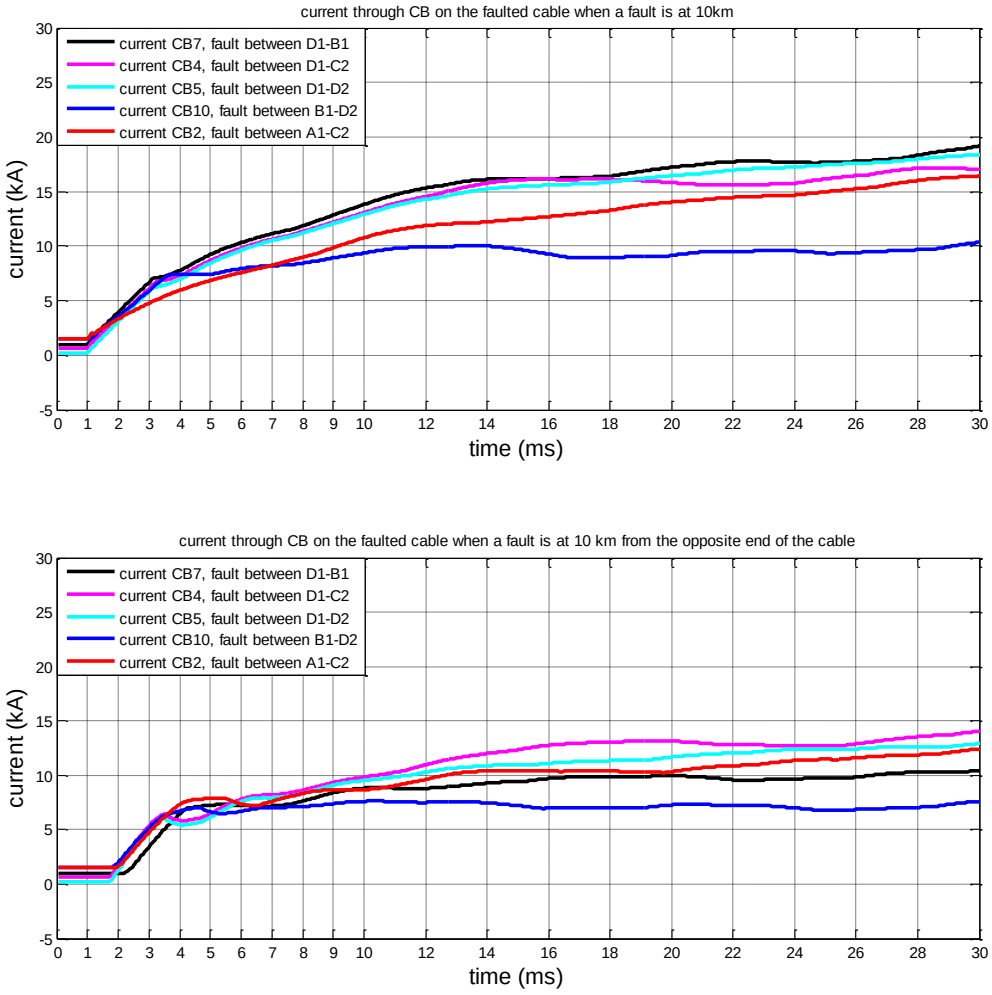

Figure 17: Impact of fault location on the magnitude of fault current (part I). A fault applied on each link, top graph fault current measured at CB 10 km from the fault, bottom graph current measured at the same CB when fault is applied at 10 km from the opposite end of the same cable.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

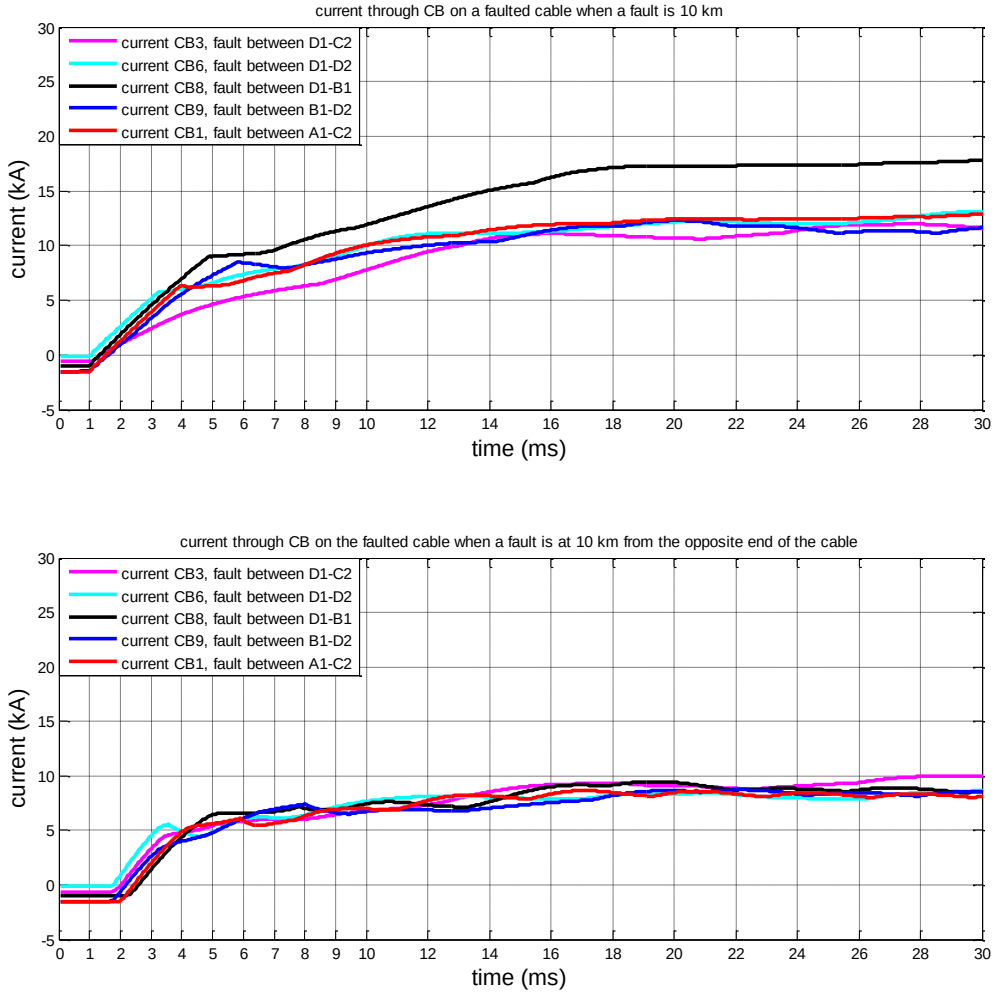

Figure 18: Impact of fault loaction on the magnitude of fault current (part II). Top graph fault current measured at CB 10 km from the fault. Bottom graph, the fault current measured at the same CB when a fault is applied at 10 km from the other end of the same cable.

4.5 IMPACT OF CONVERTER BLOCKING

In the technical literature the impact of converter blocking on the fault currents and hence on the requirements of HVDC CBs is not investigated thoroughly. In most of the publications, either a blocked converter is assumed initially (thus only rectifier circuits are analysed) or the converter not blocking at all is considered. Besides its requirement during system energization, converter blocking is crucial mainly for two reasons; the first is to protect the converter power electronics from damage due to over-currents during DC faults. The second reason is in order to avoid DC under-voltage, resulting from significant discharge of submodule capacitors, which in turn affects the proper operation of converter controls. However, in the presence of sufficiently fast protection and fast HVDC circuit breakers the need for converter blocking as well as the logic and the threshold values for converter

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

blocking must be reconsidered. Unless the fault occurred within the converter itself, a sufficiently fast network protection system should remove a fault from the DC system before any converters connected to healthy links reach an operational state from which no smooth resumption of normal operation is possible anymore, thus guaranteeing continuity of supply.

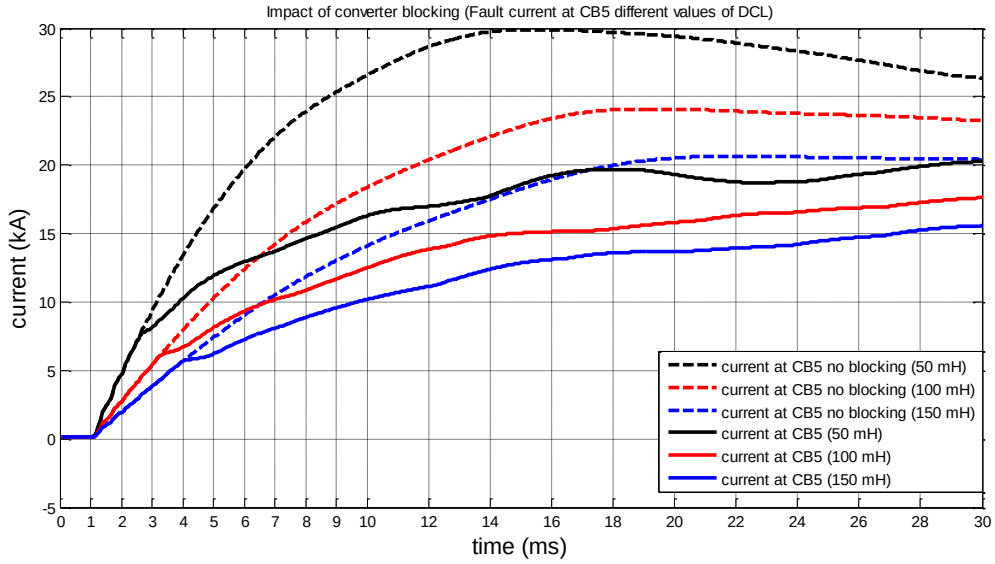

Figure 19: fault current at CB5 when converters blocks at 6 kA (solid line) and when converters do not block at all (dashed lines)

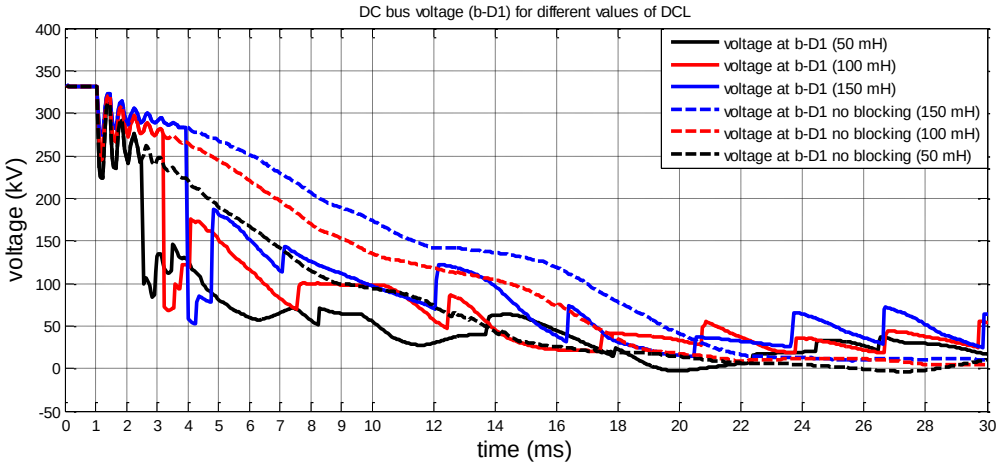

Figure 20: Voltage at DC bus b-D1. The impact of DCL on converter voltage

During normal operation, the converter acts as a controlled voltage source. When the converter blocks, it changes into a six-pulse diode rectifier and during DC fault condition, the DC side voltage of the rectifier much depends on the AC side impedance. Figure 19 shows the impact of converter blocking on the fault current when different values of DC side reactors are used. For DC reactor value of 50 mH, the fault current rises rapidly to about 20 kA in 5 ms after a fault when a converter is not blocking (see Figure 19 the dashed black curve). This is mainly because of the continued discharge of the submodule capacitors of converter D1. However, when a converter

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

blocks the fault current (shown by the black solid line in Figure 19) rises at a much slower rate. In general, when the size of DC reactor increases, the difference between fault currents when a converter blocks and when a converter does not block decreases. Indeed, it is important to retain minimum energy levels in the submodule capacitors in order to be able to smoothly resume operation. Thus, depending on the speed of protection system as well as the speed of operation of HVDC circuit breaker, it is desirable to make sure that the proper size of DC reactor is chosen so that the DC fault is cleared before converter threshold values for blocking are reached. Therefore, the converter continues in its controlled operational mode and current depending on the speed of HVDC circuit breaker, it might be possible to clear the fault before the converter blocks itself.

Moreover, the contributions from the other feeder cables as well as the converter stations connected thereby depend on the bus voltage of a converter close to the fault. Hence, if a converter does not block, this voltage is entirely determined by the total voltage of the submodule capacitors inserted across each phase leg of a converter. It is shown in Section 4.3 that, in the presence of current limiting reactor on the DC side, the DC bus voltage decays slowly at a rate inversely proportional to the size of DC reactor. Figure 20 shows the converter DC side voltage during fault when a converter is blocking and also when a converter does not block for different sizes of DC reactor. It can be seen that the DC bus voltage drops substantially as soon as the converter blocks compared to when a converter continues its operation without blocking. The collapse of the DC bus voltage following converter blocking induces further discharge of the feeder cables as well as the converters connected to the remote ends of these cables.

4.6 IMPACT OF AC NETWORK STRENGTH

In this section, the influence of the strength of the neighbouring AC network is studied. Although the impact of AC network strength can be seen in most of the simulation results discussed in the preceding sections, in order to clearly observe this, the strength of AC network connected to converter D1 is changed from 3.8 GVA to 20 GVA. Simulation result displayed in Figure 21 shows that the strength of the AC network does not affect the fault current until converter blocking. However, it has a strong impact on the magnitude of the AC infeed current after the converter is blocked. Although the DC side reactor does not affect the steady state value of the AC current infeed, it reduces the rate of rise during the build-up of the infeed current. That is why there is no significant difference in the magnitude of the fault current during the first 5 ms seconds after converter blocking. The relationship between AC grid strength and the magnitude of DC fault current is studied in detail in [49], [50]

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

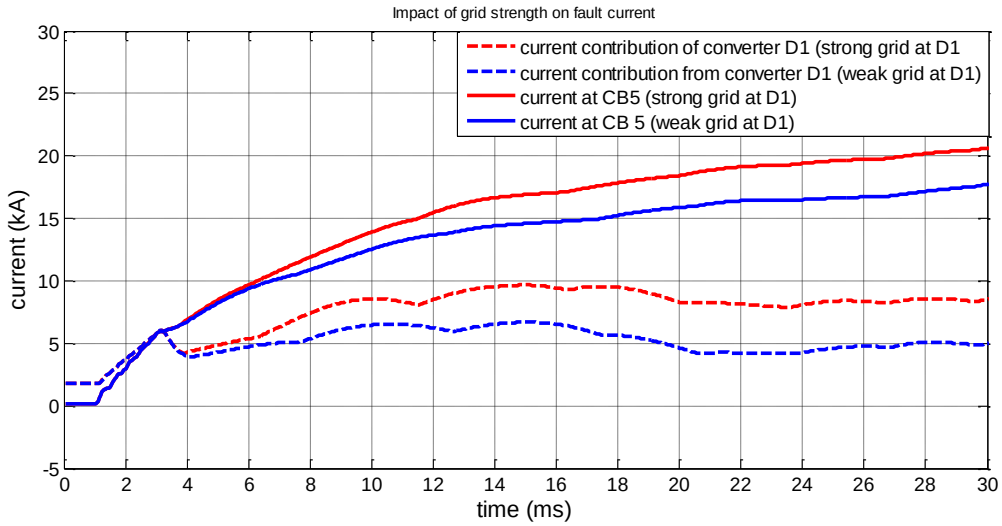

Figure 21: The impact of the strength of the AC network connected to a converter nearby fault

4.7 IMPACT OF THE SIZE OF CURRENT LIMITING REACTOR (DCL)

Application of DC reactor or current limiting reactor (DCL) in the HVDC networks is one of the effective methods to mitigate DC fault current. It is known that DCL can limit the rate of rise of fault current and mitigate DC fault current amplitude at the time when HVDC CB operates. In this section, the impact of the size of DCL on fault current is illustrated by simulation.

In order to also study the fault behaviour of a network built from symmetric monopole converters, the network shown in Figure 22 is investigated. This model consists of a four-terminal HVDC network with four symmetric monopole VSC stations connected via DC cable links. The length of the individual cable systems are set to 120 km, 240 km and 360 km, similar to the case of the radial UHV AC network that is used in previous CIGRE studies, in order to evaluate HVAC circuit breaker requirements [51]. The system parameters of this model are shown in Table 5.

As converter configuration is symmetric monopole and the converter grounding scheme is high impedance, the fault current when pole-to-ground fault occurs in this network is limited. Therefore, pole-to-pole fault near B-C/S is applied as severe fault condition. The fault current can be reduced by inserting a DCL to the DC lines. In this model, DCLs are located at both ends of each cable and near the connecting converter stations (C/Ss). The DCL values are varied for each simulation case and DC fault current behaviour for the range of values is studied.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

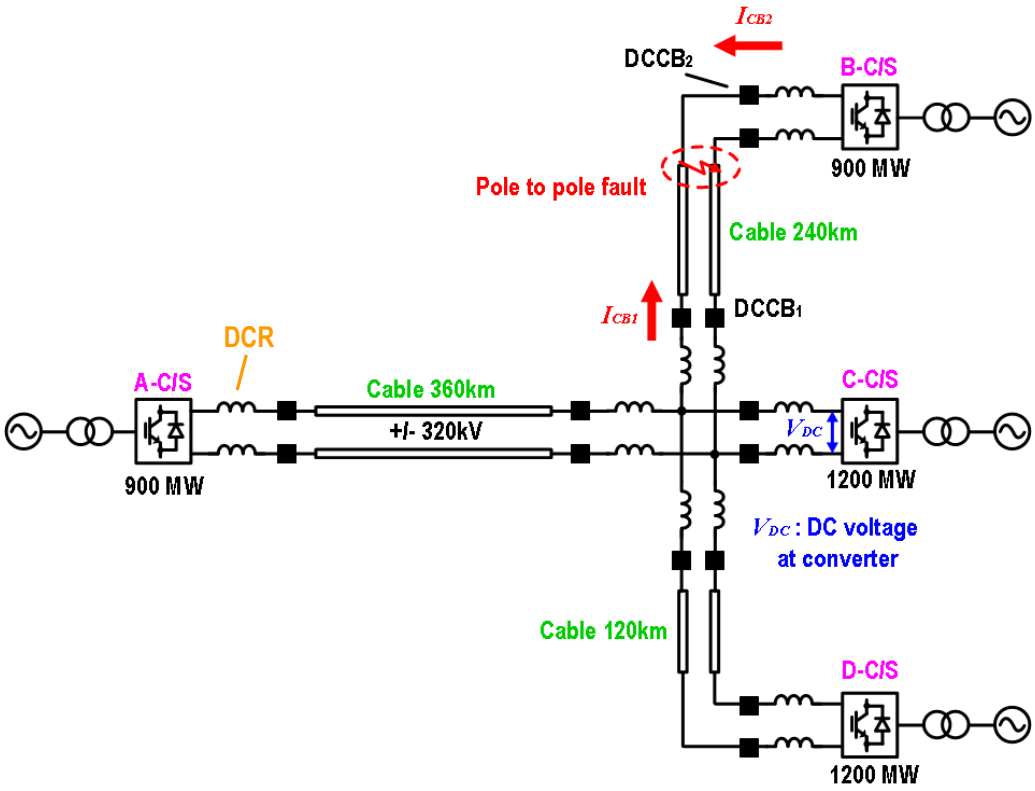

Figure 22: Four-terminal radial HVDC network model (symmetric monopole converter configuration)

Table 5: System parameters of four-terminal radial HVDC network

Parameter	A-C/S	B-C/S	C-C/S	D-C/S
DC voltage	+/-320 kV	+/-320 kV	+/-320 kV	+/-320 kV
Converter capacity	900 MVA	900 MVA	1200 MVA	1200 MVA
AC network voltage	400 kV	400 kV	400 kV	400 kV
AC network capacity	20000 MVA	8000 MVA	15000 MVA	15000 MVA
Transformer primary voltage	400 kV	400 kV	400 kV	400 kV
Transformer secondary voltage	320 kV	320 kV	320 kV	320 kV
Transformer leakage reactance	20%	20%	20%	20%
MMC arm inductance	10%	10%	10%	10%

Figure 23 shows the behaviour of the fault current through HVDC CBs located at both ends of faulty cable (I_{CB1}, I_{CB2} in Figure 22) for different values DCL in the four-terminal HVDC network. To observe only the impact of the DCL on fault current behaviour, converter gate blocking is not applied in the presented simulations. Table 6 summarizes the DC fault current amplitude at specified elapsed time from fault occurrence.

When a fault occurs at the DC line (at t = 300 ms in Figure 23), the discharge current from DC cables appear at first, and then, fault current continues to increase above 30 kA due to the fault currents flowing from converters. The simulation results show that a larger DCL can suppress the rate of rise of fault current effectively. The DC

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

fault current at each HVDC CB is less than 15 kA with 150 mH DCL and less than 23 kA with 50 mH DCL after 10 ms from when the fault occurs.

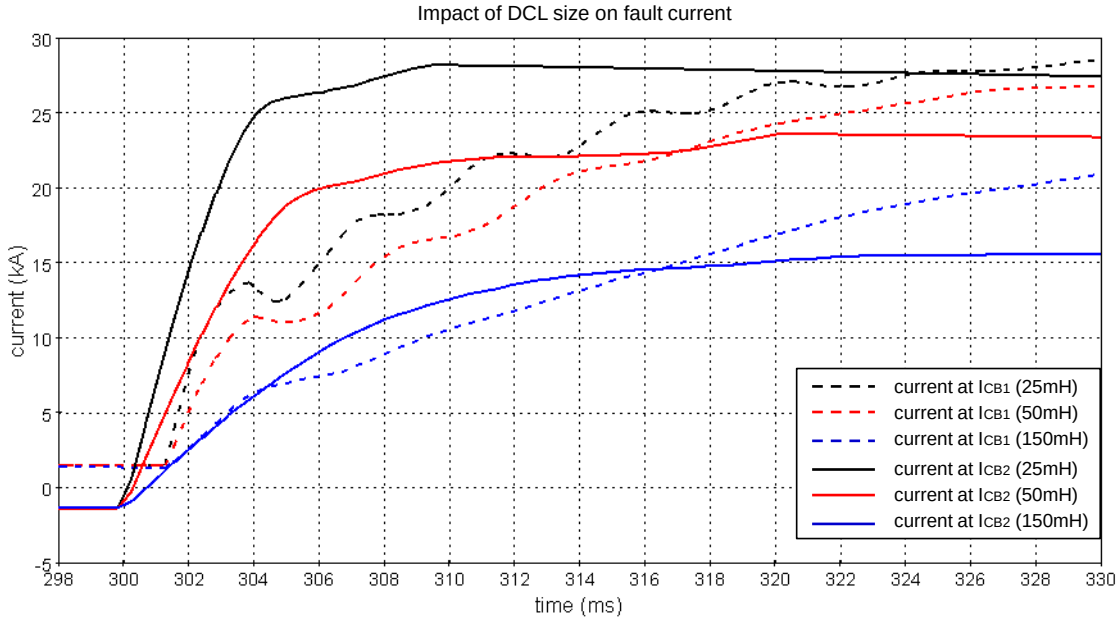

Figure 23: DC fault current behaviour in four-terminal radial HVDC network

Table 6: DC fault current amplitude at specified times

I_{CB_B1}(central node side)						
DCL value	5 ms (from the fault occurrence)	10 ms	20 ms	30 ms	40 ms	50 ms
25 mH	12.60 kA	19.98 kA	26.98 kA	28.48 kA	30.17 kA	32.88 kA
50 mH	11.03 kA	16.70 kA	24.22 kA	26.85 kA	28.67 kA	31.49 kA
150 mH	7.13 kA	10.74 kA	17.14 kA	21.27 kA	24.22 kA	25.66 kA

I_{CB_B2}(converter side)						
DCL value	5 ms (from the fault occurrence)	10 ms	20 ms	30 ms	40 ms	50 ms
25 mH	25.98 kA	28.17 kA	27.78 kA	27.40 kA	27.03 kA	26.67 kA
50 mH	18.78 kA	21.75 kA	23.52 kA	23.35 kA	23.13 kA	22.91 kA
150 mH	7.80 kA	12.65 kA	15.14 kA	15.67 kA	15.79 kA	15.64 kA

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

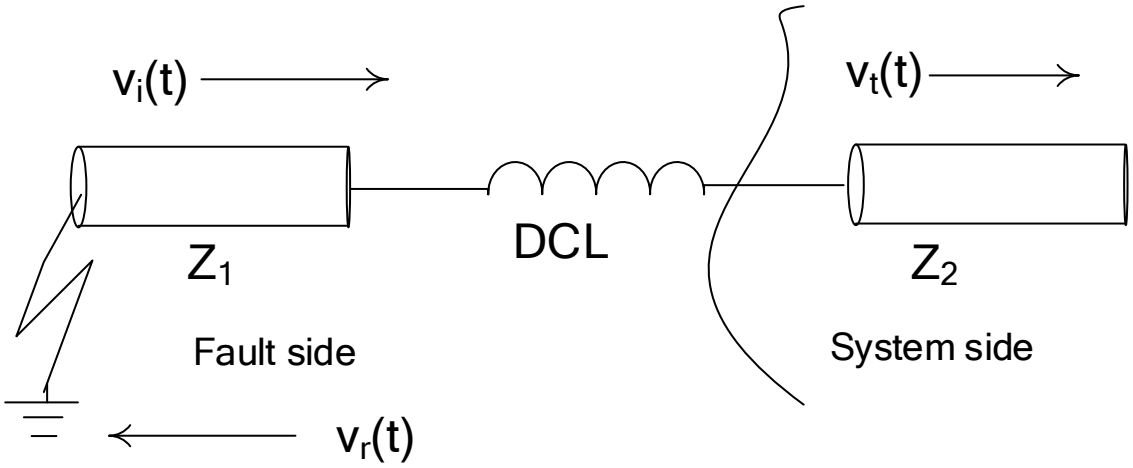

Figure 24: simplified diagram demonstarting the current limiting reactor in a system during fault

In order to visualize the impact of the size of the DC current limiting reactor, a simplified system of the two sides of the current limiting reactor is shown in Figure 24. As previously mentioned the negative travelling waves arise from the fault location and travel towards the system. Part of this negative wave is reflected and part of it is transmitted through the DC current limiting reactor (DCL). Assuming the negative travelling voltage wave as step function, the part of the wave that is transmitted through the inductor from the fault side to the system side is given by the following mathematical equation (after manipulation using Laplace transform),

$$v_t = v_i \left(\frac{2Z_2}{Z_1 + Z_2}\right).\left(1 - e^{-((Z_1+Z_2)/L)t}\right)$$

Where, Z_1 is the characteristic impedance of the faulted link, Z_2 is the impedance of the rest of the system seen at the DCL, L is the value of DCL and v_i is the incident wave. This equation shows that the larger the DC current limiting reactor is, the smaller the transmitted negative travelling voltage is. Since the transmitted voltage wave triggers the discharge of the submodule capacitors, the larger the magnitude of the transmitted waves, i.e. the smaller the value of the DCL, the higher the discharge of the submodule capacitors is.

Figure 25 depicts simulation results of the DC voltage V_{DC} (the pole-to-pole voltage) at C/S for each DCL value when a pole-to-pole fault occurs near B-C/S in Figure 22. The DCL value is set to 25 mH, 50 mH and 150 mH at each simulation. A DC fault is applied at time t= 300 ms. It can be seen from the simulation results of Figure 25 that the DC voltage starts to decrease when a fault occurs at DC line. HVDC CB is required to clear a DC fault rapidly in order to avoid the system voltage collapse. As the half-bridge MMC can maintain its AC current control until the DC voltage decreases to the lower threshold value during a DC fault occurrence, it is considered that system voltage collapse will not occur as far as the converter keeps above the threshold DC voltage value. The DC voltage value depends on a converter design parameter (e.g. modulation index) and the threshold DC voltage is generally designed within the range from 0.7 to 0.9 p.u. In this study threshold value of 0.8 p.u. is considered. Accordingly, the time from a fault occurrence until the DC voltage drops to 0.8 p.u. of rated DC voltage is defined as the maximum allowable fault neutralization time.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

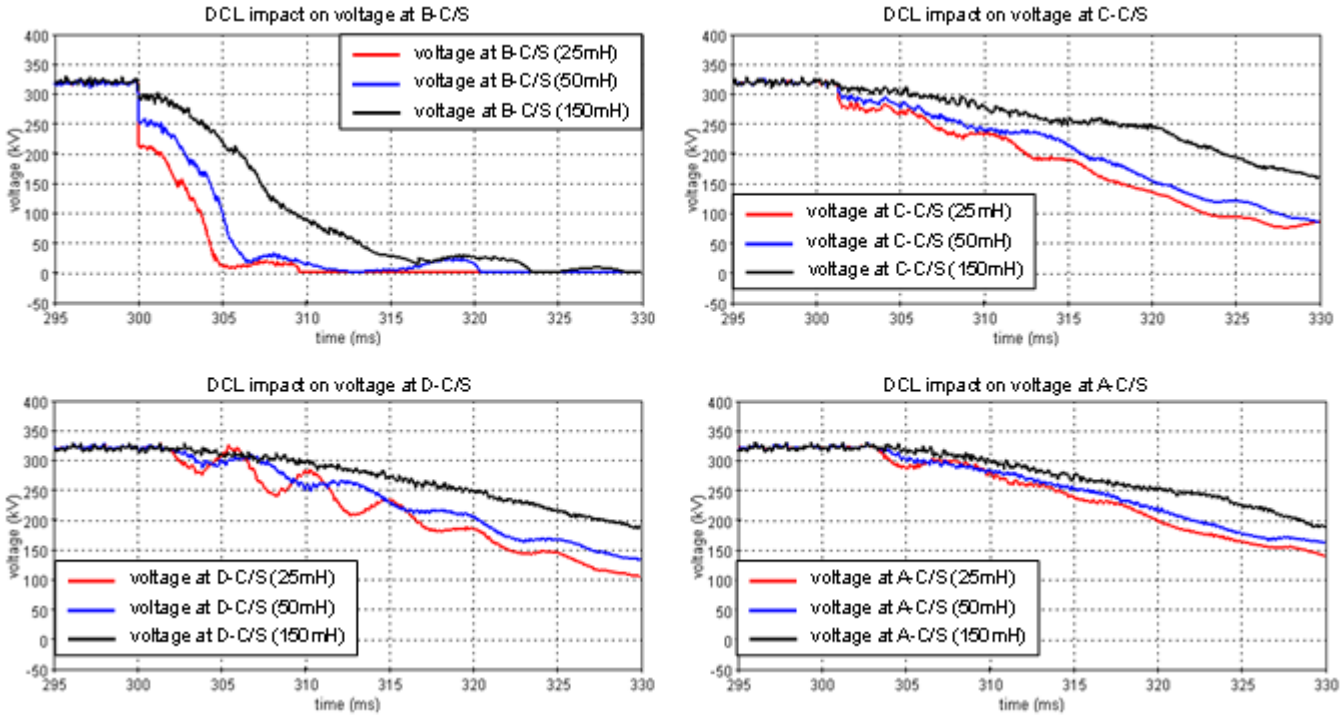

Figure 25: DC voltage behaviour in four-terminal radial HVDC network

The voltage at B-C/S near the fault immediately drops, where the line impedance and the value of DCL determine a rate of decay of voltage. The voltage at C-C/S, D-C/S and A-C/S, which are located 240 km to 600 km away from the fault location, gradually drops but the rate of decay of voltage is not as severe since the transmission line has significant impedance in addition to the DCL. Table 7 summarizes the results of the simulations showing the maximum times determined so that the converter DC voltage can continuously operate by keeping the voltage above 0.8 p.u. of the system voltage during a fault occurrence for different DCL values. Although the results do not indicate a perfect correlation between the speed of the voltage drop and distance from the fault due to transient oscillation and system parameter differences of each C/S (e.g. converter capacity), the DC voltage however tends to drop slowly with faults at farther distances from the converter station.

Table 7: The time until a voltage at each converter drops to 0.8 p.u. in a four-terminal radial HVDC network

DCL	B-C/S near	C-C/S 240 km away	D-C/S 360 km away	A-C/S 600 km away
25 mH	0.002 ms	6.52 ms	7.49 ms	12.91 ms
50 mH	0.002 ms	7.71 ms	9.86 ms	14.19 ms
150 mH	3.29 ms	13.88 ms	16.56 ms	18.00 ms

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

4.8 IMPACT OF DC LINE TYPE

Simulation studies in the preceding sections assume cable network only; however, the frequency of in OHL (Over Head Line) network is higher than that of cable network. In this section, fault current behaviour in OHL network is simulated. The lengths and configuration of the OHLs are the as four-terminal radial cable system in previous sections. The other system conditions are also same as in the previous sections.

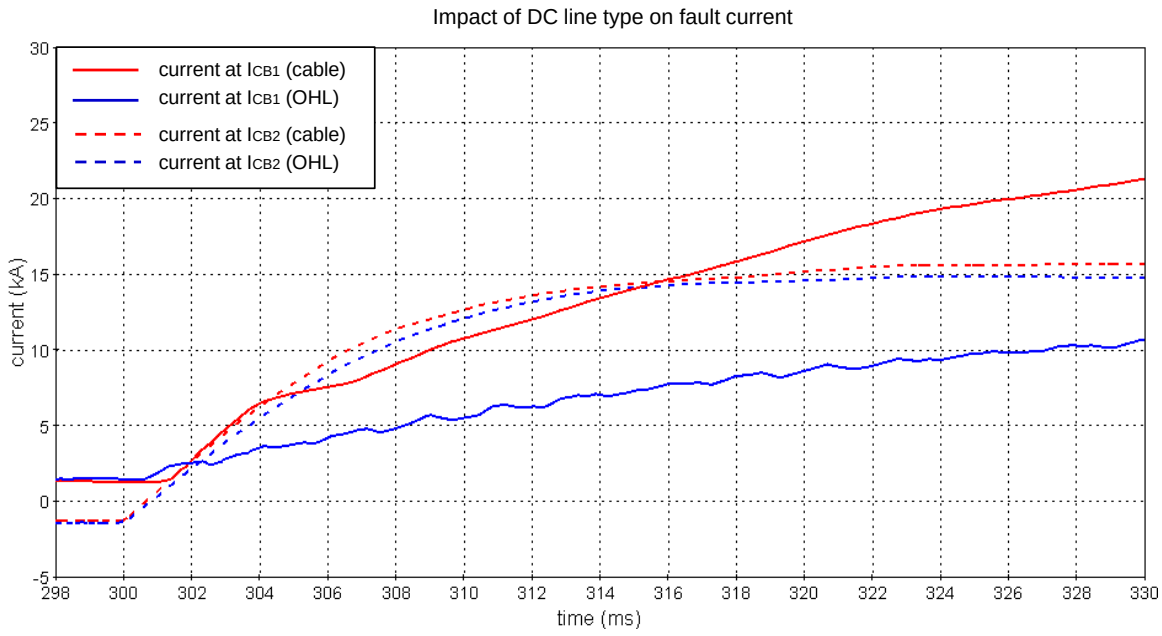

Figure 26: DC fault current behaviour for each DC line condition

Figure 26 shows fault current behaviour for each DC line type. When a fault occurs at remote side from HVDC CB (in the case of I_{CB1} Figure 26) fault current reduces dramatically. This is due to the higher impedance of OHL compared with cable. On the other hand, when fault occurs near HVDC CB (in case of I_{CB2} in Figure 26), the fault current behaviour does not change for each condition because there is no DC line between HVDC CB and fault point. Table 8 summarizes the DC fault current amplitude for each DC line type.

Table 8: DC fault current behaviour for each DC line condition at various times after fault

I_{CB_B1}(central node side)						
DC line type	5 ms (from the fault occurrence)	10 ms	20 ms	30 ms	40 ms	50 ms
Cable	7.13 kA	10.74 kA	17.14 kA	21.27 kA	24.22 kA	25.66 kA
OHL	3.71 kA	5.46 kA	8.63 kA	10.64 kA	11.49 kA	11.75 kA

I_{CB_B2}(converter side)						
DC line type	5 ms (from the fault occurrence)	10 ms	20 ms	30 ms	40 ms	50 ms
Cable	7.80 kA	12.65 kA	15.14 kA	15.67 kA	15.79 kA	15.64 kA
OHL	6.95 kA	12.06 kA	14.55 kA	14.75 kA	14.98 kA	14.84 kA

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

5 DISCUSSION

5.1 FAULT CONDITIONS

As discussed in Chapter 4, from the perspective of converter fault response it can be concluded that the transient phenomena following the occurrence of a fault can be split into two time intervals. The first part is the time until converter blocking and the second part is the time after converter blocking where the fault current is fed from the AC side through the freewheeling diodes associated with each IGBT.

The key factors determining the magnitude and the rate of rise of fault current are summarized in this Chapter. Although a fault occurring on a cable remotely from a converter station has high initial rate of rise of fault current, the faults occurring close to a converter terminal have the highest average rate of rise both before and after converter blocking. Thus, from now on the focus is on a fault closer to a converter terminal with a DC side reactor put at the ends of each cable. Consider a converter station having multiple connections as shown in Figure 27.

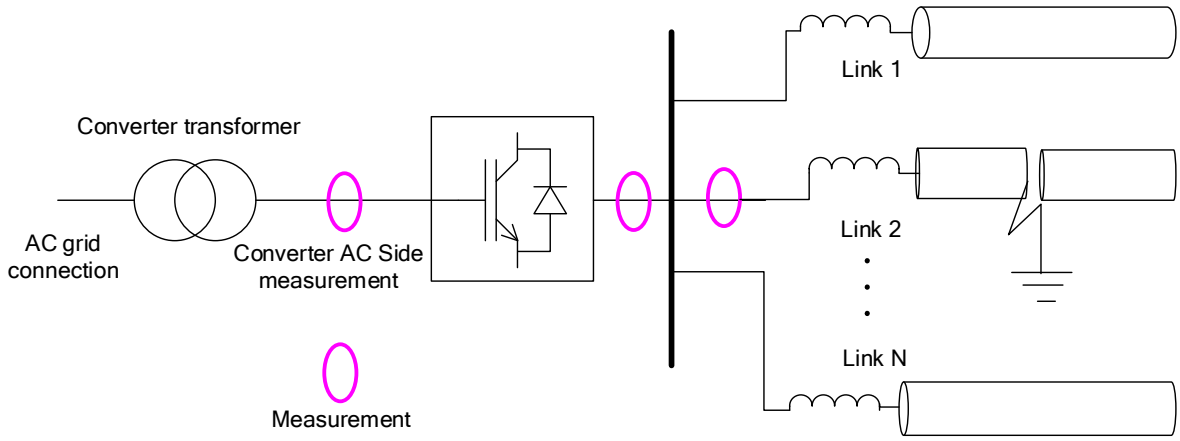

Figure 27: DC fault close to a converter terminal with multiple connections

The prospective fault current for a fault occurring close to a converter terminal is illustrated in Figure 28. Initially, a system is at steady state with the blue curve showing converter output current and the red curve showing current flowing to one of its connections (for example Link 2 in Figure 27). The difference between the two currents at steady state is due to the fact that the converter is also injecting power into the other adjacent connections. When a fault occurs at time t_1 close to this converter station on one of its connections, the converter current start rising at t_2 due to the voltage dip associated with the arrival of negative voltage wave originating from a fault location. At this time the converter is operating in its full control mode. The sizes of arm reactors as well as the DC side reactors put at the end of the faulted cable determine the rate of rise of current from the converter. The red curve shows the fault current measured at the input of the faulted link. Compared to the current measured at the output of the converter (blue curve), the current at the input of faulted cable rises at a slightly higher rate. This is due to the discharge of other cable links connected to the same DC bus. However, the discharge of these cables is

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

suppressed by the DC reactors at the ends of the corresponding cables. Another important point to see here is that the more connections terminate on the same DC bus, the larger the fault current.

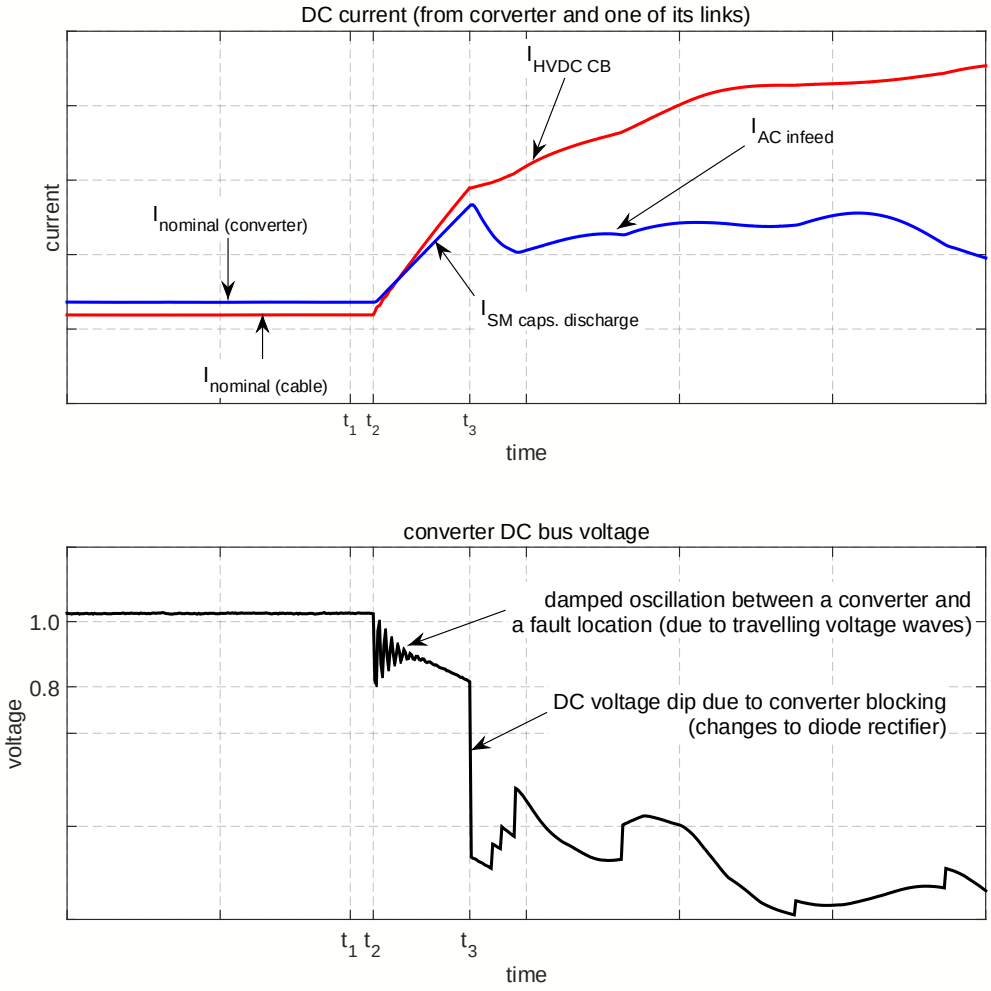

Figure 28: Summary of relationship between current through HVDC circuit breaker installed on a faulted cable and current from a converter station close to the fault (top graph) and the DC bus voltage during a fualt in multi-terminal network (bottom graph).

Nevertheless, the fault current is mainly dominated by the current coming from the converter which is caused by the discharge of submodule capacitors. In addition, the higher the power ratings of the converter close to the fault, the larger the size of submodule capacitors according to the minimum energy storage requirement per submodule described in Section 3.2.2.3. Thus, the discharge current from the submodule capacitors is also proportionally high. The discharge from the submodule capacitors continue until the threshold for blocking (either overcurrent or under-voltage threshold) is reached at t_3. At t_3 the converter blocks and as a result, the converter DC voltage is no longer controllable and is given by [52],

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

$$V_{dc,avr} = \frac{3\sqrt{2}V_{AC,l-l}}{\pi} - \frac{3}{\pi}X_{AC}I_{dc}$$

As can be seen from the above relationship, the average rectified DC voltage under load condition depends on the AC side impedance as well as DC side current. The larger the AC side impedance, the smaller the DC side rectified voltage and also the larger the rectified DC current the smaller the DC side rectified voltage (which is the case under fault condition).

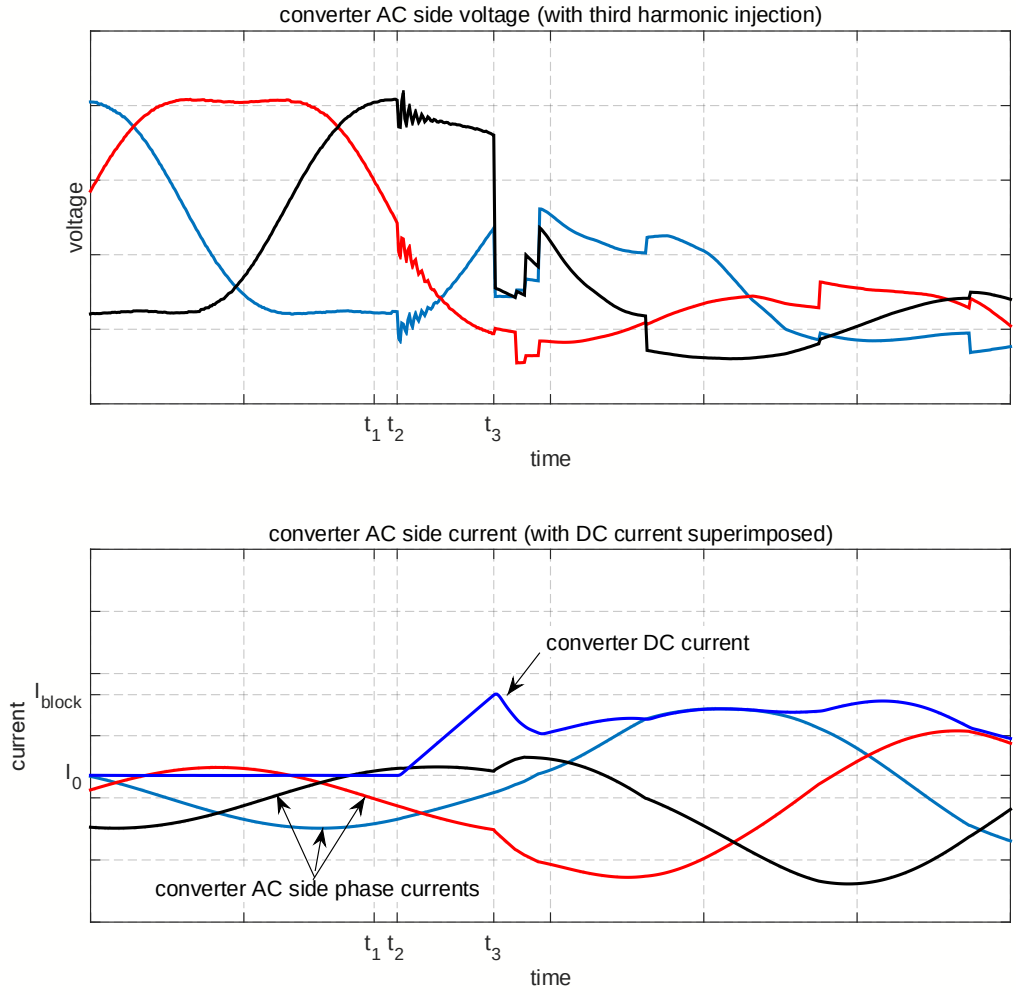

Figure 29: Converter AC side measurements before and after fault

After converter blocking at t_3 the discharge from the other links (healthy cables connected to the same DC node) and at a later stage the current contribution from the converters connected to the remote ends of these cables increase. Moreover, since half bridge submodules are used in the MMC, the AC side continues to feed current through the resulting six pulse rectifier after converter blocking (see Figure 28). Thus, the rate of rise of fault current and magnitude of fault current after converter blocking is dependent on the number of connections to the

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

same DC node, the magnitude of AC impedance of the nearby converter as well as the distance to the other converter stations from the fault.

Figure 29 shows measurements taken on AC side of a converter before and after fault. The top graph shows the AC voltage at the converter terminal and bottom graph shows converter AC current with converter DC current superimposed. The converter AC voltage has third harmonic injection (15 %), thus flattened peaks. As can be seen from this figure the converter AC side current and voltage are less affected (except small perturbations in the voltage that can be seen from top plot of Figure 29) until converter blocking.

The main conclusion from Figure 28 and Figure 29 is that time span between t_2 and t_3 dependent on the size of the DC reactor and can be optimized taking into account the speed of operation and maximum current breaking capability of the HVDC CB as well as fault ride through capability of the converter itself.

5.2 EQUIVALENT CIRCUITS

In general, during a fault condition two equivalent circuits (at different time intervals) can be identified; namely, the submodule capacitor discharge until converter blocking represented by Figure 30 and the simple diode rectifier bridge shown in Figure 31 during the AC infeed phase.

It must be noted that as long as a converter is operating in full control mode, the AC side current remain effectively unaffected until converter blocking. Thus, the contribution from the AC side during this time interval is negligible and the system can be represented by the equivalent diagram of Figure 30. At any time N_{arm} submodules are inserted and the capacitor balancing algorithm shuffles the submodules based on capacitor voltage to ensure equal discharge/recharge of all capacitors in each phase leg. Hence, each phase leg has two sets of N_{arm} submodules with equivalent capacitance of C_{eq}, which can be assumed as parallel connections. The three phases are normally connected in parallel as shown Figure 30 and therefore the total capacitance of the reduced equivalent system shown in the right side of Figure 30 is 6* $C_{eq.}$

$$C_{eq} = \frac{C_{SM}}{N_{SM,arm}}$$

$$R_{ON} = R_{arm} + R_{ON,IGBT/Diode} * N_{SM,arm}$$

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

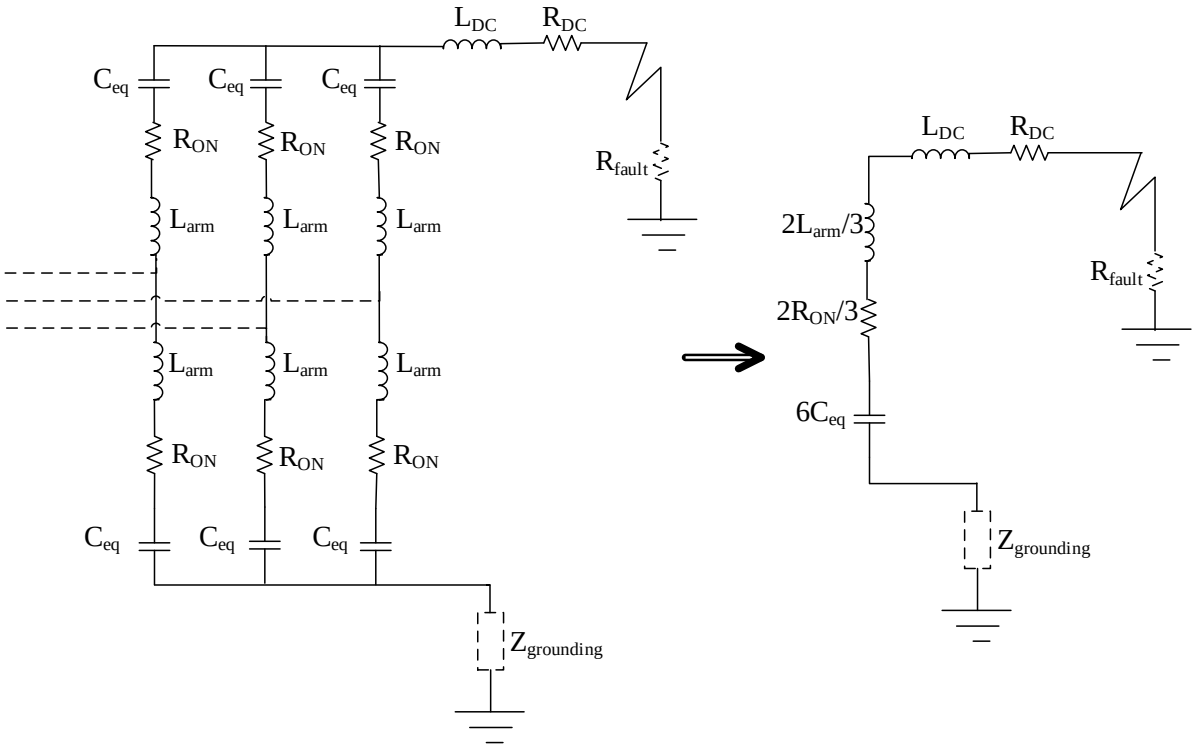

Figure 30: Equivalent circuit diagram of a system during fault until converter blocking (only submodule capacitor discharge)

As already mentioned in Chapter 4, a converter blocks either for the purpose of protecting its power electronic components against damage due to overcurrent from the discharge of the submodule capacitors and/or when it is no longer able to continue its controlled operation due to the resulting under-voltage following the discharge of the submodule capacitors. It is also shown that, the use of a DC current limiting reactor can limit the rate of discharge of these capacitors and thus can significantly delay converter blocking depending on the size of DC reactor used (the larger the DC reactor the longer delay). This has a strong implication on the protection system as well as the HVDC circuit breaker. In other words, depending on the speed of operation of a HVDC circuit breaker (and indeed assuming fast and reliable protection strategy) and the size of a DC reactor used, the DC fault might be cleared before converter thresholds for blocking are reached; thus, ensuring less disruption of the operation of the rest of the system.

The rate of rise of current from discharge of capacitors and the instantaneous value of the fault current can be obtained from the following expression.

$$i(t) = [(B\omega - \alpha A)\cos(\omega t) - (A\omega + B\alpha)\sin(\omega t)]e^{-\alpha t}$$

$$\frac{di(t)}{dt} = [B(\omega^2 + \alpha^2)\sin(\omega t) - A(\omega^2 - \alpha^2)\cos(\omega t)]e^{-\alpha t}$$

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

Where $\alpha = \frac{R}{2L}$, $\omega = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$, $R = R_{DC} + R_{fault} + \frac{2}{3}R_{ON}$, $L = \frac{2}{3}L_{arm} + L_{DC} + L_{cable/OHL}$, $C = 6C_{eq}$,

$$A = CV_{DC}$$

$$B = \frac{I_{DC} + A\alpha}{\omega}$$

The above equations are valid only for a discharge of a single converter until blocking.

However, once a converter blocks because of one of the reasons mentioned earlier, the system starts feeding the fault from AC side. The equivalent diagram of the system during this phase is shown in Figure 31.

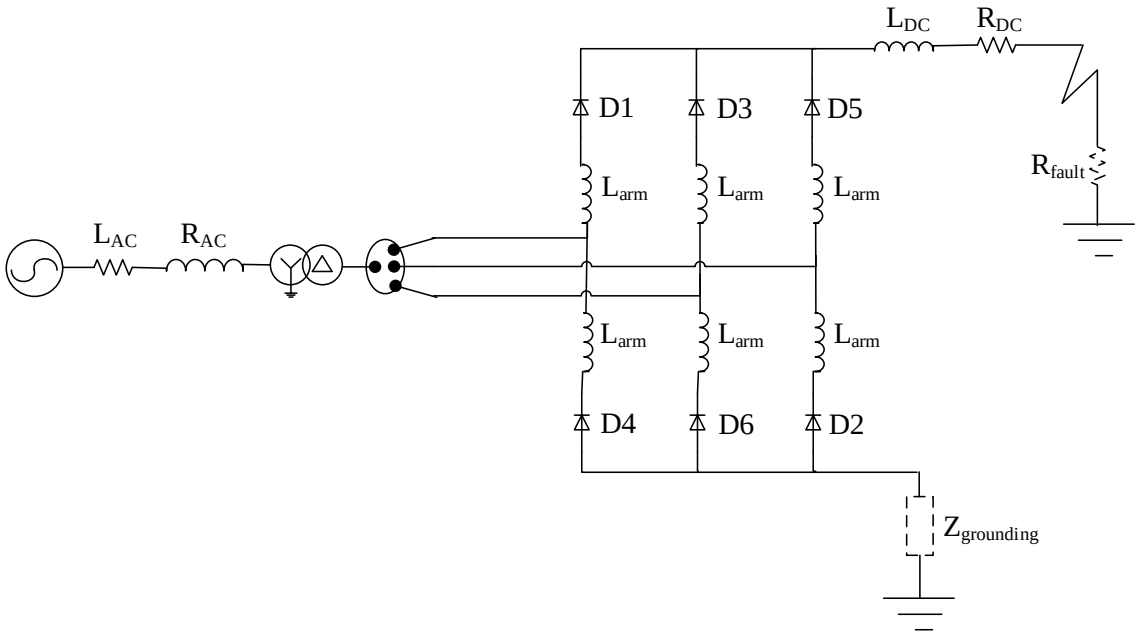

Figure 31: Equivalent circuit diagram of AC infeed through diode rectifier bridge after converter blocking

The average DC current coming from the AC side is determined by the total impedance between the AC source and the fault location which includes both AC and DC side impedances as shown by the following equation [37];

$$I_{AC,component} = \frac{\left(\frac{3}{\pi}\sqrt{2} \cdot V_{AC}\right)}{Z_{total}}$$

Where V_{AC} is the AC phase voltage on the transformer secondary side.

$$Z_{total} = Z_{AC} + Z_{tr} + \frac{1}{2}Z_{arm} + \frac{2}{3}\left(R_{DC} + R_{fault}\right)$$

Z_{AC} is the short AC circuit impedance of the system at the point of common coupling transferred to the secondary side of the transformer, Z_{tr} total impedance of converter transformer transferred to the secondary side and Z_{arm}

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

is the arm impedance consisting of inductance and resistance of arm reactor as well as total resistance of the N_{arm} series connected diodes.

The above mathematical expression provides the AC current infeed at steady state and hence DCL does not have an impact. Therefore, as discussed in Chapter 4 the AC current contribution is determined by not only the DC side parameters, but also mainly by the AC side parameters.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

6 CONCLUSIONS

Fault analysis has been carried out by means of PSCAD simulations on a multi-terminal HVDC benchmark study network fed by half bridge modular multi-level voltage source converters to study the various fault current contributions and their characteristics. The effects of network topology, series reactors, fault location, converter blocking logic, AC network strength and line type on the rate of rise and the magnitude of the fault current have been analysed qualitatively. Based on the results the following concluding remarks can be made:

C1 A fault is characterised by a breakdown of the insulation between one or more conductors of different voltages and/or ground. It results in a temporary conductive path between the conductor(s) and/or ground. A fault in any power cable, AC or DC, is characterized by a voltage transient which travels in both directions away from the fault location along the cable at the propagation speed of the cable. As the negative voltage transient travels through the HVDC system, it invokes, first, the discharge of any charged capacitances such as cables, filter capacitors and submodule capacitors resulting in a discharge current limited only by any series impedance in the cable. The sequence and timing of the discharges is determined by the distance of the capacitances from the fault and the speed of propagation of the voltage transient through the HVDC system. After the discharges of capacitive elements are over, the AC sources start feeding in the short-circuit current. The magnitude of the AC current infeed is determined by AC side impedances and DC side resistance.

C2 At impedance boundaries such as series components or busbars, a part of the negative voltage wave is transmitted and the rest is reflected, based on transmission line theory. At HB MMC VSC terminals, the arrival of a negative voltage transient triggers the discharge of the submodule capacitors leading to a (near linear) rise in current limited only by the converter arm reactor.

C3 In order to protect internal circuitry, an HB MMC VSC converter stops switching its power electronic switches i.e. it blocks, at which point the converter essentially turns into an uncontrolled diode rectifier. The decision to block is based on a logic combination combining arm and output overcurrent and DC under-voltage thresholds. Prior to blocking, the increasing DC output current of the converter has no impact on the AC current. Therefore, all energy is supplied by the submodule capacitors.

C4 The time it takes from the occurrence of a fault until a converter blocks depends on the converter rating, blocking logic and its electrical distance from the fault. Due to the different arrival times of the negative voltage transient at various points in the network, converters at different distances block at different times.

C5 After blocking, the DC output current of the converter is determined by the DC resistance between the fault, the converter (diode & reactor) resistance, the converter transformer impedance and the AC network strength.

C6 The insertion of series reactors at the ends of cables reduces/limits the rate of rise of fault currents. The higher the inductance of the reactor, the slower the rate of rise of current.

C7 Due to the insertion of series reactors, the time until converter blocking is increased and the converters are enabled to regulate their terminal voltage. The higher the inductance of the reactor, the smaller the voltage drop at the converter terminal before it blocks.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

C8 As long as a converter can regulate its output voltage (in the presence of series reactors), the discharge of adjacent feeders is very limited.

C9 The moment a converter blocks, the terminal voltage collapses and discharge of adjacent cables is induced

C10 Rate of rise of current in adjacent cables is suppressed twice (or more) because of two (or more) current limiting reactors in the fault current path.

C11 The rate of rise of fault current through a DC circuit breaker increases with increasing numbers of adjacent cables (or converter stations) being connected to its bus.

C12 After occurrence of the fault, the negative voltage transient travels to the end of the cable where a part of it is reflected back to the fault. At the fault a similar phenomenon happens but now the polarity of the transient changes so a somewhat attenuated positive voltage transient travels back to the cable end. This process of reflecting waves causes periodic voltage swings of both positive and negative polarity.

C13 Depending on the length of the cable and the location of the fault, the reflection of a positive voltage transient may increase the average voltage at the cable end and reduce the rate of rise of fault current. For this reason, a fault at the remote end of a long cable can result in a higher initial rate of rise of fault current than a close fault due to the long time it takes for the positive voltage wave to return.

C14 Due to the reactive nature of overhead lines, their presence in a DC network has a similar effect to that of a series reactor and decreases the rate of rise of fault current.

Finally, it is noted that these qualitative descriptions may be used to predict the worst case fault condition in a given HVDC network. The worst case conditions are always network specific and must under all circumstances be less severe than the maximum ratings of a DC circuit breaker. From the analysis, it follows that the value of the series reactor may be adjusted in order to change the stresses or demands placed on converter stations and/or prospective DC circuit breakers.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

7 BIBLIOGRAPHY

[1] J. Kreusel and D. Retzmann, “Integrated AC/DC Transmission Systems Benefits Of Power Electronics For Security And Sustainability Of Power Supply,” 2008.

[2] W. Breuer, V. Hartmann, D. Povh, D. Retzmann and E. Teltsch, “Application of HVDC for Large Power System Interconnections,” CIGRÉ, Session paper no. b4-106, 2004.

[3] C.-K. Kim, V. K. Sood, G.-S. Jang, S.-J. Lim and S.-J. Lee, HVDC Transmission: Power Conversion Applications in Power Systems, Wiley-IEEE Press, 2009.

[4] W. Breuer, D. Povh, D. Retzmann and E. Teltsch, “Trends for Future HVDC Applications,” in *16th Conference of the Electricity Power Supply Industry*, Mumbai, India, 2006.

[5] H. Pang, G. Tang and Z. He, “ Evaluation of losses in VSC-HVDC transmission system,” in *IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century*, 2008.

[6] A. Cavallini, D. Fabiani, G. Mazzanti and G. C. Montanari, “Life model based on space-charge quantities for HVDC polymeric cables subjected to voltage-polarity inversions,” *IEEE Transactions on Dielectrics and Electrical Insulation,* vol. 9, no. 4, pp. 514-523, 2002.

[7] A. Cavallini, D. Fabiani, G. Mazzanti, G. C. Montanari and L. Simoni, “Life estimation of DC insulation systems in the presence of voltage-polarity inversions,” in *Conference Record of the 2000 IEEE International Symposium on Electrical Insulation*, 2000.

[8] N. Flourentzou, V. G. Agelidis and G. D. Demetriades, “VSC-Based HVDC Power Transmission Systems: An Overview,” *IEEE Transactions on Power Electronics,* vol. 24, no. 3, pp. 592-602, 2009.

[9] J. Arrillaga, Y. Liu and N. Watson, Flexible Power Transmission: The HVDC Options, London, UK: John Wiley and Sons, 2007.

[10] U. Axelsson, A. Holm, C. Liljegren, M. Aberg, K. Eriksson and O. Tollerz, “The Gotland HVDC Light project-experiences from trial and commercial operation,” in *16th International Conference and Exhibition on (IEE Conf. Publ No. 482) Electricity Distribution, 2001. Part 1: Contributions. CIRED.* , 2001.

[11] Siemens AG, “BorWin 2,” SIEMENS, 2010.

[12] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors and T. Jonsson, “Vsc-hvdc transmission with cascaded two-level converters,” in *CIGRE session*, Paris, 2014.

[13] J. Glasdam, J. Hjerrild, Ł. H. Kocewiak and C. L. Bak, “Network fault tolerant voltage-source-converters for high-voltage applications,” in *Power System Technology (POWERCON), 2012 IEEE International Conference on*, 2012.

[14] H. Saad, J. Peralta, S. Dennetière, J. Mahseredjian, J. Jatskevich, J. A. Martinez, A. Davoudi, M. Saeedifard, V. Sood, X. Wang, J. Cano and A. Mehrizi-Sani, “Dynamic Averaged and Simplified Models for MMC-Based HVDC Transmission Systems,” *IEEE Transactions on Power Delivery,* vol. 28, no. 3, pp. 1723-1730, 2013.

[15] C. Oates and C. Davidson, “A comparison of two methods of estimating losses in the Modular Multi-Level Converter,” in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011.

[16] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes and F. Hassan, “The Alternate Arm Converter: A New Hybrid Multilevel Converter With DC-Fault Blocking Capability,” *IEEE Transactions on Power Delivery,* vol. 29, no. 1, pp. 310-317, 2014.

[17] H.-J. Knaak, “Modular multilevel converters and HVDC/FACTS: A success story,” in *Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011)*, 2011.

[18] G. Adam, R. Li, D. Holliday, S. Finney, L. Xu, B. Williams, R. Uda, K. Kuroda, R. Yamamoto and “. H. Ito, “Continued Operation of Multi-Terminal HVDC Networks Based on Modular Multilevel Converters,” Lund, May, 2015.

[19] S. Cui, S. Kim, J.-J. Jung and S.-K. Sul, “Principle, control and comparison of modular multilevel converters (MMCs) with DC short circuit fault ride-through capability,” in *IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014.

This project has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement No 691714.

[20] G. P. Adam, S. J. Finney, B. W. Williams, D. R. Trainer, C. D. M. Oates and D. R. Critchley, “Network fault tolerant voltage-source-converters for high-voltage applications,” in *9th IET International Conference on AC and DC Power Transmission, ACDC.* , 2010.

[21] D. V. Hertem, O. Gomis-Bellmunt and Jun Liang, HVDC Grids For Offshore and Supergrid of the Future, Wiley-IEEE Press, 2016.

[22] T. Magg, M. Manchen, E. Krige, J. Wasborg and J. Sundin, “Connecting networks with VSC HVDC in Africa: Caprivi Link interconnector,” in *Power Engineering Society Conference and Exposition in Africa (PowerAfrica)*, 2012.

[23] P. Kundur, Power System Stability and Control, McGraw-Hill, 1994.

[24] H. Rao, “Architecture of Nan'ao multi-terminal VSC-HVDC system and its multi-functional control,” *CSEE Journal of Power and Energy Systems, ,* vol. 1, no. 1, pp. 9-18, 2015.

[25] G. Tang, Z. He, H. Pang, X. Huang and X.-P. Zhang, “Basic topology and key devices of the five-terminal DC grid,” *CSEE Journal of Power and Energy Systems,* vol. 1, no. 2, pp. 22-35, 2015.

[26] F. Page, G. Adam, S. Finney, D. Holliday and L. Xu, “DC Fault Parameter Sensitivity Analysis,” in *12th IET International Conference on Developments in Power System Protection (DPSP 2014)*, Copenhagen, 2014.

[27] O. Gomis-Bellmunt, J. Liang, J. Ekanayake, R. King and N. Jenkins, “Topologies of multiterminal HVDC-VSC transmission for large offshore wind farms,” *Electric Power Systems Research,* vol. 81, no. 2, pp. 271-281, October 2010.

[28] M. K. Bucher, “Contribution of Fault Current Sources in Multiterminal HVDC Cable Networks,” *IEEE Transactions on Power Delivery,* vol. 28, no. 3, pp. 1796-1803, July 2013.

[29] E. Kontos, S. Rodrigues, R. T. Pinto and P. Bauer, “Optimization of limiting reactors design for DC fault protection of multi-terminal HVDC networks,” 2014.

[30] K. Tahata, S. Ka, S. Tokoyoda, K. Kamei, K. Kikuchi, D. Yoshida, Y. Kono, R. Yamamoto and H. Ito, “HVDC circuit breakers for HVDC grid applications,” in *CIGRÉ AORC Technical meeting*, Tokyo, Japan, 2014.

[31] B. Xiang, Z. Liu, Y. Geng and S. Yanabu, “DC Circuit Breaker Using Superconductor for Current Limiting,” *IEEE Transactions on Applied Superconductivity,* vol. 25, no. 2, 2015.

[32] J.-G. Lee, U. A. Khan, S.-W. Lim, W.-j. Shin, I.-J. Seo and B.-W. Lee, “Comparative study of superconducting fault current limiter both for LCC-HVDC and VSC-HVDC,” *Physica C: Superconductivity and its Applications,* vol. 518, pp. 149-153, 2015.

[33] Magnus Callavik; Anders Blomberg; Jürgen Häfner; Björn Jacobson, “The Hybrid HVDC Breaker An innovation breakthrough enabling reliable HVDC grids,” 2012. [Online]. Available: http://new.abb.com/docs/default-source/default-document-library/hybrid-hvdc-breaker---an-innovation-breakthrough-for-reliable-hvdc-gridsnov2012finmc20121210_clean.pdf?sfvrsn=2. [Accessed 21 September 2016].

[34] J. Häfner and B. Jacobson, “Proactive Hybrid HVDC Breakers - A key innovation for reliable HVDC grids,” in *CIGRÉ Symposium* , Bologna, Italy , Sep 2011.

[35] E. Kontos, R. T. Pinto, S. Rodrigues and P. Bauer, “Impact of HVDC Transmission System Topology on Multiterminal DC Network Faults,” *IEEE Transactions on Power Delivery,* vol. 30, no. 2, pp. 844 - 852, 2015.

[36] M. K. Bucher, R. Wiget, G. Andersson and C. M. Franck, “Multiterminal HVDC Networks—What is the Preferred Topology?,” *IEEE Transactions on Power Delivery,* vol. 29, no. 1, pp. 406-413, 2014.

[37] M. K. Bucher and C. M.Franck, “Contribution of Fault Current Sources in Multi-Terminal HVDC Cable Networks,” *IEEE Transaction on Power Delivery,* vol. 28, no. 3, pp. 1796-1803, 2013.

[38] M. Bucher and C. Franck, “Comparison of fault currents in multiterminal HVDC grids with different grounding schemes,” 2014.

[39] M. K. Bucher and C. M. Franck, “Fault Current Interruption in Multiterminal HVDC Networks,” *IEEE Transactions on Power Delivery,* vol. 31, no. 1, pp. 87-95, 2016.

[40] W. Leterme, N. Ahmed, J. Beerten, L. Angquist, D. V. Hertem and S. Norrga, “A new HVDC grid test system for HVDC grid dynamics and protection studies in EMT-type software,” in *11th IET International Conference on AC and DC Power Transmission*, Birmingham, 2015.

[41] M. Hadjikypris and V. Terzija, “Transient fault studies in a multi-terminal VSC-HVDC grid utilizing protection means through DC circuit breakers,” in *PowerTech (POWERTECH), 2013 IEEE Grenoble*, Grenoble, 2013.

This project has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement No 691714.

[42] CIGRE WG B4-57, Guide for the Development of Models for HVDC Converters in a HVDC Grid, CIGRE Technical Brochure 604, December 2014.

[43] S. Wenig, Y. Rink and T. Leibfried, “Multi-terminal HVDC control strategies applied to the Cigré B4 DC Grid Test System,” in *49th International Universities Power Engineering Conference (UPEC)*, 2014.

[44] Twenties Project, “DEMO 3 requirement specifications: detailed specifications for a DC network and detailed specifications for ALSTOM Grid's DC Breaker,” 2012.

[45] H. Saad, S. Dennetiére, J. Mahseredjian, T. Ould-Bachir and J.-P. David, “Simulation of Transients for VSC-HVDC Transmission Systems Based on Modular Multilevel Converters,” in *Transient Analysis of Power Systems:Solution Techniques, Tools and Applications*, Wiley-IEEE Press eBook Chapters, 2014, pp. 317-359.

[46] P. M. Meshram and V. B. Borghate, “A Simplified Nearest Level Control (NLC) Voltage Balancing Method for Modular Multilevel Converter (MMC),” *IEEE Transactions on Power Electronics,* pp. 450-462, 2015.

[47] MANITOBA HVDC RESEARCH CENTRE, “MyCentre,” 10 08 2016. [Online]. Available: https://hvdc.ca/knowledge-base/read,article/57/cigre-b4-57-working-group-developed-models/v:.

[48] F. B. Ajaei and R. Iravani, “Enhanced Equivalent Model of the Modular Multilevel Converter,” *IEEE Transactions on Power Delivery,* vol. 30, no. 2, pp. 666-673, 2015.

[49] D. Jovcic and K. Ahmed, High Voltage Direct Current Transmission: Converters, Systems and DC Grids, WILEY, September 2015.

[50] D. Jovcic, M. Taherbaneh, J. P. Taisne and S. Nguefeu, “Topology assessment for 3 + 3 terminal offshore DC grid considering DC fault management,” *IET Generation, Transmission & Distribution,* vol. 9, no. 3, pp. 221-230, 2015.

[51] CIGRE WG A3.28, “Switching phenomena for EHV and UHV equipment”,,” CIGRE Technical Brochure 570, Feb. 2014.

[52] N. Mohan, T. M. Undeland and W. P. Robbins, Power Electronics: Converters, Applications, and Design, John Wiley & Sons, Inc. , 2003.

This project has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement No 691714.

APPENDIX

A) SUBMODULE CAPACITORS AND ARM REACTORS SIZING

The basic structure of MMC is shown in Figure 3 of Chapter 2 along with the schematics of a half-bridge sub-module (HB-SM). It consists of N_{arm} number of submodules across each phase arm.

The sub-module capacitors are dimensioned based on the desired maximum voltage ripple. ±10 % is usually considered as acceptable and to achieve this, the energy stored per SM (E_{MMC}) should be in the range of 30-40 kJ/MVA [42]. Besides, capacitor-balancing algorithms are employed to keep the submodule capacitor voltage within acceptable range during operation. Thus, the sub-module capacitor sizes are obtained using the following expression;

$$C_{SM} = \frac{2\, S_{base} E_{MMC}}{6 N_{arm} {v_c}^2}$$

Where, $v_c = \frac{V_{DC}}{N_{arm}}$

The arm inductance can be optimized for various purposes; however, in this case it is determined from system base impedance as;

$$L_{arm} = 0.15 * \frac{Z_{base}}{\omega_{base}}$$

Where $Z_{base} = \frac{{v_{base}}^2}{S_{base}}$, S_{base} is the converter power rating, v_{base} transformer secondary voltage, $\omega_{base} = 2\pi f$

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

B) CONVERTER BLOCKING LOGIC FLOW DIAGRAM

The converter blocks based on local current and/or voltage measurements at its output. In the case considered in this report, the converter blocks when the DC current reaches 6 kA and/or the DC voltage of a converter falls below 75% of the nominal value. However, in order to ensure that it is not a measurement error, fault pickup time of 50 µs is assumed so that if the current and/or voltage measurement still exceeds the threshold values, the blocking signal is triggered. Also the IGBTs take 20 µs to block the current and this is taken as IGBT blocking delay in the model.

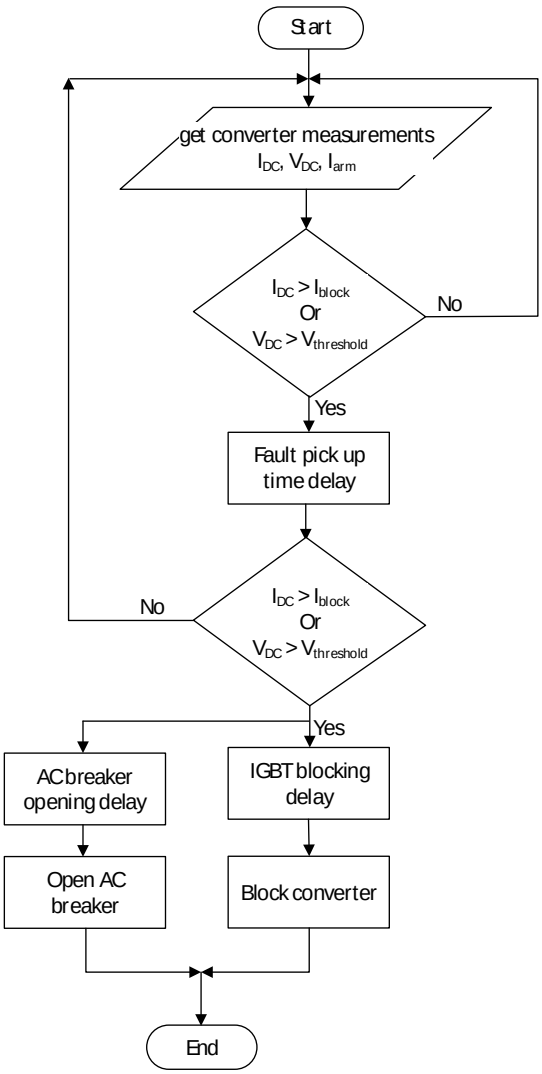

Figure 32: Converter blocking logic flow chart

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

C) GENERAL BLOCK DIAGRAM OF VSC MMC CONTROL SYSTEMS

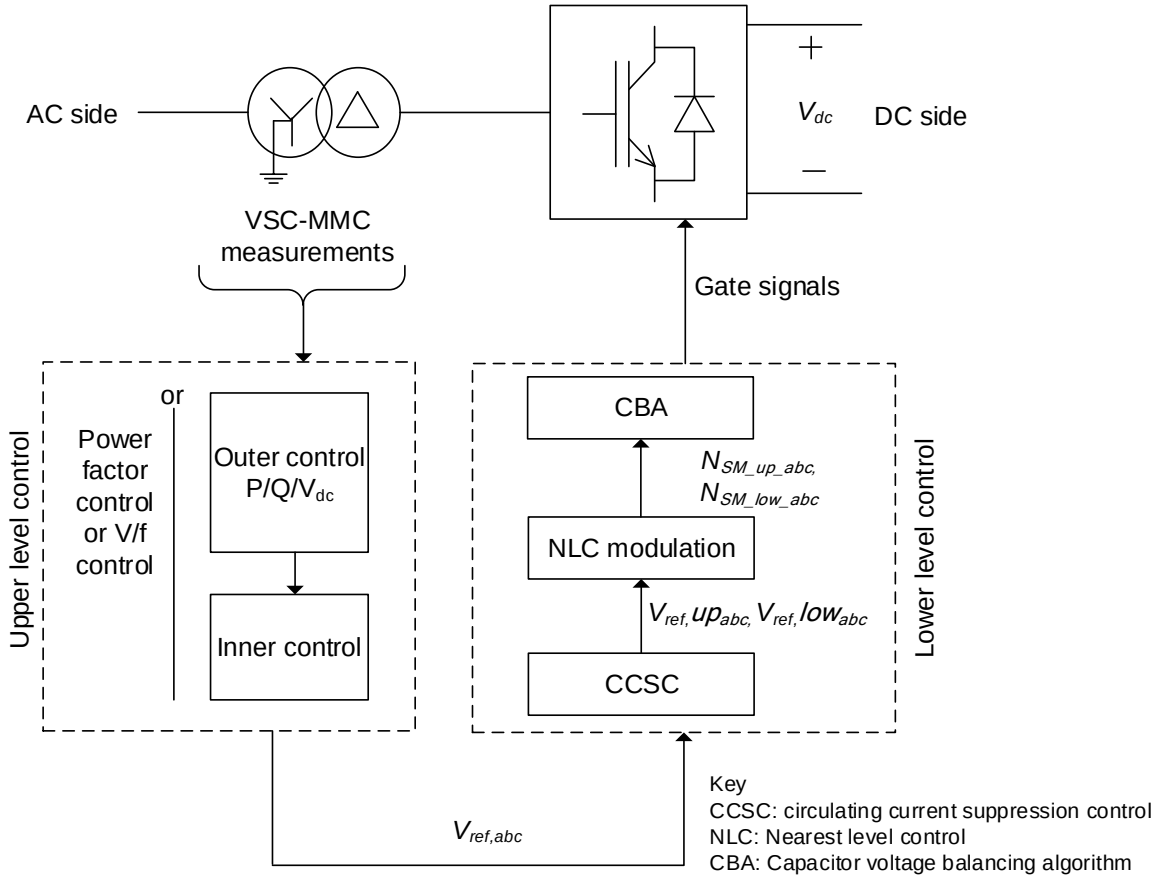

Figure 33: General description of control hierarchy for VSC MMC converter station [42]

A detailed control diagrams of each block in Figure 33 are available in PROMOTioN D2.1, “Grid Topology and Model Specification”.

This project has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement No 691714.