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PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

D5.3 Fault Stress Analysis of HVDC Circuit Breakers

PROMOTioN – Progress on Meshed HVDC Offshore Transmission Networks
Mail info@promotion-offshore.net
Web www.promotion-offshore.net

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CONTACT

DOCUMENT INFO SHEET

Document Name: Fault Stress Analysis of HVDC Circuit Breakers
Responsible partner: DNV GL
Work Package: WP 5
Work Package leader: Cornelis Plet
Task: 5.3
Task lead: Nadew Adisu Belda

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APPROVALS

	Name	Company
Validated by:	Alexander Broy	SIEMENS
	Dragan Jovjic	University of Aberdeen
Task leader:	Nadew Adisu Belda	DNV GL
WP Leader:	Cornelis Plet	DNV GL

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LIST OF CONTRIBUTORS

Work Package and deliverable involve a large number of partners and contributors. The names of the partners, who contributed to the present deliverable, are presented in the following table.

PARTNER	NAME
DNV GL	Nadew Adisu Belda
DNV GL	Cornelis Plet
DNV GL	René Smeets
MEU	Claudia Spallarossa
MELCO	Tahata Kazuyori, Fredrick Page

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CONTENT

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EXECUTIVE SUMMARY

In order to realize multi-terminal, meshed HVDC networks (MTDC), considerable research and development, both on component as well as system level, is underway. Before putting these research results into practical applications, appropriate testing of these developments is crucial. Hence, to accelerate the realization of the envisaged MTDC networks, test facilities sufficiently representing a practical DC system under various conditions need to be designed and developed.

One of the essential building blocks of the future multi-terminal HVDC grids, currently drawing significant research interest, is the HVDC circuit breaker. So far there are no clearly specified and quantified requirements of HVDC circuit breakers let alone a standardized method to test these devices. The main objective in this report is, therefore, to gain sufficient insight into the requirements for HVDC circuit breakers by embedding their simulation models in a multi-terminal HVDC study grid. The stresses observed on the models of the circuit breakers during current interruption under various conditions are used as guide to design proper test circuits for practical HVDC circuit breakers in a high-power laboratory.

The detailed operation principle of three different technologies of HVDC circuit breakers; namely, active current injection HVDC circuit breaker and two types of hybrid power electronic HVDC circuit breakers are illustrated first. Then the models of these circuit breakers are inserted in the benchmark study grid defined in deliverable D5.1 and simulation results are analyzed in detail.

For all the HVDC circuit breakers considered in this report, it is necessary to have a series DC current limiting reactor. However, assuming fast enough protection system, the size of the reactor used along with each circuit breaker technology depends mainly on the operation time (the time from trip order until the circuit breaker can withstand a transient interruption voltage (TIV)) of the circuit breaker. In general, the DC current limiting reactor is chosen to,

- Limit the magnitude of the fault current occurring in the protection zone of the circuit breaker to within the interruption capability of the circuit breaker during fault current neutralization time.
- Ensure continued controlled operation of the healthy part of the system by avoiding the voltage collapse of the entire DC grid during the fault neutralization time. In doing so the series DC current limiting reactor also provides more time for the protection system to detect and locate the fault.

Accordingly, 150 mH DC reactor is used in series with the active current injection HVDC circuit breaker and a breaker operation time of 8 ms is assumed. A peak current of about 12 kA is interrupted and an amount of energy of about 25 MJ is absorbed by the breaker. In this case the converters at the ends of the faulted cable block as either of these converters cannot continue its controlled operation during relatively longer fault neutralization time. It must be noted that the maximum interrupted current and the corresponding energy absorbed by a circuit breaker are highly dependent of the system architecture and associated parameters.

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For the hybrid HVDC circuit breakers, a breaker operation time of 2 ms is assumed. Due to the shorter breaker operation time, a 100 mH DC current limiting reactor is used in series with the hybrid HVDC circuit breakers. Hence, a peak current of about 8.5 kA is interrupted and an amount of energy of circa 10 MJ is absorbed by hybrid circuit breakers. With the assumed relay time, the fault can be cleared before any of the converters in the system block.

For all the circuit breakers, it is observed that the system voltage starts to recover even before the fault current is completely cleared. Thus, from the system perspective, the most important phase of the current interruption process is, therefore, the fault neutralization time. However, this poses an additional burden to the HVDC circuit breaker as it must dissipate more energy including the electrical energy supplied by the system due to the recovered system voltage.

In general, to stress the HVDC circuit breakers as in service, a test circuit should provide sufficient current, voltage and energy. The specific details are mainly dependent on the system under consideration. However, the most important parameters which must be tested are;

1. Capability to create a local current zero without restrike/breakdown of mechanical switches/interrupters or thermal overload of power electronic components at rated DC fault current
2. Generation of sufficient counter voltage to initiate fault current suppression
3. Capability of energy absorption components to absorb energy during fault current suppression wave trace as in service. Depending on the rated test sequence, this capability must be demonstrated several times within a defined sequence.
4. Capability to withstand the rated DC voltage after the current interruption process
5. The breaker operation time: the minimum time at which the circuit breaker reaches the TIV withstand level after trip order
6. The maximum current interruption: The maximum current the breaker can interrupt within the breaker operation time
7. The maximum energy that the circuit breaker can absorb
8. The number and frequency of operation: the number of interruption operations that the circuit breaker can perform before thermal run away occurs in its surge arresters. The interruption interval needs to be defined, e.g. like auto reclosure in AC circuit breakers

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NOMENCLATURE

ABBREVIATION	EXPLANATION
AC	Alternating Current
CB	Circuit Breaker
DCCB	Direct Current Circuit Breaker
DCL	DC Current Limiting Reactor
FB	Full Bridge
HB	Half Bridge
HVAC	High voltage AC
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
ITIV	Initial Transient Interruption Voltage
LCC	Line Commutated Converter
MMC	Modular Multi-Level Converter
MTDC	Multi-Terminal HVDC
NLC	Nearest Level Control
OHL	Overhead Line
PCC	Point of Common Coupling
TIV	Transient Interruption Voltage
VSC	Voltage Sourced Converter
WP	Work Package

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1 INTRODUCTION

In order to realize multi-terminal, meshed HVDC networks (MTDC), considerable research and development, both on component as well as system level, is underway. Before putting these research results into practical applications, appropriate testing of these developments is crucial. Hence, to accelerate the realization of the envisaged MTDC networks, test facilities sufficiently representing a practical DC system under various conditions need to be designed and developed.

One of the essential building blocks of the future multi-terminal HVDC grids, currently drawing significant research interest, is the HVDC circuit breaker. At present, a few industrial concepts of HVDC circuit breakers have been proposed. However, the practicality of these concepts remains to be proven. Lack of practical experience related to the operation of MTDC networks under various conditions makes proper characterization of the expected fault conditions which these breakers are exposed to even more difficult.

So far there are no clearly specified and quantified requirements of HVDC circuit breakers, let alone a standardized method to test these devices. The main objective in this report is, therefore, to gain sufficient insight into the requirements of HVDC circuit breakers by embedding their simulation models in a multi-terminal HVDC study grid. The stresses observed on the models of the circuit breakers during current interruption under various conditions are used as guide to design proper test circuit for practical HVDC circuit breakers in a high-power laboratory.

1.1 MOTIVATION

To date no HVDC circuit breakers have been applied in real HVDC systems. Due to the absence of practical experience with such devices, discussions about their implementation mostly remain an academic affair, and are not part of network strategists' vocabulary. As a result, the state-of-development, abilities and limitations of HVDC circuit breakers and the impact of their operation on an HVDC network, both adverse and beneficially, are not well understood by their prospective end-users. This uncertainty, along with economic considerations, impedes the uptake of HVDC circuit breakers and thus, in part, prevents the realisation of meshed multi-terminal networks.

By independently and publicly demonstrating the performance and operation of the proposed HVDC circuit breaker technologies through full-power testing, risk associated with the viability of the technologies is effectively reduced. The results of such tests can be used to independently validate academic studies and thus serve as a starting point for the dialogue between manufacturers and end-users to formulate requirements for this type of device.

Hence, to formulate the test requirements of HVDC circuit breakers it is necessary to investigate the transients to which these devices are subjected during fault condition in a multi-terminal grid. To this end, this report

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focuses on identifying the important stresses, which should be replicated in the test circuit, from simulation study.

1.2 DOCUMENT OVERVIEW

The remainder of the report is organized as follows. In chapter 2, general background of DC current interruption is provided along with wave trace and timing definitions. The detailed operation principle of three different technologies of HVDC circuit breaker is provided. In Chapter 3 simulation results obtained by embedding the models of HVDC circuit breakers are presented in detail. The impacts of fault location and thus, travelling waves are qualitatively described. Chapter 4 provides discussion regarding test requirements and in Chapter 5 conclusions based on the results obtained in the report are provided.

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2 HVDC CIRCUIT BREAKERS AND MODELS USED FOR SYSTEM SIMULATION

2.1 BACKGROUND OF DC CURRENT INTERRUPTION

Several DC side fault conditions in HVDC grid have been simulated in deliverable D5.1 [1]. It was observed that the main characteristics of a fault in a HVDC grid is that the fault current rises rapidly to a high steady state DC current. This poses several challenges that need to be addressed by HVDC circuit breaker. These are:

1. It has no current zero which means an interrupting device must be equipped with a mechanism to create a current zero crossing.
2. In AC, the system contains no stored magnetic energy at each zero crossing. In DC systems in contrast, because of the absence of a current zero crossing, a HVDC circuit breaker has the additional duty of dissipating the magnetic energy in the system.
3. The breaker must produce a voltage higher than the system voltage. In doing so it must be able to reach dielectric withstand of such a high voltage within a few milliseconds. This must be considered in the insulation coordination of the system in which the circuit breaker is to be installed.
4. The circuit breaker must act fast, otherwise, the fault current rises to a value that exceeds the interrupting capability beyond which a breaker will not be able to clear and damage to system components could be inflicted.

To address these requirements/challenges, a HVDC circuit breaker typically consists of several current branches (see Figure 2-1) through which the (fault) current is guided in a pre-determined sequence during an opening or closing operation. The function of each branch is briefly described below.

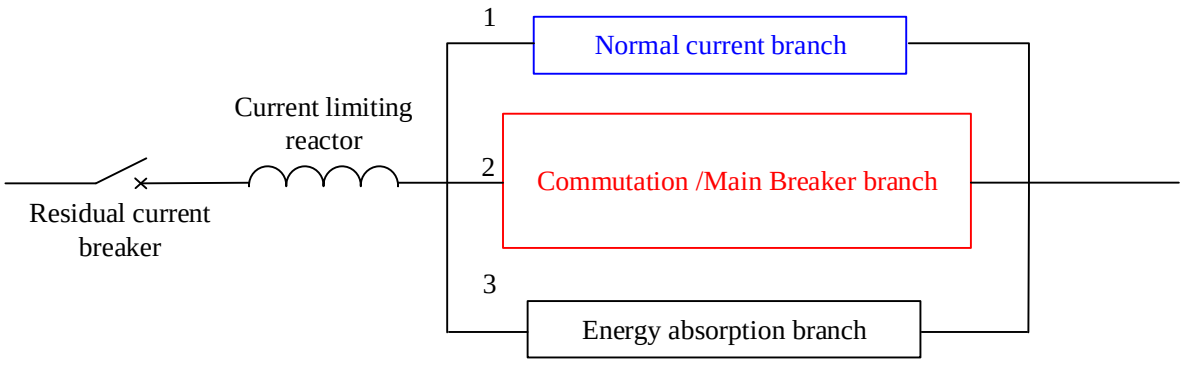

Figure 2-1: Generic model of HVDC Circuit Breaker

1. **Normal current branch**: this is a low loss path through which current flows during normal operation.

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2. **Commutation / Main breaker branch:** depending on circuit breaker technology this is a branch to inject counter current or a branch (one or more) that diverts current from the normal branch during fault current interruption and that finally commutates it into the energy absorption branch.
3. **Energy absorption branch:** this is a branch in which counter voltage is generated and the magnetic energy stored in the system inductance is absorbed.

Depending on the components used in each of the branches, several HVDC circuit breaker concepts have been proposed as discussed in the following sections. Only the major categories are considered in this report.

2.2 TIMING DEFNITIONS AND ASSUMPTIONS FOR CIRCUIT BREAKER OPERATION

Although the actual operation of various HVDC circuit breaker technologies varies, the general interruption process is similar, creating a counter-voltage that exceeds the system voltage. As such, it is possible to define a common terminology regarding the operational modes and timings. CIGRÉ JWG A3/B4.34 developed Figure 2-3 which shows voltage and current waveform terminologies and timing definitions related to fault current interruption by a generic HVDC circuit breaker.

Since fault current interruption involves the disciplines of circuit breaker design, protection system design, and power system studies, the definitions are classed into three categories, namely breaker related, protection related and system related (see Figure 2-3). In this section the most important definitions and associated assumptions are described.

i. Waveform definitions

1. **Prospective fault current:** The fault current that results at circuit breaker location when no action to clear the fault is made.
2. **Peak fault current:** the maximum value of the fault current that flows through the circuit breaker during fault current interruption. The peak fault current occurs the moment TIV equals the system voltage.
3. **Transient interruption voltage (TIV):** The voltage that a circuit breaker develops (appears across the circuit breaker terminals) during DC current interruption. This is the voltage across the breaker during the interruption process, imposed by the DC breaker (in particular, the surge arrester). This in contrast to the TRV in AC circuit breakers, which occurs after current zero and is imposed by the system (see Figure 2-2).

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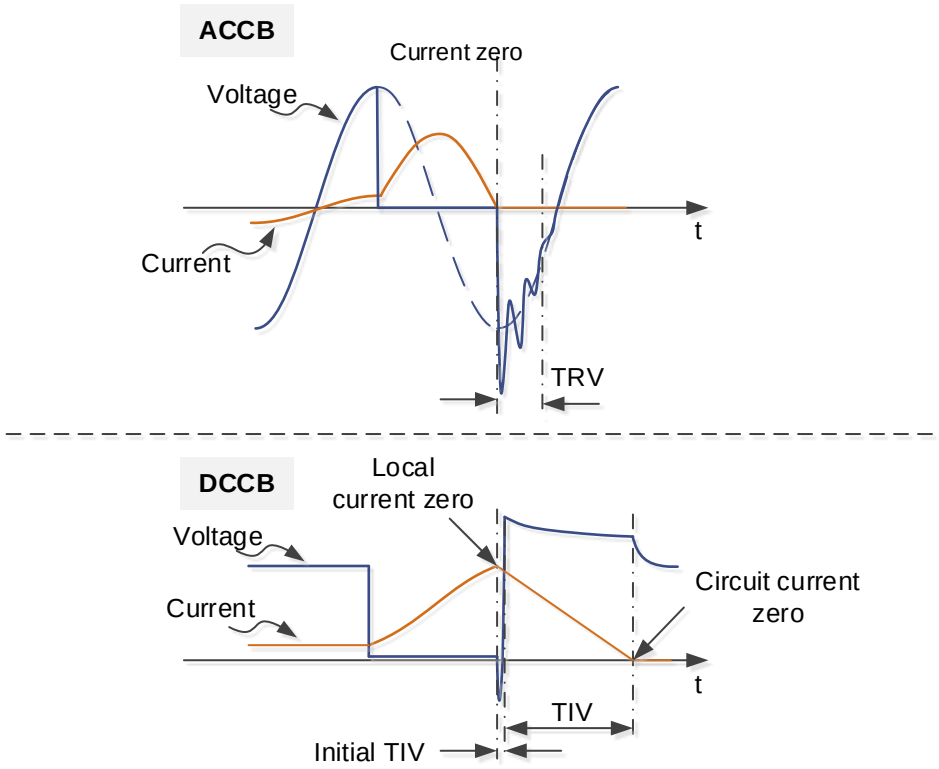

Figure 2-2: Comparison of TRV in AC circuit breakers and TIV in DC circuit breakers

4. **Leakage (residual) current**: the current that flows through the surge arrester after fault current interruption.

ii. Timing definitions

1. **Relay time**: the time from fault inception until a fault is detected and its location is identified. In this study relay time is assumed to be in the range of 1-2 ms.
2. **Breaker operation time:** is the time required by a circuit breaker from trip order until it attains a TIV withstand level.
3. **Internal current commutation time**: the time required by the breaker to commutate current to its energy absorption branch. In other words, the time from trip order up to the time when the peak TIV is reached.
4. **Fault neutralization time**: the time from fault inception until the peak TIV is reached: (relay time + internal current commutation time)
5. **Fault current suppression time (energy dissipation time):** the time required to bring the fault current from its peak value to zero or residual current. During this time the system voltage is restored, though the fault current persists.
6. **Break time:** time from trip order until fault current is reduced to the residual current
7. **Interruption time:** the total time from fault inception until fault clearing

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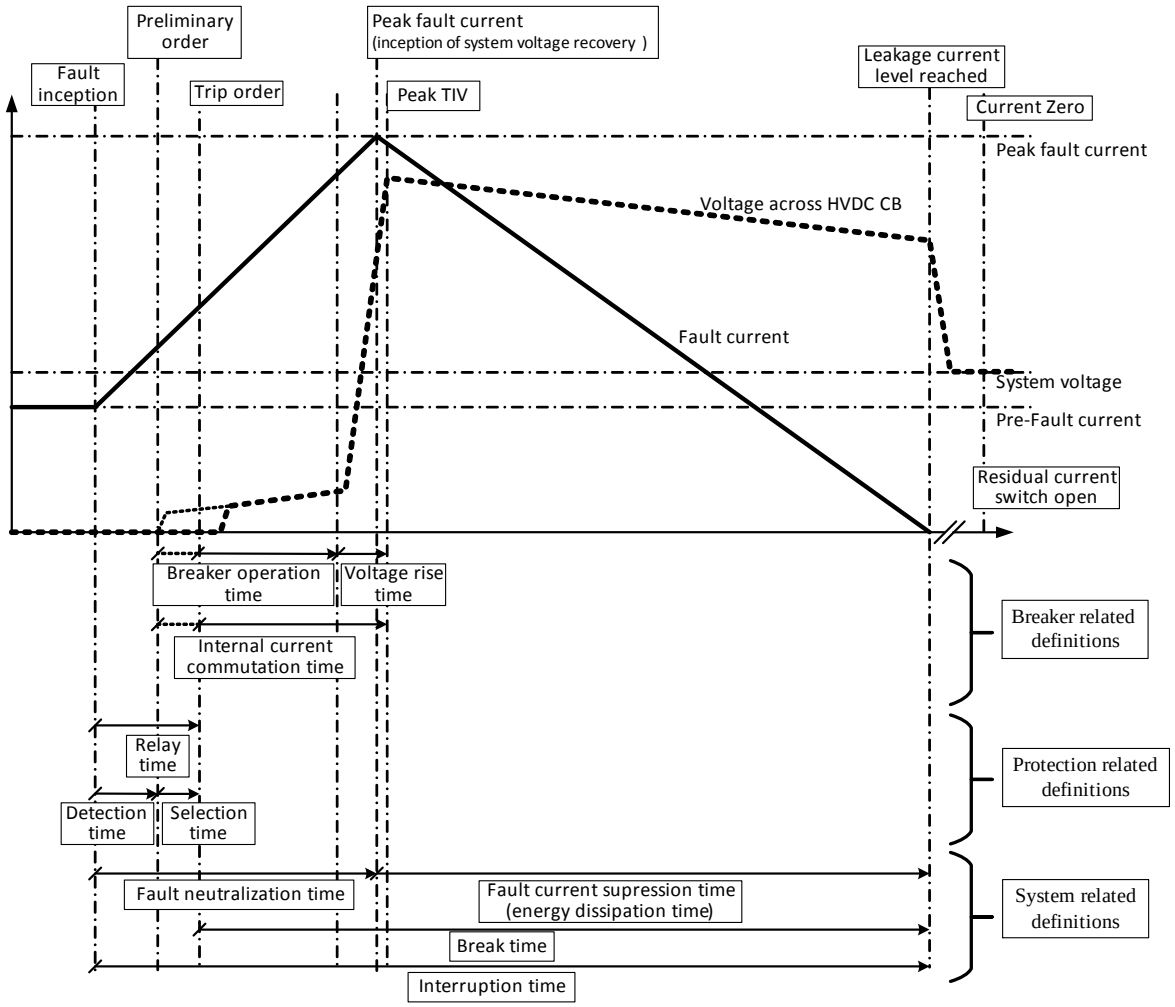

Figure 2-3: Timing definitions and wavetrace terminologies [2]

Until the *trip order*, the system fault current flows through the **normal current branch**. Upon receiving the trip order, the circuit breaker will start interruption by opening the normal current branch and activating the **Commutation / Main breaker branch(s)**. Once the normal current branch achieves voltage withstand level, the system fault current is commutated from the **Commutation / Main breaker branch** into the energy absorption branch during the *voltage* ***rise time*** in which the voltage across the breaker rises until the surge arrester conduction voltage is reached. The *breaker operation time* and the *voltage rise time* combined constitute the *internal current commutation time*. During ***fault current suppression time***, both the normal current and the commutation branches are fully opened and the fault current flows through the **energy absorption branch**. The surge arrestor imposes a counter voltage across the circuit breaker which leads to a negative di/dt until the fault current is suppressed to a small **leakage (residual) current**. The latter is interrupted by the residual current breaker.

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2.3 HVDC CIRCUIT BREAKER TECHNOLOGIES AND MODELS

The HVDC circuit breaker concepts that have been proposed in the technical literature can generally be categorized into four different basic topologies, as shown in Figure 2-4 [2]. In each topology, the energy absorption path is implemented as a (metal oxide) surge arrester (MOSA). The topologies are distinguished by different combinations of mechanical interrupters, power electronic switches (IGBTs, thyristors, GTOs) and passive components (inductors, capacitors and resistors) in the nominal current, Commutation/Main breaker branches.

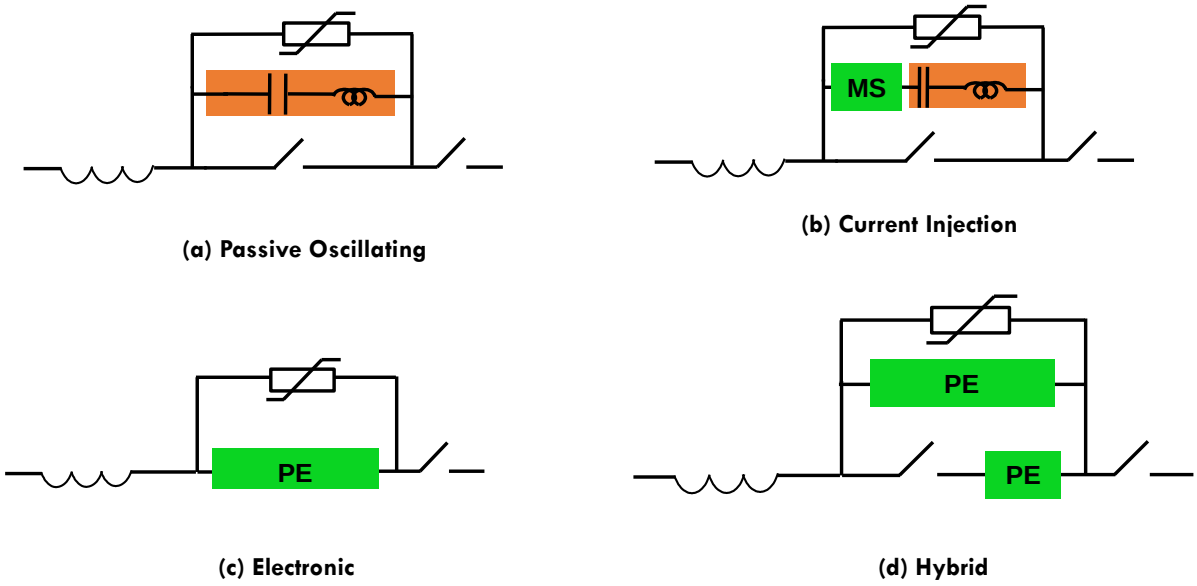

Figure 2-4 – Generalised HVDC circuit breaker topologies (PE = Power Electronics) [2]

In terms of performance, the topologies are distinguished by the internal current commutation time, maximum current interruption capability, maximum di/dt, cost, nominal losses, dimensions and weight, re-closing capability, etc. By combining elements of the passive oscillating and electronic topologies, current injection and hybrid topologies are formed which achieve a favourable compromise between any of the performance characteristics.

The circuit breaker topologies that rely on mechanical interrupters are typically limited in voltage rating to approximately 100 kV. To achieve the desired HVDC voltage rating, a series connection of modules must be made. In this section, only the major types HVDC circuit breakers which have been developed into prototypes and tested are considered.

Note that in this report branches and paths mean the same thing and are used interchangeably.

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2.3.1 ACTIVE CURRENT INJECTION HVDC CIRUIT BREAKER

The electrical design of active current injection HVDC circuit breaker is shown in Figure 2-5 adapted from [3]. It consists of a mechanical interrupter in parallel with a series connection of an inductor and a charged capacitor. In parallel with a charged capacitor is a metal oxide surge arrester bank for limiting the peak TIV and energy absorption.

Under normal operation, current flows through the mechanical interrupter unit, usually consisting of one or more fast vacuum interrupter(s), as shown in Path1 of Figure 2-5. The generic sequences of operation and the resulting waveforms of the DC fault current interruption process using the active current injection HVDC circuit breaker are illustrated in Figure 2-6. An ideal DC source is used for illustration purpose. When a fault is detected, a trip signal is sent to the CB, and the mechanical interrupter starts to open at t_2, resulting in arc current between its contacts. The entire fault current flows through the arc path during the interval from t_2–t_3. After the contacts of the mechanical interrupter have reached a certain minimum separation, the making switch in the Commutation path (L-C branch in Path2) closes (at t_3). This results in a discharge of the pre-charged capacitor. Due to the inductor in this path, an oscillating current is superimposed onto the arcing fault current through the mechanical interrupter, thus creating zero crossing(s) for extinguishing the arc. In Figure 2-6 the mechanical interrupter extinguishes the arc at the first zero crossing and hence, no oscillation can be seen. After the arc is extinguished, current commutates to Path2 and re-charges the capacitor (from t_3–t_4). Thus, the transient interruption voltage (TIV), equivalent to transient recovery voltage (TRV) in AC circuit breakers, builds up ultimately reaching the protective voltage of the surge arrester. From this moment on, the fault current commutates to the surge arrester in Path3. Finally, during the period from t_4–t_5, the surge arrester absorbs the magnetic energy stored in the system causing the fault current to decay to a small residual current. The oscillation that can be seen between t_5–t_6 is due to the interaction between the L-C branch of the breaker and the source side (system side in the grid). At t_6 the residual current breaker is expected to clear a small oscillating current due to interaction between the source side and the L–C branch of the breaker. The voltage spike that can be observed at t_6 is due to a small current chopping by residual current breaker. The residual current breaker is required also to clear the residual current that would flow through the surge arrester as it is subjected to the system voltage. If not cleared, there will be a small leakage current that gradually results in overheating of the surge arrester.

Note that the DC source in parallel to the capacitor in the electrical diagram shown in Figure 2-5 is required to pre-charge the capacitor. It also considered to charge the capacitor directly from the system to the rated voltage of the system.

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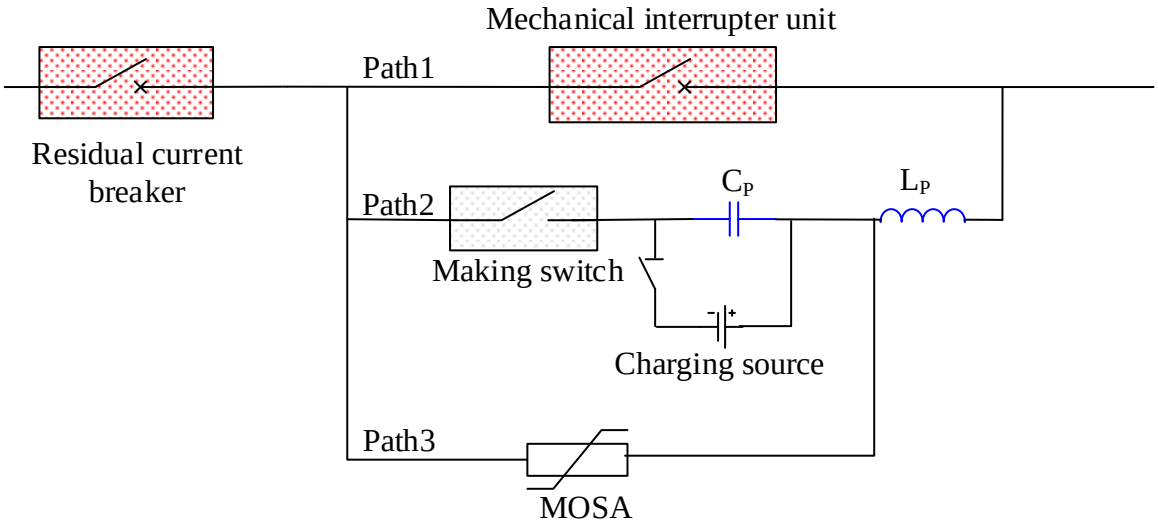

Figure 2-5: Electrical design of active injection HVDC circuit breaker

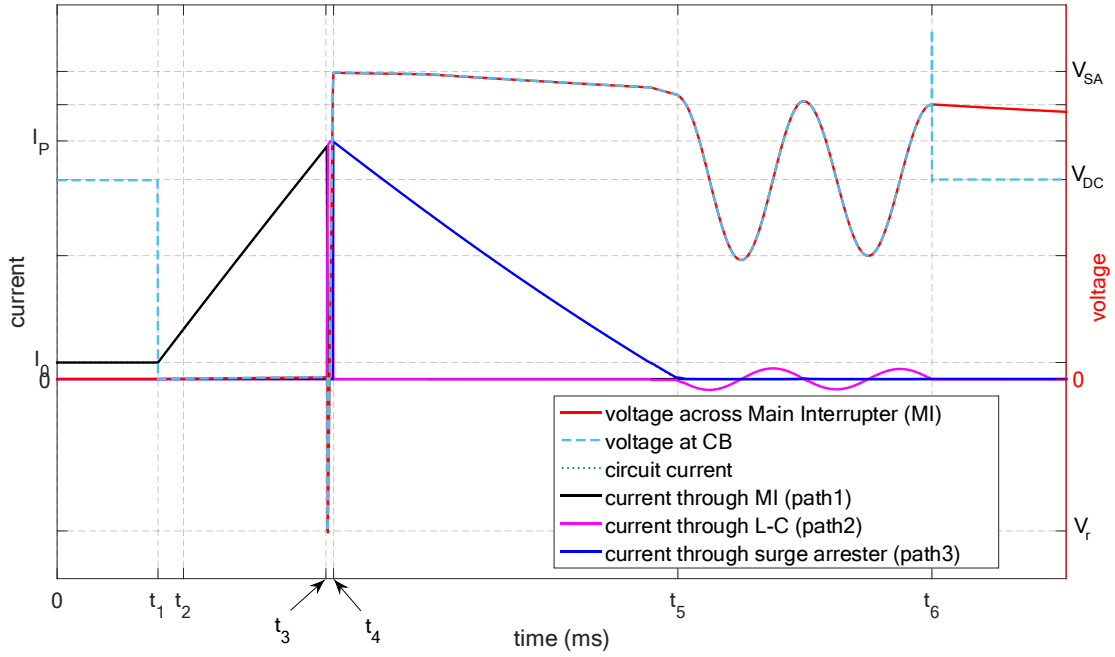

Figure 2-6: DC current interruption process by an active current injection HVDC circuit breaker. Current through and voltage across internal sub-components

If I_P is the peak value of the fault current that can be expected in the system in which the circuit breaker is installed, the capacitor C_P and its pre-charge voltage V_C as well as the indictor L_P must be designed in such a way that the current generated by the L-C ($I_{L\text{-}C}$) branch is higher than the I_P [3]. Mathematically,

$$I_{L-C} > I_P$$

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Where $I_{L-C} = V_C\sqrt{\frac{C_P}{L_P}}$, assuming negligible resistance in the loop of Path1 and Path2.

Besides, if the mechanical interrupter succeeds in extinguishing the arc current during the first zero crossing, there will be remnant charge across the capacitor since the level of discharge of the capacitor depends on the magnitude of the fault current (see Figure 2-6). If the interrupted current is i, the negative voltage across the capacitor (V_r) due to remnant charge following current interruption in the mechanical interrupter at first zero is,

$$V_r = \sqrt{\left(V_C^2 - \frac{L_p}{C_p} i^2\right)}$$

Thus, the lower the current i to be interrupted, the larger the remaining voltage across the capacitor when the main interrupter succeeds in extinguishing the arc at the first zero crossing. This initial TIV (ITIV) may challenge the dielectric recovery of the gap and needs to be considered in a test. If the breaker sustains the negative ITIV, then the TIV rises at a rate determined by the size of the capacitor and the instantaneous value of the interrupted current up to the protection level of the surge arrester.

2.3.2 HYBRID POWER ELECTRONIC HVDC CIRCUIT BREAKERS

Hybrid power electronic HVDC circuit breakers are developed by combining the positive features of mechanical and power electronic switches. A mechanical switch has lower conduction loss in a closed state and better voltage withstand capability in its open state. Besides, compared to the power electronic switches, the pure mechanical breaker is cheaper. The main drawback of a pure mechanical breaker is that it has longer switching time. On the other hand, power electronic switches exhibit higher losses. However, power electronic switches have faster switching times. Hence, hybrid power electronic HVDC breakers combine these properties by utilizing mechanical switches during normal operations and using power electronic switches only during switching. Two types of hybrid HVDC circuit breakers are described in the sections below.

2.3.2.1 HYBRID HVDC CIRCUIT BREAKER TYPE I

Figure 2-7 shows the electrical design of hybrid HVDC circuit breaker type I [4]. Note that there is another hybrid HVDC circuit breaker having similar operation principle but based on full-bridge modules [5]. Under normal load operation, current flows through Path1 consisting of the load commutation switch (LCS) and ultra-fast disconnector (UFD) as shown in Figure 2-7. The load commutation switch is a power electronic switch that can carry the load current with low losses since it contains only a few modules of IGBTs required to commutate the current into the main breaker when ordered to trip. The main breaker consists of many IGBTs connected in series to withstand the TIV that appears across circuit breaker terminals during energy absorption phase of the current interruption process. The operation sequence and the voltage and current waveforms that appear through circuit breaker internal components are shown in Figure 2-8.

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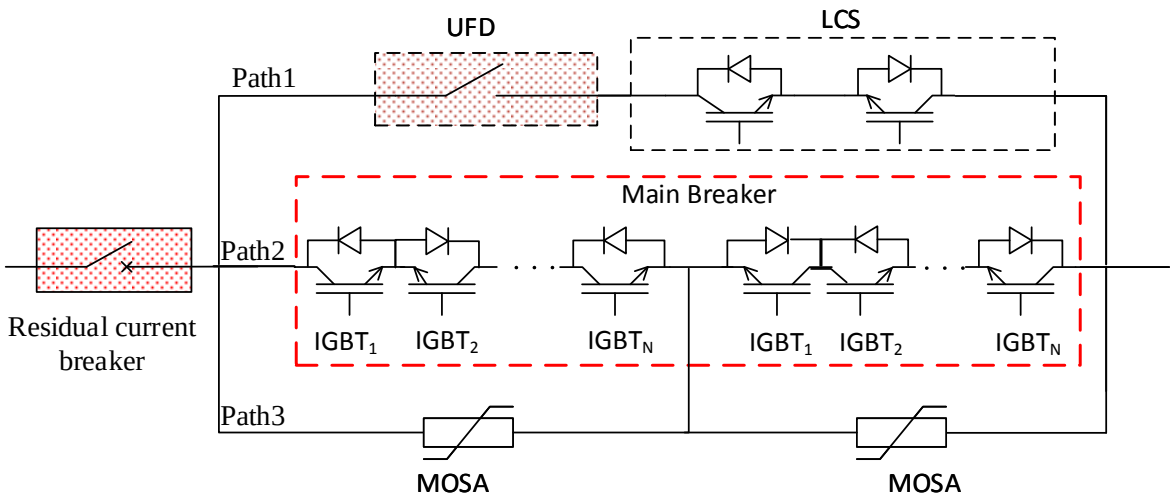

Figure 2-7: Electrical design of hybrid HVDC circuit breaker type I

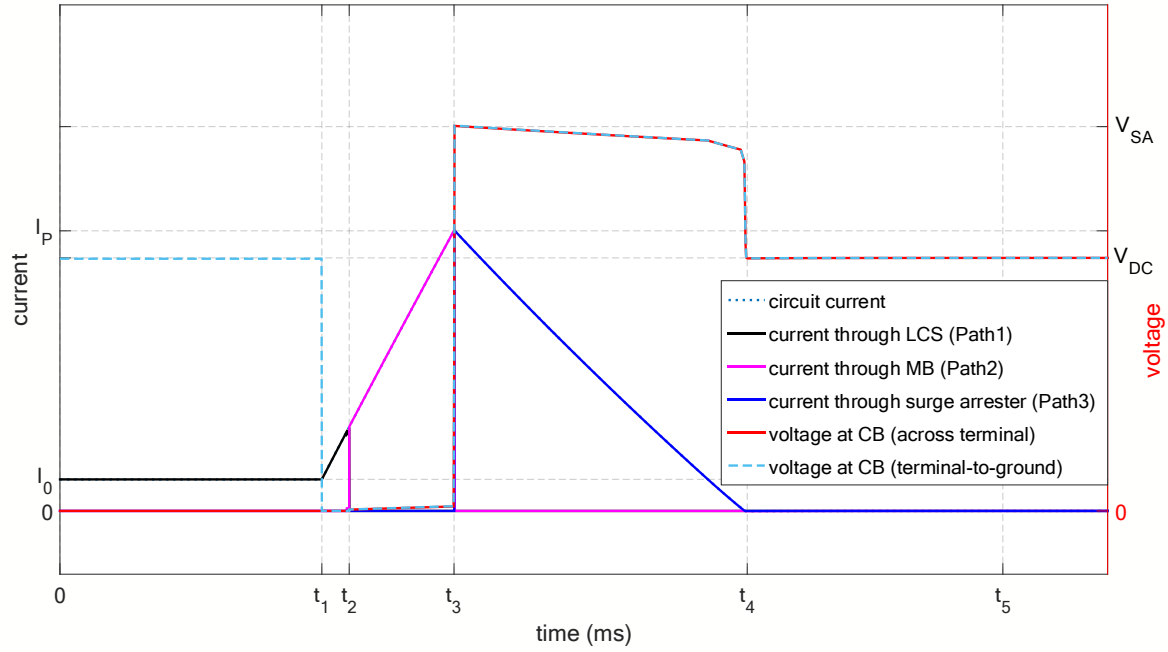

Figure 2-8: DC current interruption process by hybrid HVDC circuit breaker type I. Current through and voltage across internal sub-components

When the breaker receives a trip command, the load commutation switch IGBTs switch off (at t_2 as shown in Figure 2-8). This leads to current commutation into the main breaker in Path2 which has many IGBTs connected in series to withstand the high voltage stress compared to the load commutation switch. However, this branch has higher on-state loss and hence, this is the reason why it is used only during fault current interruption operations. After the current is fully commutated to the main breaker, the ultra-fast disconnector is opened to protect the load commutation switch against transient interruption voltage (TIV) which occurs later when the main breaker opens. By the time the contacts of the ultra-fast disconnector reach the position where it can

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withstand the TIV, the main breaker is switched off (at t_3). The rise of TIV immediately follows the opening of the main breaker and soon it reaches the surge arrester protective voltage level. By this time the surge arrester is turned into conducting mode (Path3) and finally this branch will dissipate the magnetic energy in the system (from t_3–t_4). Consequently, the fault current is interrupted. The resistor-capacitor-diode (RCD) snubber circuits are used to ensure equal distribution and to control the rate of rise of TIV (du/dt) after the main breaker is switched off.

At t_5, the residual current breaker interrupts a small leakage current through the surge arrester and isolates the faulty line from the HVDC grid to protect the arrester banks of the hybrid HVDC breaker from thermal overload [4].

2.3.2.2 HYBRID HVDC CIRCUIT BREAKER TYPE II

The electrical design of the second type of hybrid power electronic HVDC breaker is depicted in Figure 2-9 based on the concept proposed in [6], [7]. It has several current paths categorized as low impedance branch, time delaying branches, arming branch and extinguishing branch. The low impedance branch designated as Path1 in Figure 2-9 consists of an UFD in series with a few power electronic switches (IGBTs) for bypassing short circuit current into the time delaying branches. The time delaying branches consist of thyristors in series with capacitors which, during the interruption process charge sequentially to a voltage proportional to the parting contacts of the ultra-fast mechanical disconnector of the low impedance branch. To limit further increase of the voltage, the capacitors in the time delaying branches have surge arresters in parallel, as shown in Figure 2-9. Besides, in these paths, larger capacitors are chosen to keep rate of rise of voltage lower. When the UFD reaches sufficient separation, the thyristors in the arming branch (shown in Path3) are switched on and, the capacitor C_3 starts charging. When voltage across C_3 reaches the protective level of surge arrester SA_3 in the extinguishing branch (shown as Path4), the short-circuit current commutates to this path and the magnetic energy stored in the system is dissipated.

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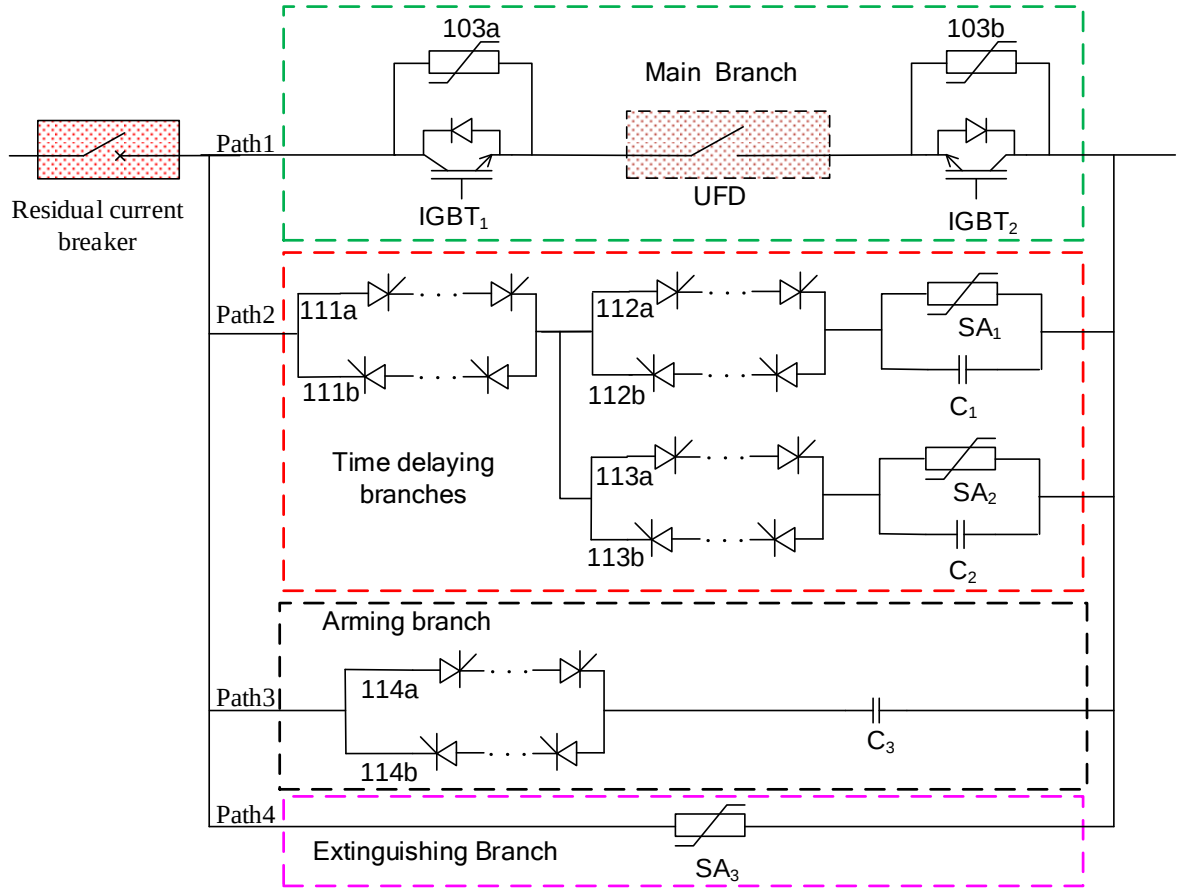

Figure 2-9: Electrical design of hybrid HVDC circuit breaker type II

Figure 2-10 shows the operation sequence of hybrid HVDC circuit breaker type II along with the voltage and current waveforms that can be seen through the internal sub-components during DC current interruption. Under normal operating condition, current flows through the low impedance branch (Path1) of Figure 2-9. As soon as a fault is detected (at t_2 in Figure 2-10), the IGBTs in this path block and the thyristors in path 111a and 112a switch on simultaneously. The IGBTs are protected from overvoltage by the surge arrester 103a & 103b, thus, current flows through the surge arresters until the thyristors 111a and 112a are fully turned on. Due to initially uncharged capacitor C_1, current commutates to this branch through the thyristors. As soon as current is commutated from Path1 to Path2, the TIV starts to build up across the breaker. This voltage is prevented from further rise by surge arrester SA_1 (from t_2–t_3) after the capacitor C_1 is fully charged. At t_3, thyristors 113a switch on and similarly, due to the capacitor C_2, current commutates to this branch. Since the capacitor C_1 is charged, it attempts to inject current opposite to fault current which, however, naturally turns off thyristor 112a. The charging voltage of C_2 is higher than that of C_1. In a similar manner, as for C_1, the voltage across C_2 is prevented from further rise by surge arrester SA_2 until the thyristors 114a are turned on at t_4. In a similar way, the current is commutated to Path3.

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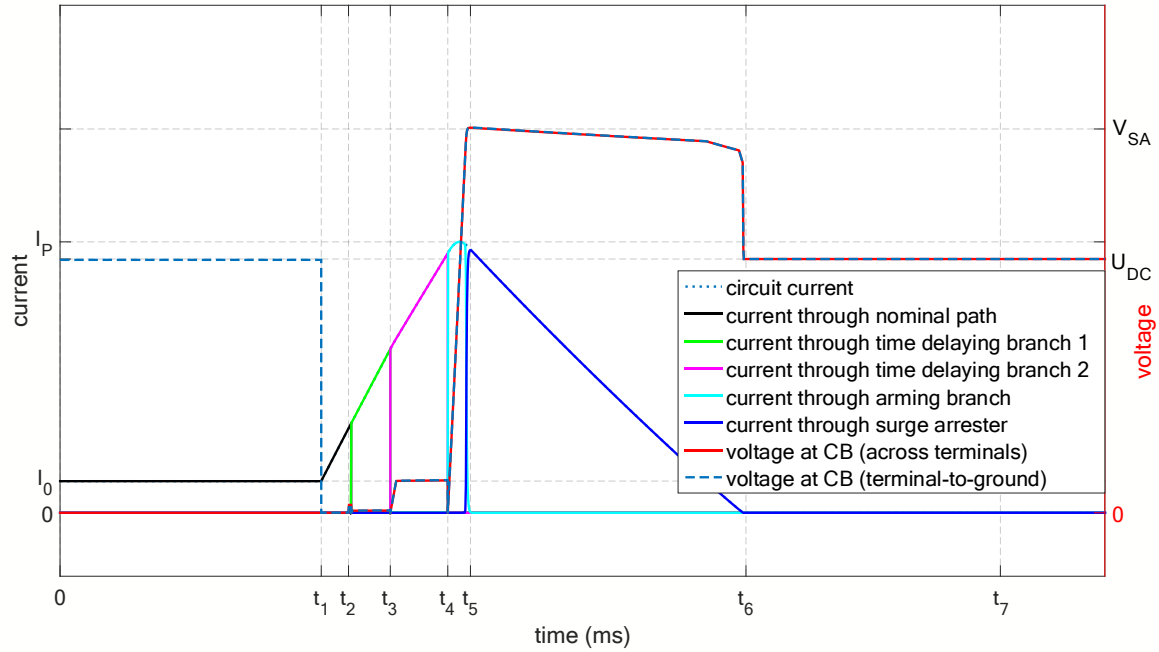

Figure 2-10: Current interruption process using hybrid HVDC circuit breaker type II. current through and voltage across internal sub-components

It is important to note that the UFD opens by the time current is fully commutated to Path2. After current commutates to Path3, the voltage across the breaker (TIV) starts to build up (from t_4–t_5) to a protection level of surge arrester SA_3. This makes the current to commutate to Path4 and finally cease to flow as the energy in the system is absorbed by this surge arrester (from t_5–t_6). It is important to note that the protection levels of the surge arresters (and the voltages across capacitors) at each path are designed to exceed the protection level in the previous path so that the TIV builds up in a controlled manner. At t_7 the residual current breaker isolates the HVDC circuit breaker from the system to avoid thermal stress on SA_3 due to a small leakage current that would continue to flow. Further details can be read in [6].

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3 SIMULATION RESULTS

3.1 INTRODUCTION

One of the goals of WP5 is to define the test requirements of HVDC circuit breakers using the stresses obtained from the system study. For this purpose, the different technologies of HVDC circuit breakers modelled using EMTDC/PSCAD are inserted along with a series DC current limiting reactor at the ends of each cable in the MTDC network shown in Figure 3-1. The objective in this chapter is, therefore, to investigate the DC fault current interruption process by various types of HVDC circuit breakers in a multi-terminal HVDC grid. Thus, the interaction between the HVDC circuit breakers and the HVDC grid as well as the stresses that can be observed on different types of circuit breakers during fault current interruption are studied in detail. In Figure 3-1, the HVDC circuit breakers are designated by the boxes labelled as numbered CBs. The blackbox models of the HVDC circuit breakers developed in D5.2 are used in the simulation study of this chapter.

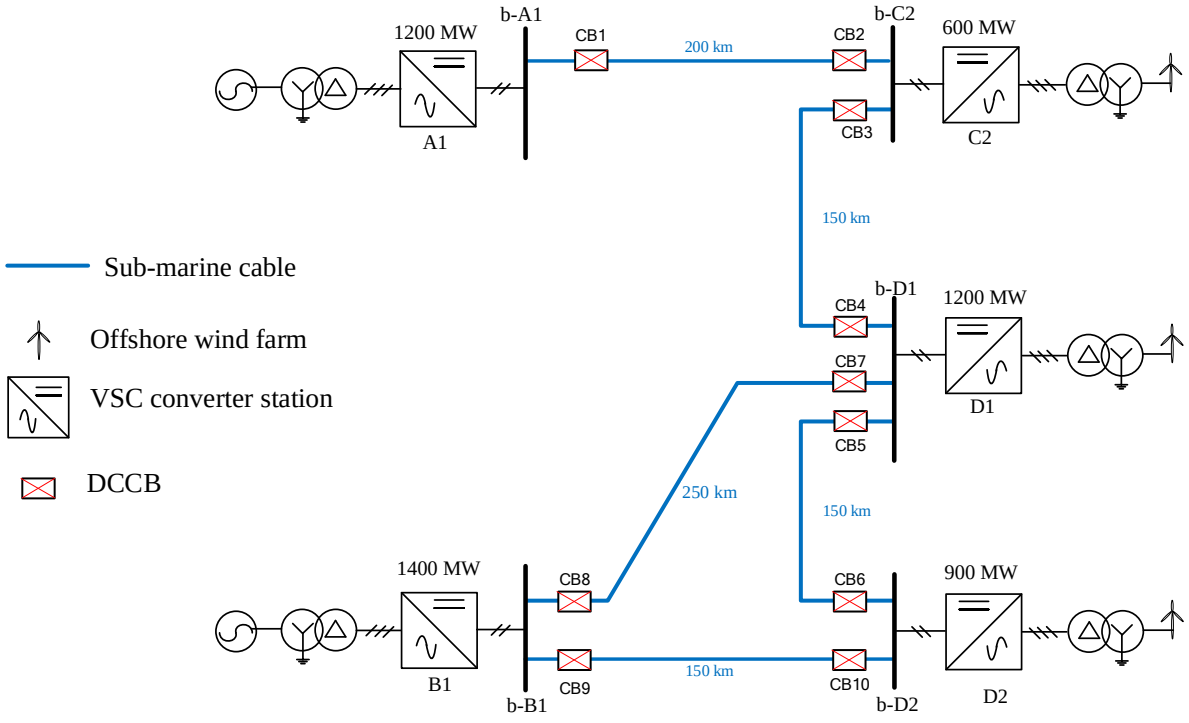

Figure 3-1: Five terminal HVDC network with embedded HVDC circuit breakers at the ends of HVDC cables

Figure 3-1 shows a five-terminal meshed HVDC network which was defined for fault analysis in deliverable D5.1 [1] (see the system parameters in appendix A). Since the system does not have a protection system, a fault detection based on local overcurrent measurement is assumed and implemented. Thus, a circuit breaker generates a trip order the moment an overcurrent threshold of 3 kA is detected on a line in which it is installed. Also, an additional assumption is required regarding the protection system, for instance, for high impedance

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faults. Thus, a breaker receives a trip order at the latest 2 ms after a fault appears in the system assuming, within this time, the protection system can detect and correctly locate any fault so that only the circuit breakers at the ends of the faulted cable receive a trip order. Therefore, when either of the two conditions are satisfied the circuit breaker starts the current interruption process.

Based on the assumptions mentioned earlier, several simulations have been performed for each type of HVDC circuit breaker technologies. As in deliverable 5.1 only a pole-to-ground fault is simulated using the HVDC grid shown Figure 3-1. For a pole-to-pole fault, a radial network built from symmetric monopole converters is simulated in Section 3.7. It has been found in D5.1 that, for a grid shown in Figure 3-1, a fault close to converter D1 results in the highest rate of rise of fault current. The main reason is that this converter has a high-power rating among offshore converters. In addition, since it is always sending power, the fault current does not change direction during fault. For converters A1 and B1, at steady state, power is flowing into these converters and when a fault occurs nearby these converters, the direction of current flow has to change and it therefore takes a longer time to reach overcurrent threshold (or the fault is detected long before the current reaches high value).

Hence, a pole-to-ground fault is applied on the positive pole of cable B1-D1 at various locations (10 km, 100 km and 240 km from converter D1) and is cleared by CB7 and CB8. The stresses on CB7 and CB8 are analyzed for different technologies of HVDC circuit breakers in the proceeding sections. In addition, since there is no clear specification in the literature for a condition beyond which a converter must block during fault, under voltage of 0.75 p.u. at converter DC terminal and/or overcurrent of 4 kA per arm are assumed for blocking in the simulations.

3.2 SIMULATION RESULTS OF CURRENT INTERRUPTION USING ACTIVE CURRENT INJECTION HVDC CB

In this section a model of active current injection HVDC circuit breaker described in Section 2.3.1 is embedded in the benchmark study grid shown in Figure 3-1. The capacitor and inductor in the current injection branch are dimensioned for rated interruption current of 16 kA. The capacitor is charged to the system voltage since it is expected that in the practical application this capacitor is charged by the system rather than by a separate source.

Current limiting reactors of 150 mH are used at the ends of each cable for simulations involving active current injection HVDC circuit breakers. It is desired that at most only the converters at either end of the faulted cable are affected by over-current and/or under voltage, and hence may block, during the fault neutralization period of the interruption process. A fault is applied at 10 km from converter D1 on cable B1-D1. Figure 3-2 depicts simulation results showing the interaction of the active current injection HVDC circuit breaker (at CB7, see Figure 3-1) with the system during fault clearing. The current through and voltage across the breaker internal branches as well as the voltage at the D1 converter's DC terminal during fault current interruption process are

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overlaid on one graph. The left and the right-side y-axis show current and voltage, respectively. A breaker operation time of 8 ms is assumed in this simulation. A pole-to-ground fault is applied at 1 ms and the interruption process is initiated as the mechanical interrupter starts opening its contacts when the fault current reaches a value of 3 kA. The fault current continues to flow via the arc path between the contacts of the mechanical interrupter (shown by the black curve in Figure 3-2) until counter current is injected from the pre-charged capacitor 8 ms later. The mechanical interrupter extinguishes the arc at first zero crossing and then the current commutates to the L-C branch. The moment the arc is extinguished at the mechanical interrupter the negative voltage due to the remnant charge on the capacitor appears across the interrupter (this is indicated by V_r on the red curve). Then the system current charges the capacitor until the surge arrester protective voltage level is reached. After this time the fault current is suppressed until the leakage current is reached and it is assumed that the residual current breaker clears the residual current at the first current zero (due to oscillations of the L-C path with the system) and hence no oscillation can be seen after fault current suppression period.

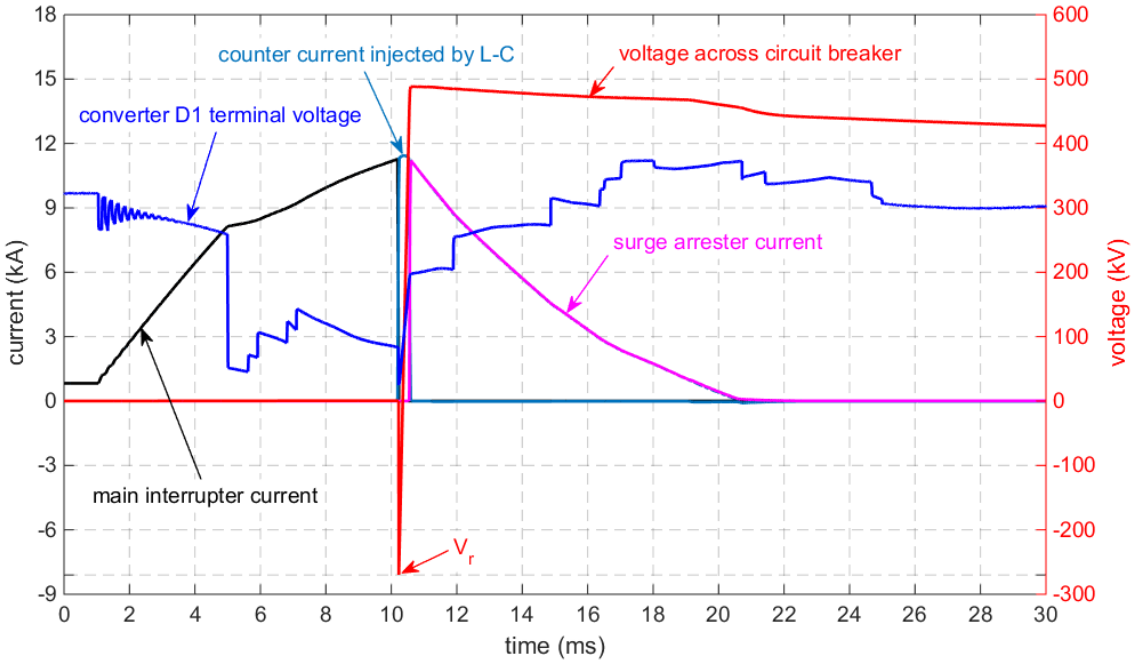

Figure 3-2: Fault current interruption by active current injection HVDC circuit breaker CB7 after a fault 10 km away. Interaction of circuit breaker with the system

Looking at converter D1 terminal voltage, it decreases slowly until the converter blocks due to overcurrent through one of its arms. The converter blocking leads to the collapse of the DC bus voltage. The oscillation that can be seen immediately after the fault is because of back and forth travelling waves between the converter and the fault location. This is explained in detail in D5.1 [1]. However, the interesting point to note here is that the converter terminal voltage starts to recover the moment the circuit breaker starts building up the counter voltage across its terminals. Thus, although the fault is not completely cleared, the system voltage restores during the energy dissipation phase of the interruption process. This phenomenon has significant impact on the amount of energy that the circuit breaker must absorb which is described in detail below.

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Figure 3-3 shows the current (top graph) through and the voltage (middle graph) across the CB7 and CB8 when these circuit breakers clear the fault on cable B1-D1. The fault is applied at 240 km from CB8 and the trip signal is sent to this breaker 2 ms after the fault is applied not because of overcurrent measured at this CB but because of the assumption that the protection system can detect and locate the fault by this time. Since the current through CB8 changes direction (the pre-fault current is of opposite polarity as that of CB7 at the other end of the line), it takes a relatively longer time until the overcurrent threshold of 3 kA is reached. Although the fault current rises rapidly during the first three milliseconds after the occurrence of the fault, this rate reduces significantly during the next milliseconds due to the incidence of reflected travelling waves as described in detail in deliverable D5.1. Also, the converter B1 blocks due to under-voltage at about 7.5 ms (see Figure 3-3).

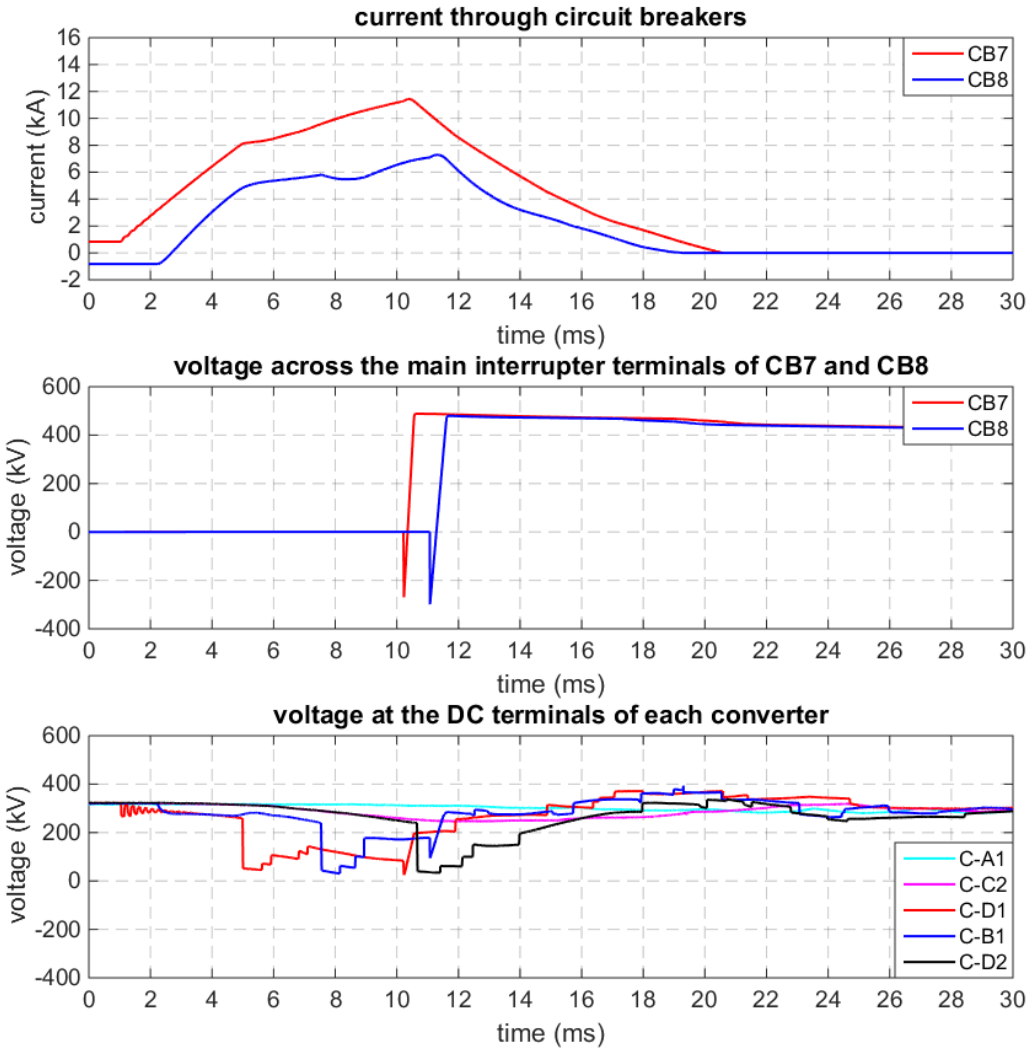

Figure 3-3: Fault current interruption by active current injection HVDC circuit breakers (CB7 and CB8) when a fault is applied at 10 km from CB7 on cable B1-D1 (top graph), the voltage across main interrupter terminals (middle graph) and converter terminal voltage (bottom graph).

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Therefore, the peak interrupted fault current at CB8 is lower than the peak interrupted fault current at CB7. Because of this, the magnitude of the initial TIV due to remnant charge (V_r) on the capacitor of CB8 is larger than the corresponding voltage of CB7. (Note that the pre-charged capacitor in all the circuit breakers are charged to the system voltage of 320 kV).

The bottom graph of Figure 3-3 shows the DC terminal voltages at all converter stations. In addition to the converters that are directly connected to the faulted cable (converters D1 and B1), converter D2 which is not directly connected to the fault cable also blocks due to under voltage. To avoid this larger DC current limiting reactors can be used. However, the impact of increasing DC current limiting reactors on the converter power flow control must be investigated. Besides, increasing the size of current limiting reactor has an impact on the energy that the circuit breaker must absorb. Nevertheless, it can be seen from the bottom graph of Figure 3-3 that the system voltage recovers even before the fault is completely cleared. Thus, the breaker operation time is the important parameter from a system perspective. The shorter the breaker operation time, the faster the system voltage is restored.

It is described in Chapter 2 that one of the requirements of the HVDC circuit breaker is that it must be able to absorb the magnetic energy stored in the system. Figure 3-4 shows the energy that CB7 and CB8 must absorb during current interruption by the active current injection HVDC circuit breaker.

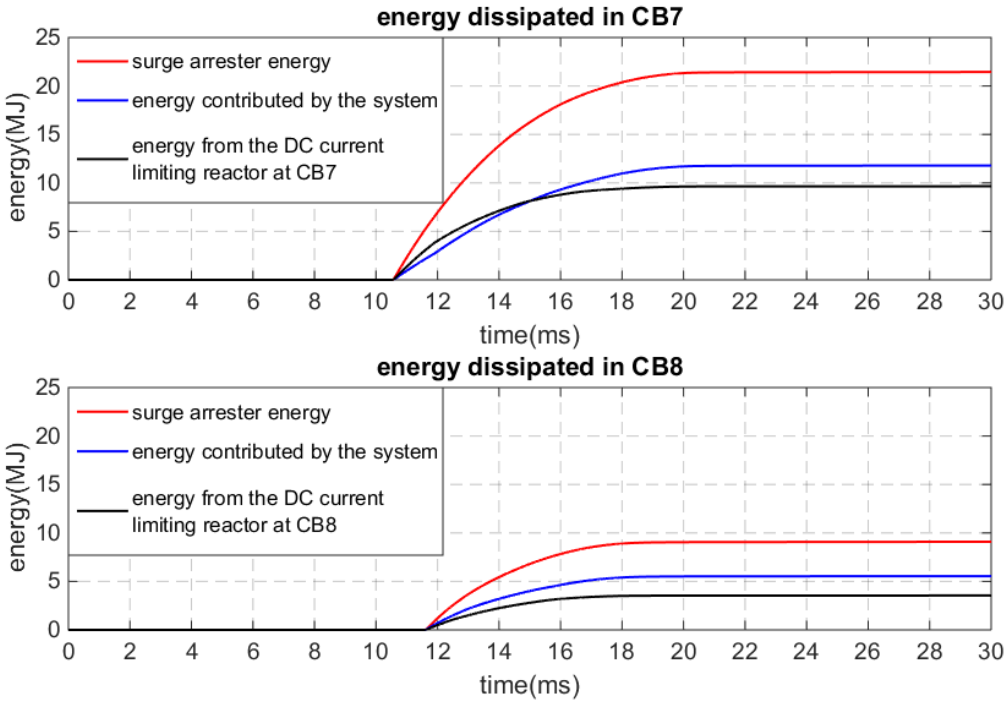

Figure 3-4: Energy absorbed by active current injection HVDC circuit breakers during fault current interruption when a fault occurs 10 km from CB7 on cable B1-D1 (red curves). The blue and black curve show the energy contributed by the system and the energy coming from the stored energy of DC current limiting reactor, respectively.

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The total energy dissipated in the surge arresters (excluding the negligible energy stored in various components) of each circuit breaker is shown by the red curves. The total energy is further decomposed into two sources; namely, the energy stored in the DC current limiting reactor at the corresponding circuit breaker (shown by black curves) and the energy coming from the other parts of the system including the converters and incoming feeders at a node where the circuit breaker is installed (depicted by blue curves). Note that the energy stored in the DC current limiting reactor at the beginning of the energy dissipation phase is $0.5\,Li_P^2$ and this energy is dissipated over the fault suppression period as shown by the black curves.

From Figure 3-4, it can be concluded that it is not only the system magnetic energy that the circuit breaker must dissipate but also the electrical energy coming from the system during the fault current dissipation period. The latter comes inevitably since the breaker requires some time to dissipate the magnetic energy. The energy contributed by the system is determined by the power flowing into the circuit breaker from the converter DC bus. Since the DC bus voltage recovers during the energy dissipation phase of the interruption process, the energy coming from the grid is even larger than the energy stored in the DC current limiting reactors at each of the circuit breakers (CB7 and CB8), see Figure 3-4. The relationship between the size of the DC current limiting reactor and the energy dissipated in the circuit breaker is illustrated mathematically in more detail in Chapter 4.

Table 3-1 summary of interrupted current and energy dissipated

	Peak fault current (kA)	Average rate of rise of current (kA/ms)	$\frac{1}{2}LI_P^2$ (MJ)	Energy from the system (MJ)	Total energy dissipated (MJ)
CB7	11.44	1.14	9.645	11.78	21.43
CB8	7.29	0.89	3.536	5.527	9.075

3.3 SIMULATION RESULTS OF CURRENT INTERRUPTION BY HYBRID HVDC CIRCUIT BREAKER TYPE I

Figure 3-5 shows the simulation result when a fault occurring at 10 km from CB7 on cable B1-D1 is applied. In this case, current limiting reactors of 100 mH are used at the ends of each cable because the breaker operation time of the hybrid HVDC circuit breaker is short (2 ms is assumed as indicated in [4]).

In a similar way, as for the active injection HVDC circuit breaker described in Section 3.2, the hybrid HVDC breakers receive the trip orders when either of the two conditions are fulfilled. That is, if 3 kA overcurrent is measured through the nominal current path (for example, CB7 in this case) or if 2 ms time has elapsed after the fault is applied. It can be seen from Figure 3-5 that lower peak currents, for example about 8.3 kA and 6.4 kA are interrupted by CB7 and CB8, respectively, compared to the current interrupted by the active current injection HVDC circuit breakers although a 150 mH DC current limiting reactor is used in series with the latter. This difference is mainly due to the difference in the breaker operation times of these technologies.

Moreover, it can be seen from Figure 3-5 that the circuit breakers clear the fault before any of the converters block. Since the fault is applied 240 km from CB8, the circuit breaker at CB8 clears before the travelling waves are completely damped. This can be observed from the oscillation of the voltage across CB8 after the current

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interruption. Moreover, the point on the travelling wave at which the circuit breaker start to build its counter voltage (TIV) is very important since it has a significant implication on the voltage across the circuit breaker terminals to ground. This is illustrated in detail in Section 3.5.

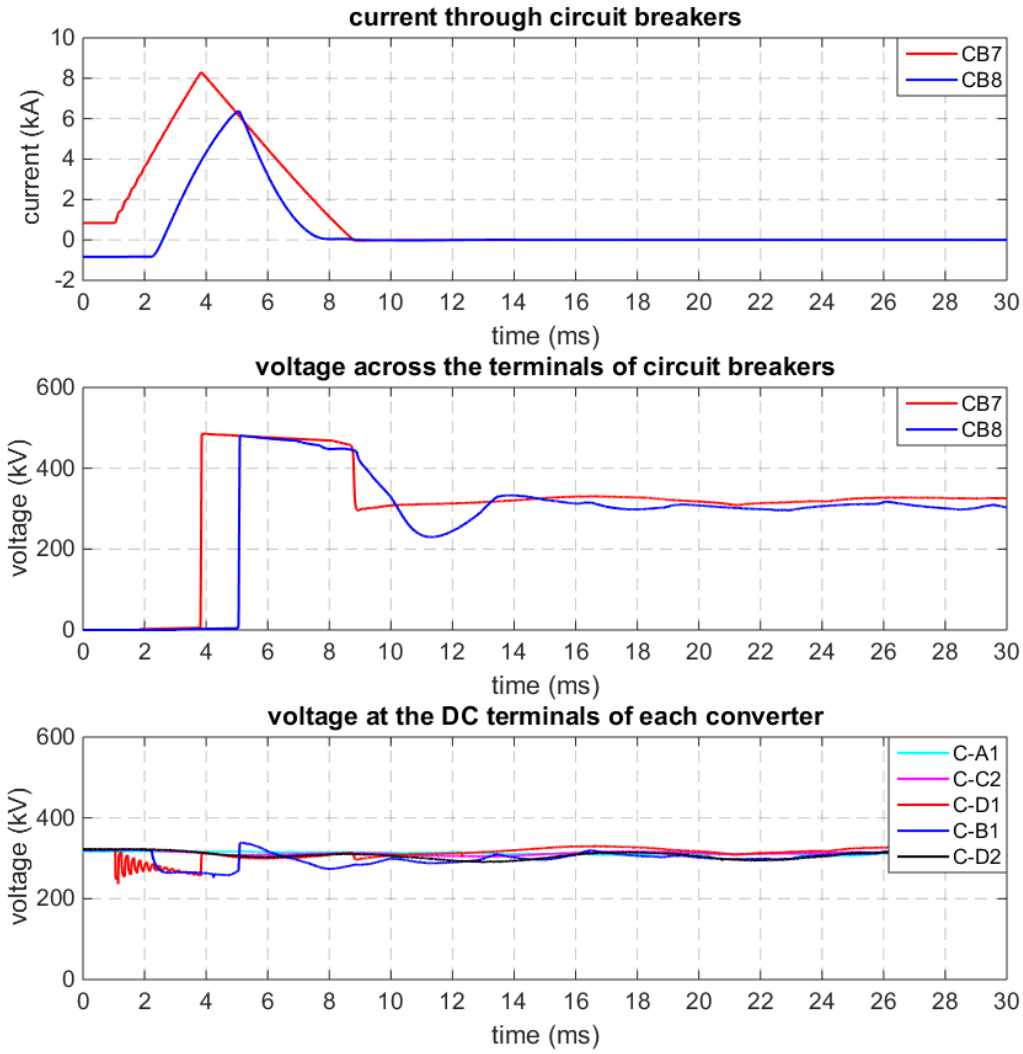

Figure 3-5: Fault current interruption by hybrid HVDC circuit breaker type I (at CB7 and CB8) when a fault is applied at 10 km from CB7 on cable B1-D1.

Figure 3-6 depicts the energy dissipated by CB7 (top graph) and CB8 (bottom graph) by further decomposing the total energy dissipated into the energy supplied by various sources during the fault current interruption. It can be seen from the figure that more energy is supplied by the system than the energy stored in the DC current limiting reactor installed in series with the breaker. Besides, compared to the energy absorbed by active current injection HVDC circuit breaker described in 3.2, hybrid HVDC circuit breaker absorbs less than half of the energy the former must absorb.

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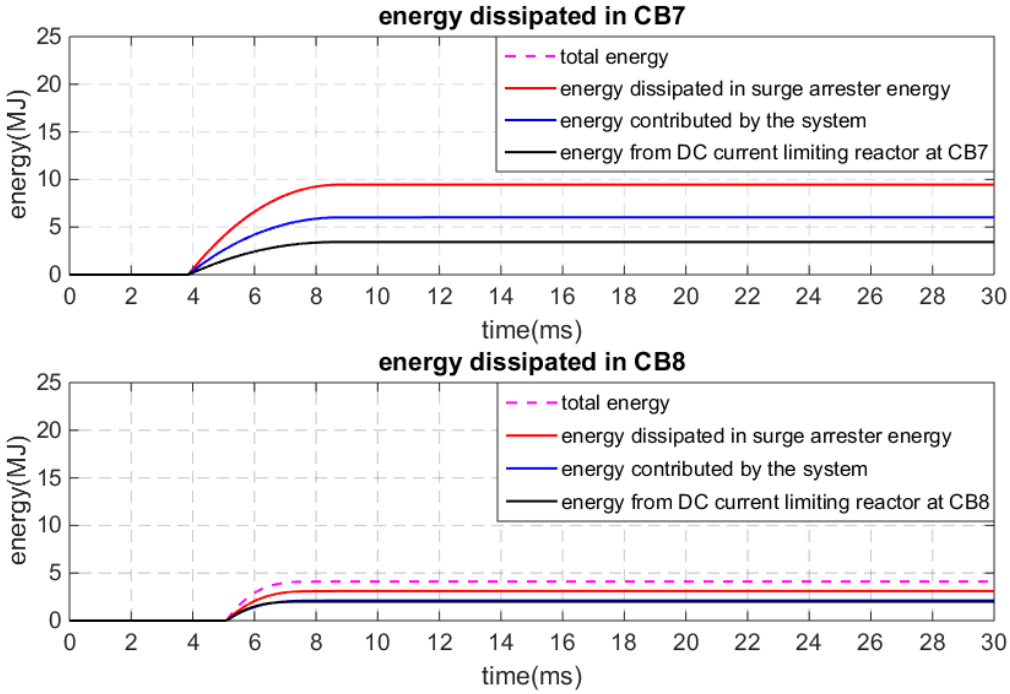

Figure 3-6: Energy absorbed by the hybrid HVDC circuit breakers type I during fault current interruption

Note that not all the energy is absorbed by the surge arrester of a circuit breaker for all the fault conditions, especially when a fault is occurring far from a circuit breaker. For instance, in the above simulation the fault is applied at 10 km from CB7 and the same fault is located at 240 km from CB8. It can be observed from the top graph of Figure 3-6 that, all the energy stored in the DC reactor as well as the energy coming from the rest of the system is absorbed in CB7. However, from the bottom graph of this figure, the total energy flowing into the fault through CB8 is not entirely dissipated in the circuit breaker. This is mainly due to the travelling waves carrying some portion of this energy along the cable to the fault location. In the case of CB7 since the fault is occurring close to the circuit breaker, the travelling waves are completely damped during the fault neutralization period and hence no energy is carried along the cable.

When the fault neutralization period is long (e.g. as for active injection HVDC CB discussed in Section 3.2), the travelling waves could neutralize out as well depending on the length of the cable and the distance of the fault from the circuit breaker. However, in terms of the energy that the circuit breaker must absorb, the condition that must be considered for testing is when the fault is occurring close to a converter terminal since this results in much more energy than when a fault occurs at a long distance. Nevertheless, the travelling waves have an impact on the terminal-to-ground voltage of the circuit breaker as well as at the converter terminal (the latter depends on the size of DC reactor).

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Table 3-2: Summary of fault current interuption by hybrid HVDC circuit breaker type I

	Peak fault current (kA)	Average rate of rise of current (kA/ms)	$\frac{1}{2}LI_P^2$ (MJ)	Energy from the system (MJ)	Total energy dissipated (MJ)
CB7	8.30	2.678	3.436	6.016	9.454
CB8	6.4	2.545	2	2.11	3.107

3.4 SIMULATION RESULTS OF CURRENT INTERRUPTION BY HYBRID HVDC CIRCUIT BREAKER TYPE II

In this section a model of hybrid HVDC circuit breaker type II is inserted in the benchmark study grid. Like for hybrid HVDC circuit breaker type I, DC current limiting reactors of 100 mH are used at the ends of each cable in this case. Also, a breaker operation time of 2 ms is assumed for hybrid HVDC circuit breaker type II [6].

Figure 3-7 shows the detailed interaction between hybrid HVDC circuit breaker type II and the converter DC bus during interruption of fault current of a fault located 10 km from the circuit breaker. The current commutation through various branches as well as the counter voltage generation across the circuit breaker are shown with the left and right side y-axis scales for current and voltage, respectively.

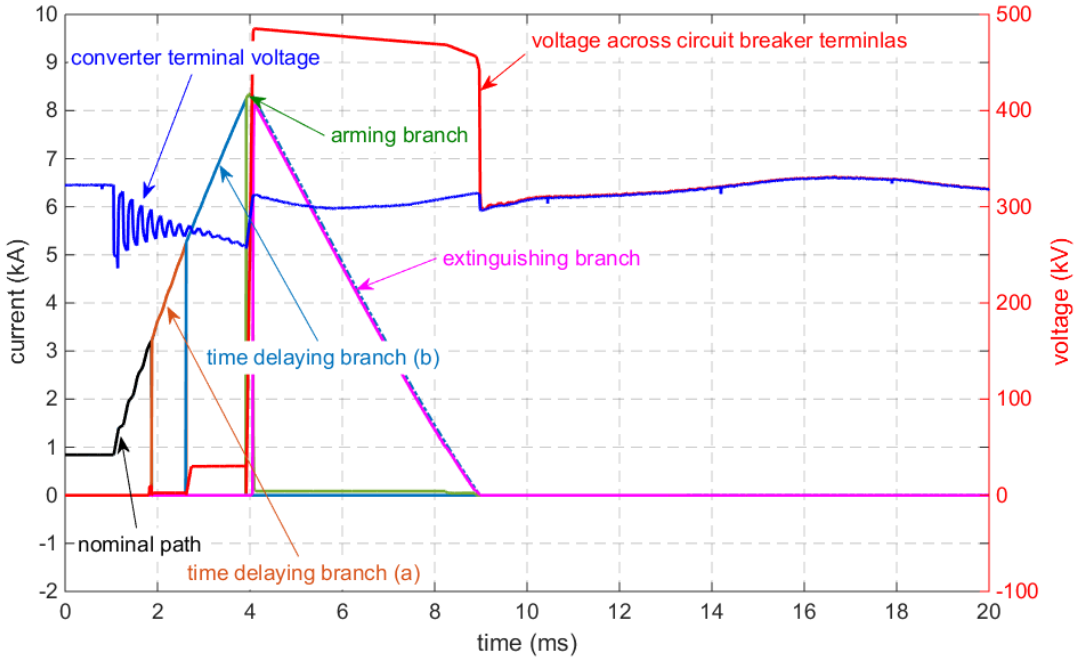

Figure 3-7: Sequence of operation and interaction of hybrid HVDC circuit breaker type II during fault current clearing in HVDC grid. Left side y-axis shows current and right side y-axis shows the voltage.

Although several time delaying branches are recommended for high system voltages [7], only two time delaying branches are used for simplicity in the circuit breaker model. Besides, there is no sufficiently detailed information available in the public literature regarding the internal switching times. Thus, the switching times and

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sequences used in the simulations are merely estimations from test graphs available in the literature. However, as the number of time delaying branches increases, the breaker operation time increases (more than 2 ms).

Figure 3-8 depicts fault current interruption (top graph) by hybrid HVDC circuit breaker type II at CB7 and CB8 when a pole-to-ground fault is applied 10 km from CB7 on the cable B1-D1. Since, the same size of DC current limiting reactor and equal breaker operation time is assumed as for hybrid type I HVDC circuit breaker, the simulation results are very similar to the results obtained using hybrid type I circuit breaker (Figure 3-5). Only very slight differences in peak interrupted currents due to relatively higher impedances provided by the large capacitors in the time delaying branches as well as arming branch of hybrid HVDC circuit breaker type II is observed.

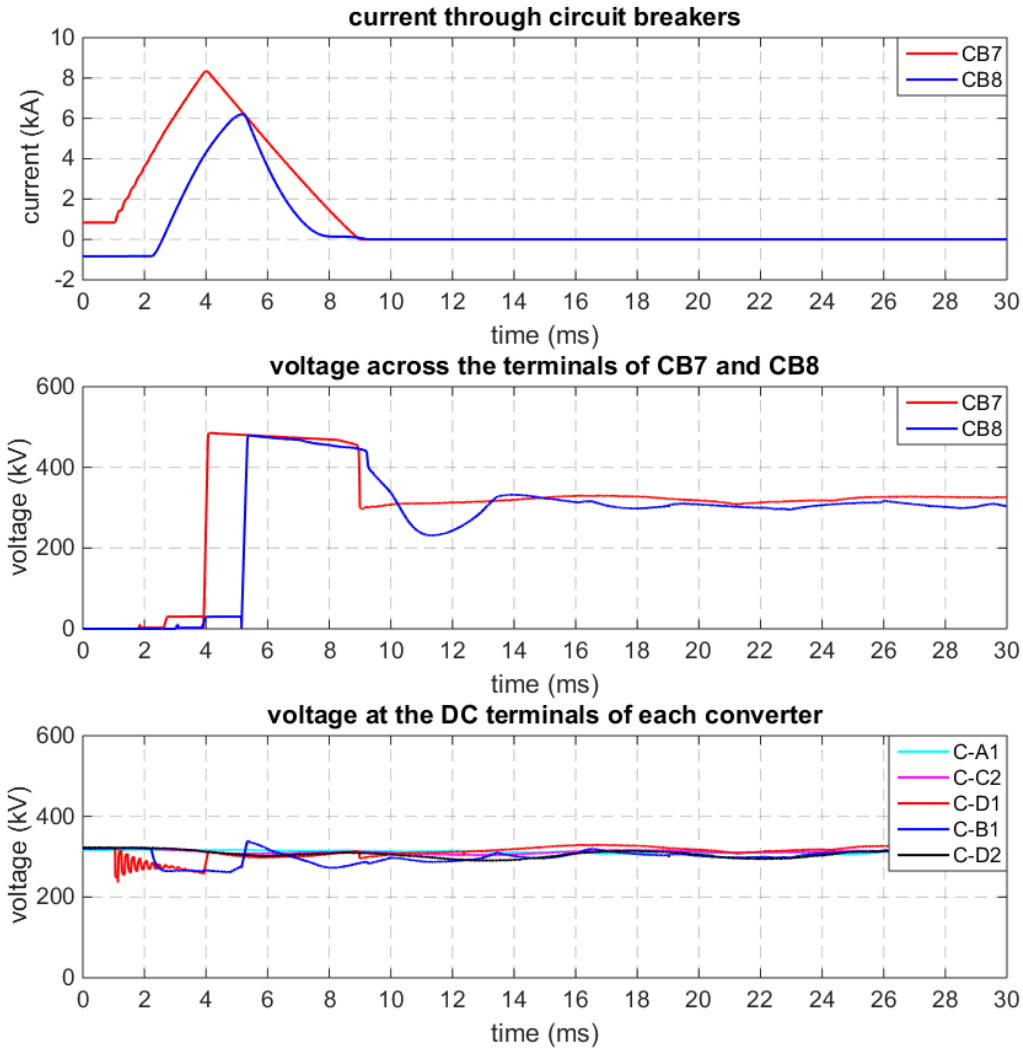

Figure 3-8: Fault current interruption by hybrid HVDC circuit breaker type II

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Figure 3-9 shows the energy dissipation during fault current suppression time of the interruption process. The energy contributed by the system (blue curves) and the energy contributed from the stored energy in the DC current limiting reactor (black curves) during the energy dissipation phase are shown. Note that a small portion of energy that is stored in capacitors in various paths of this circuit breaker are not included in Figure 3-9. Only the energy absorbed in the surge arrester of extinguishing branch is shown. Moreover, since there are number of surge arresters in the circuit breaker (parallel with each of the capacitors and the IGBTs), there is also part of the energy that is absorbed by these surge arresters. Compared to the energy dissipated in the extinguishing branch the energy dissipated in the other surge arresters is negligible and this is not considered in Figure 3-9.

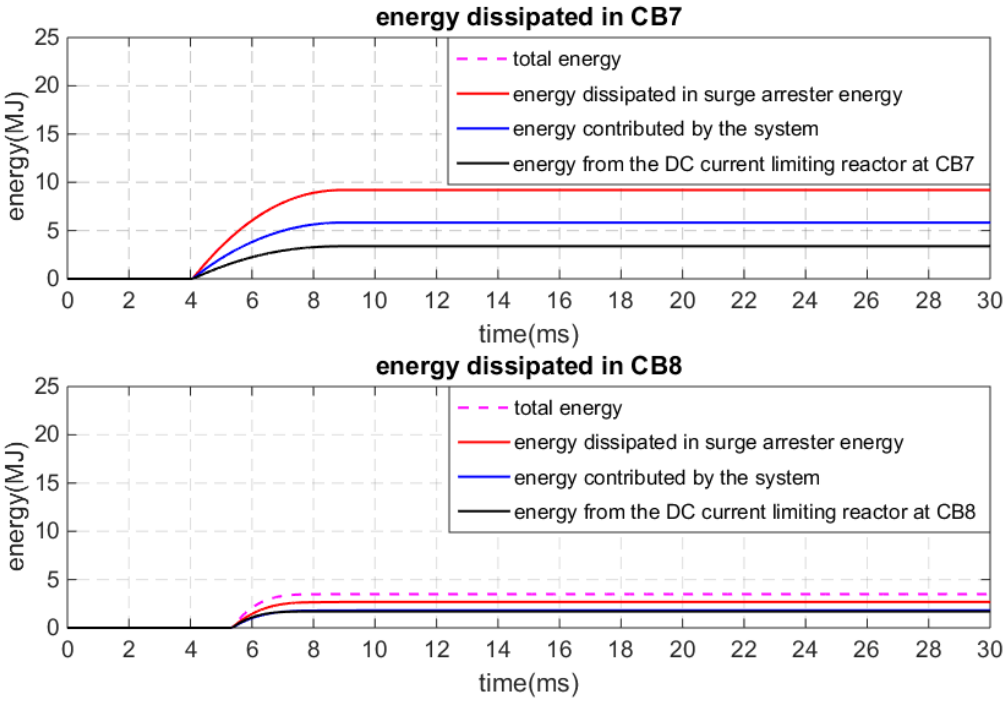

Figure 3-9: Energy dissipated in the HVDC circuit breakers during fault current interruption

3.5 IMPACT OF FAULT LOCATION

In deliverable D5.1 [1], it was indicated that one of the key factors affecting the rate of rise of fault current is its location within a grid. The fault occurring at long distance from a converter station has higher initial rate of rise current. This can also be seen from Figure 3-10 which shows current interruption by CB7 (hybrid HVDC circuit breaker type I) at three different locations along cable B1-D1. For instance, for a fault at 100 km from CB7 the initial rate of rise is the highest (see blue curve in top graph of Figure 3-10). However, due to back and forth travelling waves between the converter DC bus and the fault location, the average rate of rise becomes lower than when a fault current occurs close to a converter terminal.

Assuming, the fault neutralization time of t_N, theoretically the highest rate of rise of fault can be observed when a fault occurs at least at distance S from a circuit breaker where S can be determined as follows [8];

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$$S \geq \frac{v \cdot t_N}{3}$$

Where v is the travelling wave propagation speed through the cable.

Note that t_N is measured from the moment the fault is applied and not from the moment it starts to rise at the circuit breaker. The propagation speed of travelling waves in the cable considered in the simulation is circa 190 km/ms. From top graph of Figure 3-10, it can be seen that the black curve has the highest average rate of rise among the three different faults. However, the resistance of the cable up to the fault location including the fault resistance affects the average rate of rise as it attenuates the travelling wave. This is a reason why the blue curve has the highest initial rate of rise since the travelling waves are attenuated less in 100 km than in 240 km.

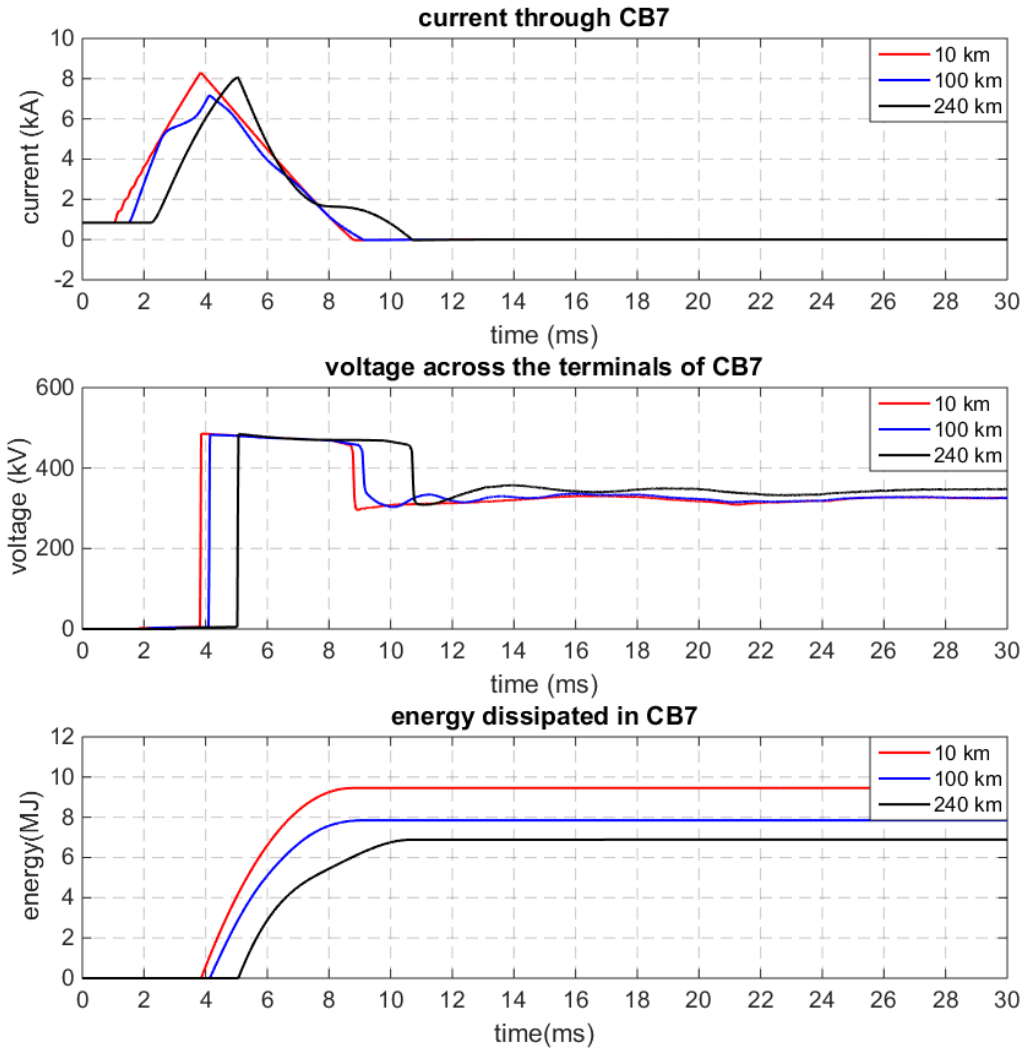

Figure 3-10: Fault current (top graph) through, voltage (middle graph) across CB7 and energy dissipated (bottom graph) in CB7 (using the model of hybrid HVDC circuit breaker type I) during current interruption for a fault on cable B1-D1 at different locations

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In general, in terms of the average rate of rise as well as the peak fault current, a fault close to a converter terminal is the worst for a circuit breaker. This can be seen from the red curve in the top graph of Figure 3-10. Moreover, the travelling waves have considerable impact on the rate of decay of fault current during fault current suppression period (see black curve in the top graph of Figure 3-10). Because of this the energy dissipated in the circuit breaker is lower when a fault occurs at a long distance, than the energy dissipated in the circuit breaker for a fault occurring close to a converter station. Thus, the energy dissipated in a circuit breaker decreases with the fault location distance (see bottom graph of Figure 3-10). As the fault location along the cable increases from the circuit breaker CB7, the impact of voltage oscillation on the circuit breaker becomes more apparent.

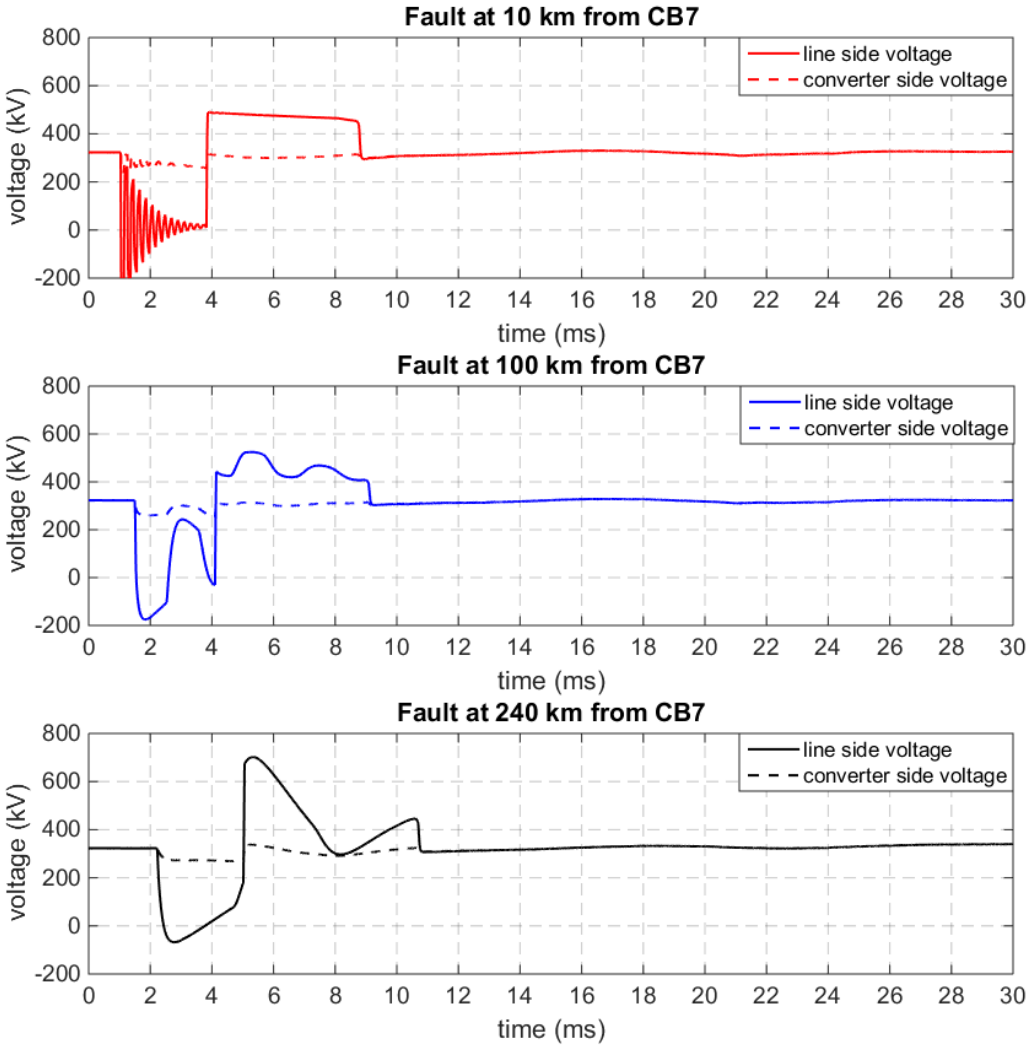

Figure 3-11: Converter side and line side voltage measured before and after DC current limiting reactor at CB7, respectively, for a fault at different location along cable B1-D1. Hybrid HVDC circuit breaker type I is interrupting

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Figure 3-11 shows the line side (solid line) and converter side voltages measured at the terminals of DC current limiting reactor at CB7. It must be noted that the voltage across the circuit breaker is superimposed on the oscillating line side voltage. When the circuit breaker starts the interruption process, the line side voltage is in fact a superposition of the travelling wave voltage and the circuit breaker voltage. Thus, depending on the position of the current limiting reactor relative to the HVDC circuit breaker, the line side voltage appears as voltage-to-ground at the circuit breaker terminal and can (theoretically in case of zero attenuation) reach as high as 2.5 p.u. value when a fault occurs far from the circuit breaker. However, practically surge arresters may be installed at this location to protect against such over-voltage. The difference between the two voltages appears as a stress to the current limiting reactor at CB7.

3.6 IMPACT OF CONVERTER BLOCKING

The impact of converter blocking depends on several factors, such as the strength of the AC network, the number of feeder cables connected at converter DC terminal and the size of arm reactors.

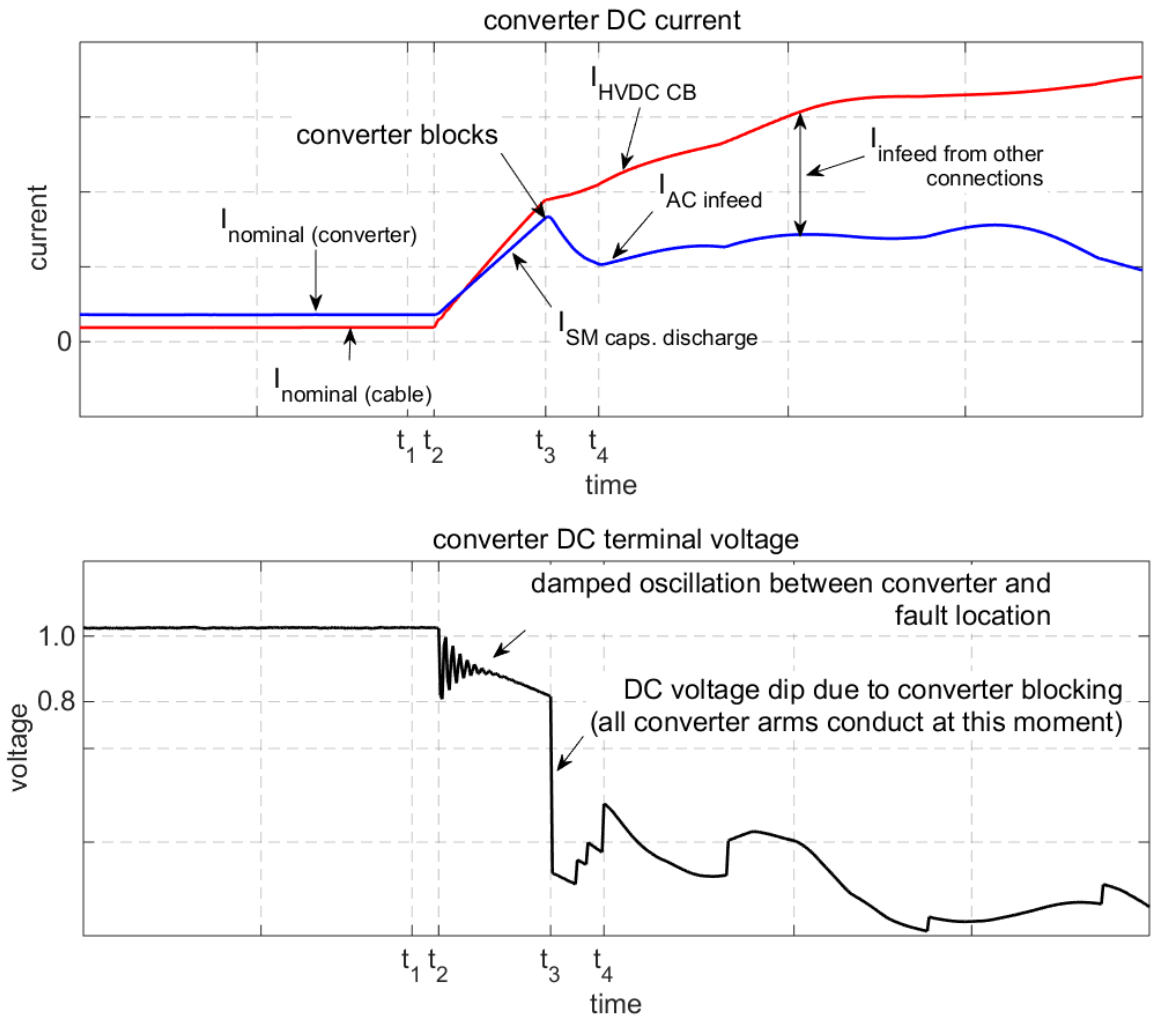

Figure 3-12: Impact of converter blocking on peak fault current [1].

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Figure 3-12 depicts the phenomena before and after converter blocking under fault condition. The top graph shows the currents measured at converter output (blue curve) and at a circuit breaker on a faulted cable (red curve). For demonstration purpose the circuit breaker does not interrupt in this case. Immediately following converter blocking (at t_3), there is a reduction in the rate of rise of fault current at a circuit breaker. This is because until the moment of blocking, the fault current is mainly supplied by the discharge of the converter submodule capacitors. Considering only the current measured at converter output, there is reduction in current contribution. This is since all the six arms of a converter are conducting simultaneously at t_3 and because of the arm reactors the current in each arm continue to flow through the freewheeling diodes until it decays to zero one after the other depending the magnitude of current and circuit time constant. This can be observed from the bottom graph of Figure 3-12 as a step changes in the DC voltage at converter terminal between t_3 and t_4. Thus, the AC side is momentarily decoupled from the DC side until the AC infeed through the rectifier (freewheeling diodes) fully takes over at t_4. Note that, the arm reactors result in commutation overlap and hence, three of the six converter arms conduct at any time even during the rectifier mode of operation. It is shown in D5.1 that the AC side fault current infeed is dependent on the strength of the neighbouring AC grid.

However, unlike the current measured at converter output (between t_3 and t_4), the current measured at circuit breaker is increasing although the rate of rise has slightly decreased. This is because of the fault current infeed from cables connected to the DC converter terminal. As the number of feeders connected to a converter DC terminal increase, the impact of converter blocking on fault current magnitude reduces.

Besides, it is preferable to clear the DC side fault rapidly even before any of the converters block so that the power flow to healthy parts of the system is not interrupted. For active injection type HVDC circuit breakers, with breaker operation time of 8 ms or longer, at least the converters directly connected to the faulted cable need to block, otherwise the converter cannot maintain controlled operation. The use of reactors in the range of 200 - 300 mH could ensure that each converter continues its controlled operation during the entire fault neutralization period. However, the impact of increased DC current limiting reactor on the controls of a converter as well as the losses associated with it need to be investigated.

3.7 FAULT CURRENT INTERRUPTION IN RADIAL MTDC NETWROK

Figure 3-13 shows a four-terminal radial HVDC network which was also used in deliverable D5.1 [1]. The system data for this network are provided in Table 3-3. The converter configuration of each station is symmetric monopole with high impedance grounding scheme. Since a pole-to-ground fault does not result in a significant overcurrent in such a system, a pole-to-pole fault at B-C/S terminal is applied and the simulation results are analysed for different system conditions. A model of the HVDC circuit breaker based active current injection scheme is inserted at each end of the DC lines. It is assumed that the protection system can correctly detect and locate the fault and hence, only the HVDC CBs connected at both ends of the faulted cable, in this case $DCCB_1$ and $DCCB_2$ are opened.

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In deliverable D5.1 (Figure 25 in [1]) it was demonstrated that, with an appropriate DC current limiting reactor, voltage can be maintained above 0.8 p.u. and the DC network can continue operating for up to 10ms. Therefore, for the studies in this section, a fault neutralization time (Figure 2-3) of 10 ms has been assumed.

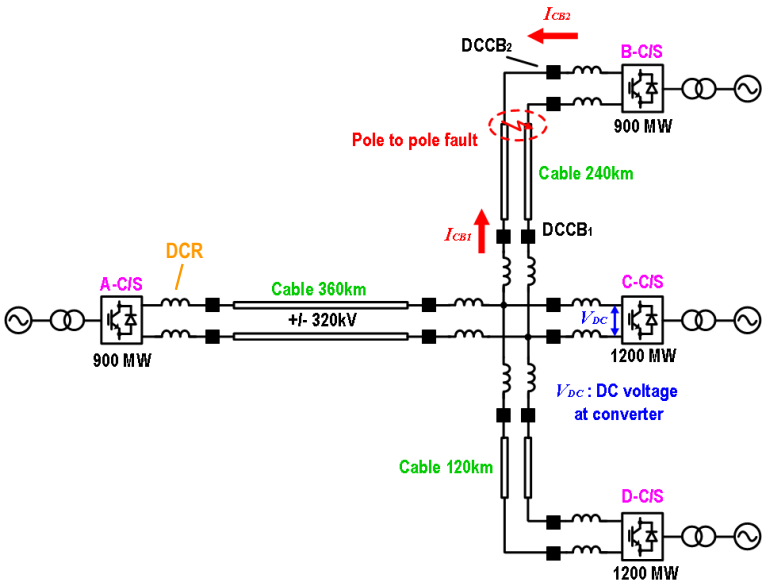

Figure 3-13: Four-terminal radial HVDC network model

Table 3-3: System parameters of four-terminal radial HVDC network

Parameter	A-C/S	B-C/S	C-C/S	D-C/S
DC voltage	+/-320 kV	+/-320 kV	+/-320 kV	+/-320 kV
Converter capacity	900 MVA	900 MVA	1200 MVA	1200 MVA
AC network voltage	400 kV	400 kV	400 kV	400 kV
AC network capacity	20000 MVA	8000 MVA	15000 MVA	15000 MVA
Transformer primary voltage	400 kV	400 kV	400 kV	400 kV
Transformer secondary voltage	320 kV	320 kV	320 kV	320 kV
Transformer leakage reactance	20%	20%	20%	20%
MMC arm inductance	10%	10%	10%	10%

The stresses on mechanical HVDC CBs at $DCCB_1$ and $DCCB_2$ are shown in the simulation results. Figure 3-14 shows the DC fault current behaviour for three different values of DCL (25 mH, 50 mH and 150 mH). Table 3-4 summarizes interruption current and the TIV for faults with different values of DCL. It can be seen from Figure 3-14 that the peak interrupted current decreases with increasing size of DCL.

For each simulation case, negative initial TIV is observed just after the interruption of current in the main interrupter. This initial TIV is due to the residual voltage of the capacitor in the injection branch of the breaker. Therefore, when interruption current is much smaller than rated interruption current of the HVDC CB, the residual voltage of capacitor is still high at current zero and initial TIV amplitude also becomes large (this is provided the main interrupter succeeds in the first zero crossing).

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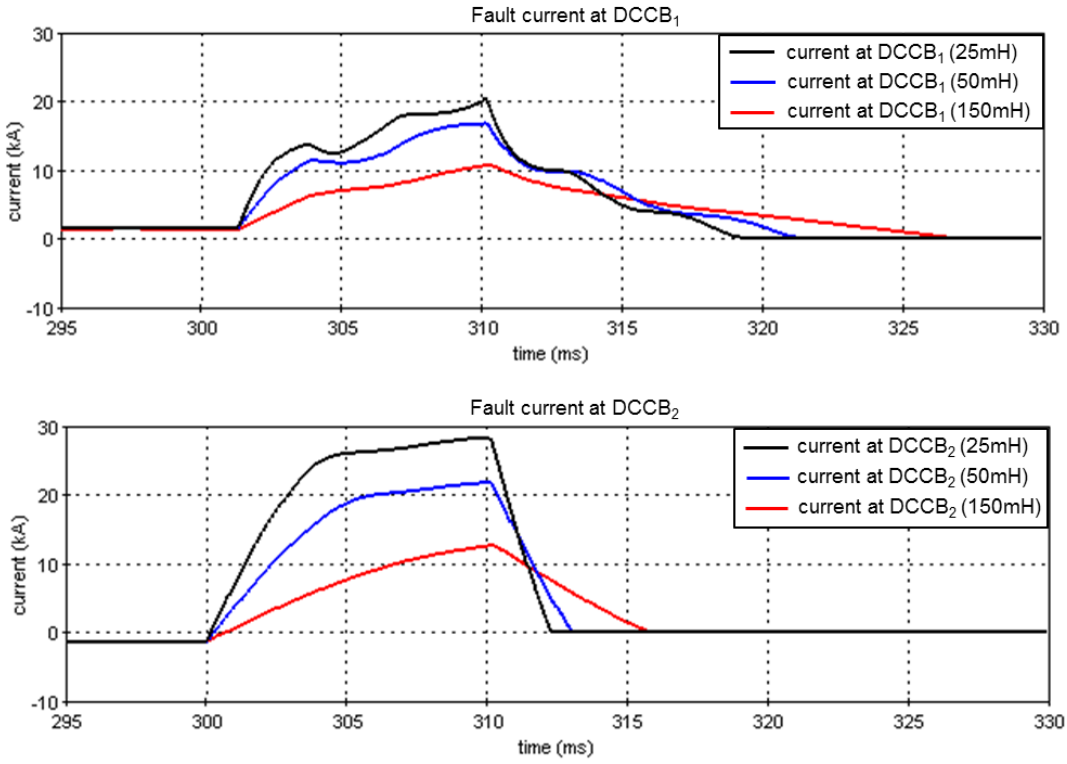

Figure 3-14 : Fault current behavior at each DCCB located at the ends on the faulted cable

Table 3-4: Interruption current and TIV for different values of DCL

$DCCB_1$ (central node side)			
DCL value	Interruption current	TIV dv/dt	TIV amplitude
25 mH	19.98 kA	2.53 kV/µs	521.1 kV
50 mH	16.70 kA	2.12 kV/µs	512.2 kV
150 mH	10.74 kA	1.33 kV/µs	497.2 kV

$DCCB_2$ (converter side)			
DCL value	Interruption current	TIV dv/dt	TIV amplitude
25 mH	28.17 kA	3.80 kV/µs	527.2 kV
50 mH	21.75 kA	2.92 kV/µs	522.2 kV
150 mH	12.65 kA	1.61 kV/µs	502.4 kV

Table 3-5 show the energy dissipated in the surge arresters of the HVDC CBs for different values of DCL. The energy dissipated in $DCCB_1$ (remote side from fault point) is larger as compared with $DCCB_2$ (near side from fault point) even if the interruption current of $DCCB_1$ is smaller than that of $DCCB_2$. This is because, while the surge arrester in $DCCB_1$ must dissipate all the energy from A, C and D-C/S, the surge arrester in $DCCB_2$ must dissipate only the energy from B-C/S due to the topology of the system.

Furthermore, it can be seen from Table 3-5 that the variation of the energy dissipation in the surge arrester does not change significantly (only by 13% for the simulated cases) when DC current limiting reactor value increases. The reason is that the interrupted current decreases as DC reactor size increases and the energy stored in the

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reactor changes nonlinearly with $\frac{1}{2}LI^2$. From these results, it can be said that the energy dissipated in the surge arresters of the HVDC CB is determined by not only interruption current but also system parameters and DC network topology.

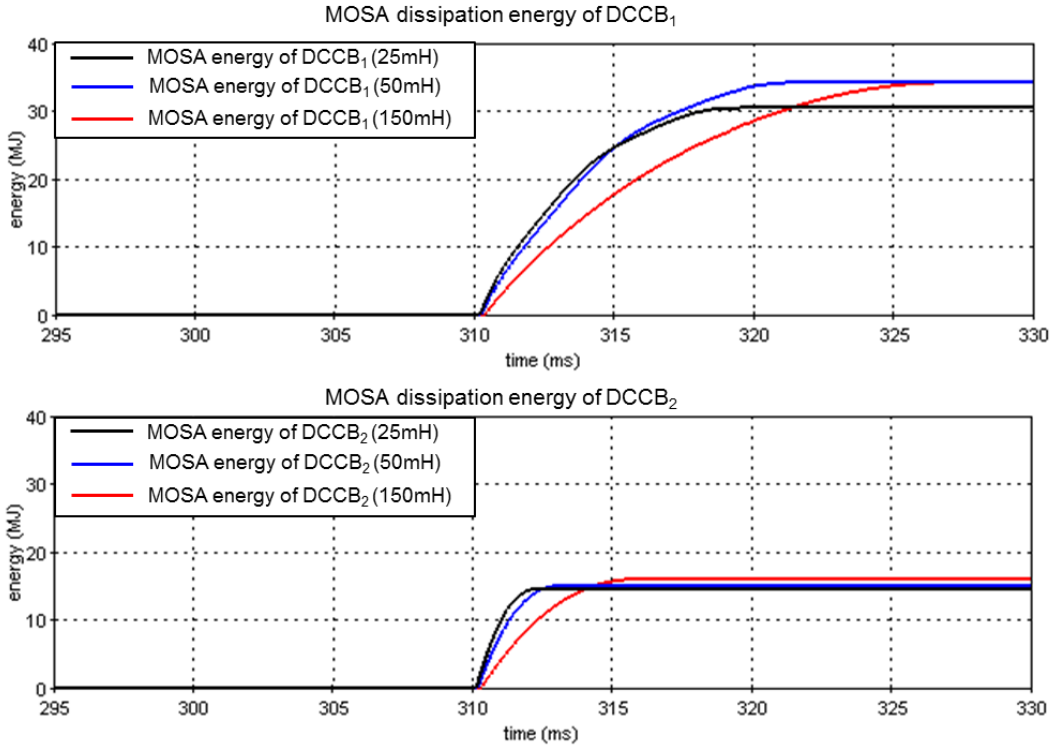

Figure 3-15 MOSA dissipation energy for each DCL condition

Table 3-5: MOSA dissipation energy for each DCL condition

$DCCB_1$ (central node side)		$DCCB_2$ (converter side)	
DCL value	MOSA dissipation energy	DCL value	MOSA dissipation energy
25 mH	30.5 MJ	25 mH	14.6 MJ
50 mH	34.2 MJ	50 mH	15.0 MJ
150 mH	34.2 MJ	150 mH	16.0 MJ

3.7.1 THE IMPACT OF DC CURRENT LIMITING REACTOR ON SYSTEM OPERATION

The simulation results in the previous sections show that by using additional DC current limiting reactor in the HVDC system, longer fault neutralization time can be achieved without voltage collapse at remote converter terminals from the fault location. However, the impact of DCL on HVDC system is also important and it should be investigated [9].

First, the impact of DC reactor on the power loss is briefly evaluated. For instance, a 1.2 GW, ±320 kV transmission capacity (C-C/S and D-C/S in Figure 3-13), the loss associated with a 150 mH DC reactor is approximately 0.04%, compared to the loss due to a converter (about 1 % - 12 MW [10]).

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Second, the impact of DC reactor on the converter control as well as on the overall stability of the system must be evaluated. The converter must maintain its submodule capacitor voltages within an acceptable range to continue its controlled operation. The lower voltage threshold is set by the ability of the converter arms to block current flowing from the ac side to the dc side in an uncontrolled manner (diode rectifier action, via the free-wheeling diodes). The upper voltage limitation is based on the rated voltage of the sub-modules cell capacitors. If sub-module voltage goes above or below these thresholds then the converter must immediately be blocked to protect the semiconductor devices, among other components. Sub-module capacitor voltage must therefore be kept within the design range to maintain control of the converter. The impact of DCL on this stability of the system is evaluated in [11]. It is shown in this reference that DCL less than 230 mH can be acceptable to HVDC system from point of view of over-voltage or under-voltage when AC side fault or rapid power flow change occurs. In addition, it is also possible to mitigate the impact of DCL on sub-module under- and over-charging by increasing the cell capacitor size.

3.7.2 IMPACT OF DC LINE TYPE

Simulation studies in the preceding sections are performed for a system interconnected via HVDC cables only; however, the stresses on HVDC CB in OHL system must also be investigated. Generally, the line impedance of an OHL is larger than that of a cable (keeping the same length) and this difference causes the variation of stresses on the HVDC CBs.

To compare the impacts of different transmission means, all the cables in the four-terminal radial HVDC system as shown in Figure 3-13 are replaced by OHLs while keeping the same length as cables. For simplicity, only DC reactor value of 150 mH is considered for comparison of both cable and OHL. All other system parameters are also kept the same as in the previous section. Figure 3-16 shows simulation results for both cable and OHL systems when a fault occurs at a long distance from a circuit breaker ($DCCB_1$) and close to a circuit breaker ($DCCB_2$). it can be seen from the figure that the current interrupted by $DCCB_1$ is lower for OHL system than the current interrupted by the same circuit breaker in cable system because of higher impedance of the OHL. However, the interrupted current by $DCCB_2$ is almost the same for both cable system and OHL system since the fault is applied close to this circuit breaker and the difference in the impedance up to the fault location is not significant.

Table 3-6 summarizes interruption current through the HVDC CB and TIV across the main interrupter for each type of transmission means. From this table, it can be concluded that under the assumed conditions both interruption current and TIV stress of HVDC CB in OHL system are generally less severe as compared with cable system.

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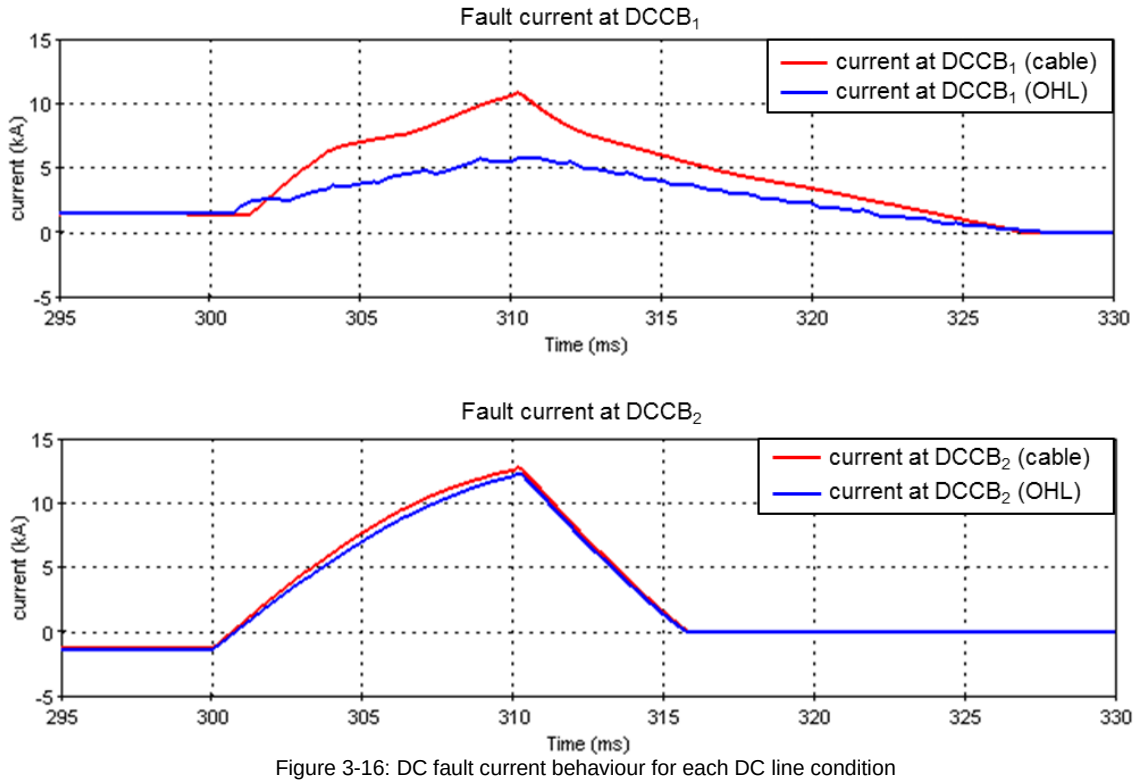

Figure 3-16: DC fault current behaviour for each DC line condition

Table 3-6: Interruption current and TIV for each DC line condition

DCCB1 (central node side)			
DC line type	Interruption current	TIV dv/dt	TIV amplitude
cable	10.74 kA	1.33 kV/µs	497.2 kV
OHL	5.46 kA	0.68 kV/µs	483.9 kV

DCCB2 (converter side)			
DC line type	Interruption current	TIV dv/dt	TIV amplitude
cable	12.65 kA	1.61 kV/µs	502.4 kV
OHL	12.06 kA	1.53 kV/µs	501.1 kV

Table 3-7 shows the energy dissipated in the MOSA of the active injection HVDC CB for each DC line types. Since interruption current is lower than that of cable system, the energy dissipated in the surge arrester when the system is interconnected by OHL is smaller than that in a cable system. In conclusion, DCCB stress in OHL system is less severe as compared to the case of a cable system.

Table 3-7: MOSA dissipation energy for each DC line condition

DCCB1 (central node side)		DCCB2 (converter side)	
DC line type	MOSA dissipation energy	DC line type	MOSA dissipation energy
cable	16.0 MJ	cable	34.2 MJ
OHL	15.1 MJ	OHL	20.7 MJ

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4 DISCUSSION

4.1 STRESS ANALYSIS

To stress the HVDC CB as in service, a test circuit must ideally produce a current envelope while maintaining the driving voltage. This implies that megawatts are needed to test HVDC CBs, while megaVArs are sufficient to test AC CBs. This comes at a price, since large active power is more costly to generate than reactive power.

To determine the test current envelope, the following parameters are important:

1. The system voltage for which the breaker is designed for
2. The total internal current commutation time (the time from trip order until the current is commutated to energy absorption branch). At commutation, the circuit breaker must be able to withstand the voltage about 1.5 times the rated voltage of the system
3. The maximum current interruption capability (the peak fault current that a circuit breaker is capable of handling).

The latter two parameters are important to determine the average rate of rise of the fault current envelope (di/dt) that a circuit breaker can deal with. The first parameter is important to determine the DC current limiting reactor that must be used to limit the rate of rise of current within the interruption capability of a circuit breaker. Assuming t_1, the total time required for internal current commutation, and I_p the peak value of current that a circuit breaker can interrupt and U_{DC} is the system voltage, the value of the DC current limiting reactor that is necessary for the proper operation of a given circuit breaker can be computed as follows:

$$\frac{di}{dt} = \frac{I_P}{t_1}$$

$$L_{DC} = \frac{1.1U_{DC}}{di/dt} = 1.1U_{DC}\frac{t_1}{I_p}$$

Assuming 10% overvoltage in the system [4].

4.1.1 VOLTAGE STRESSES

An HVDC circuit breaker generates a voltage higher than the system voltage in order to suppress the fault current to the residual current value. Thus, the maximum voltage stress depends on the protection level of the surge arresters installed as part of the breaker. The rate of rise of this voltage is dependent on the type of circuit breaker technology under consideration. It is determined by the size of capacitors and reactors in the active counter current injection branch for active injection circuit breaker, and the snubber circuits associated with the power electronics elements in the hybrid HVDC circuit breakers. However, for all the cases, the circuit breaker is subjected to the system voltage after the current interruption process. This assuming the residual current breaker clears on the first zero after the fault current is suppressed.

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Thus, the rate of rise voltage (du/dt) and the maximum voltage across the circuit breaker terminals are dependent on the circuit breaker parameter designs. The grid has little impact on these stresses during the current interruption process. However, the dielectric stress after successful interruption depends on the superposistion of the system voltage and the travelling waves not completely damped yet.

4.1.2 CURRENT STRESSES

The stress resulting from high di/dt can be controlled by using a DC current limiting reactor. As described in Section 4.1, large di/dt can be handled by very fast circuit breakers if the peak fault current does not exceed the maximum current interruption capability. The overall di/dt depends on the distance of the fault from a converter station as well as on the number of feeders connected to the bus close to the circuit breaker. Also, the type of transmission, namely, cable or overhead line, has a strong impact on di/dt.

It must be noted that the di/dt which the internal components of a circuit breaker can withstand is far higher than the di/dt of the fault current especially when DC current limiting reactors are used. The di/dt provides additional information to the maximum current interruption capability and the internal current commutation time of the circuit breaker.

For some types of HVDC circuit breakers, interrupting high current might be easier than interrupting low currents. Therefore, interruption tests of circuit breakers from load current up to the maximum current must be carried out, like AC CBs.

4.1.3 ENERGY STRESSES

Since the different types of HVDC circuit breaker technologies have different internal current commutation times, DC side reactors of various sizes are used to limit the fault current within interruption capability of the circuit breaker. However, this has a strong implication not only on the energy that the circuit breaker must absorb, but also on the total current breaking time, i.e. the time from trip order until the fault current is reduced to a leakage value. In a similar manner as it determines the rate of rise of fault current, the DC current limiting reactor determines also the rate at which the fault current is suppressed during the energy absorption phase of the interruption process as shown by the following expression.

$$\frac{di}{dt} = \frac{U_{DC} - U_{CB}}{L_{DC}}$$

Where, U_{CB} is the voltage across the circuit breaker during the energy fault current suppression time and U_{DC} is the instantaneous value of the driving voltage or the DC bus voltage during fault current suppression period. L_{DC} is the total circuit inductance between the DC bus and the fault location. Note that the d*i*/d*t* is negative since $U_{CB} > U_{DC}$ and therefore, the DC current limiting reactor (L_{DC}) determines the rate of decay of the fault current as well.

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Hence, the exact time at which the current is suppressed to zero (residual current value) in DC current interruption depends on several factors such as protection level of the surge arrester, the magnitude of the system voltage, the system inductance, the total resistance in the circuit and the peak value of the interrupted current. The total time needed for energy absorption is approximated by the following equation [12],

$$t_s = \frac{L_{DC}}{R} ln\left[1 + \frac{R}{U_{CB} - U_{DC}} I_P\right]$$

Assuming negligible resistance in the circuit and constant surge arrester voltage (U_{CB}), the above equation can be simplified to

$$t_s = L_{DC}\left(\frac{I_P}{U_{CB} - U_{DC}}\right)$$

Where, t_s is the total time required by the surge arrester to suppress the peak fault current (I_p) to zero (a small leakage current).

Thus, the total energy absorbed by the circuit breaker is,

$$E_{CB} = \int_0^{t_s} (U_{CB} \cdot i) dt$$

Closely examining the total energy dissipated in the HVDC CB and assuming negligible energy loss in the circuit resistance, there are two principal sources of energy; the first is the magnetic energy stored in the system inductance ($\frac{1}{2} L_{DC} I_P^2$) and the electrical energy contributed from the nearby converters and feeders. The latter is the energy flowing from the DC busbar into the fault location through the breaker. This energy can be expressed as follows,

$$E_{DC,Bus} = \int_0^{t_s} U_{DC} * i(t) dt$$

This represents the entire energy contributed by the other parts of the system, except the energy stored in the DC current limiting reactor. From the simulation results of Chapter 3, it is observed that the DC busbar voltage recovers at the end of the fault current neutralization period. If the converter does not block, this voltage is the same as the output voltage of the converter connected to the busbar or otherwise it becomes the rectified AC voltage in case the converter blocks. This reduces the design of HVDC circuit breaker test circuits to three important parameters.

1. Current limiting reactor (L_{DC})
2. Voltage (both system voltage U_{DC}, and circuit breaker voltage U_{CB})
3. The peak fault current (I_p)

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Indeed, the internal current commutation time must be defined as a circuit breaker parameter, since it determines how the peak current must be achieved. However, in a test circuit using a single source, achieving these parameters while keeping the desired di/dt, especially considering HVDC circuit breakers with long internal current commutation time becomes challenging.

4.2 REQUIREMENTS ON CLEARING TIME

Factors determining this are speed of protection system (relaying time), the speed of HVDC circuit breaker, the system requirements such as under voltage beyond which the system cannot operate, etc.

4.3 TEST REQUIREMENTS

The system simulation studies shed light on the requirements of test circuits of HVDC circuit breakers. The DC current liming reactors bridge the gap between HVDC circuit breaker capabilities and the HVDC grid fault current response. Considering the breaker operation times of the recently developed HVDC circuit breakers, different sizes of the DC current limiting reactors must be used. Although so much depends on the system under consideration, the choice of the size of DC current limiting reactor must ensure the following important points

i. For any DC side fault, the magnitude of fault current through the circuit breaker at the end of fault neutralization period must not exceed the maximum interruption capability of the circuit breaker under consideration
ii. The converters on the healthy side must be able to continue their controlled operation. Thus, the DC voltage of the healthy part must not drop below the threshold value for continued controlled operation.

Figure 4-1 shows generic test requirement for HVDC circuit breaker. Note that each of the parameters depicted on the graph are dependent of the type of the circuit breaker. Considering the currently developed HVDC circuit breakers, the key design parameters a test circuit needs to be able to verify are:

1. Capability to create a local current zero without restrike/breakdown of mechanical switches/interrupters or thermal overload of power electronic components at rated DC fault current capability
2. Generation of sufficient counter voltage to initiate fault current suppression
3. Capability of energy absorption components to absorb energy during fault current suppression wave trace as in service. Depending on the rated sequence, this capability must be demonstrated several times within a defined sequence.
4. Capability to withstand the rated DC voltage for a certain duration after the interruption process
5. The breaker operation time: the minimum time at which the circuit breaker reaches the TIV withstand level after trip order
6. The maximum current interruption: The maximum current the breaker can interrupt within the breaker operation time (from t_2 until t_3)
7. The maximum energy that the circuit breaker can dissipate during fault current interruption

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8. The number and frequency of operation: the number of interruption operations that the circuit breaker can perform before thermal run away occurs on its surge arresters. The interruption interval needs to defined, e.g. like auto reclosure in AC circuit breakers
9. Dielectric withstand to ground, also during incident of superimposed travelling waves

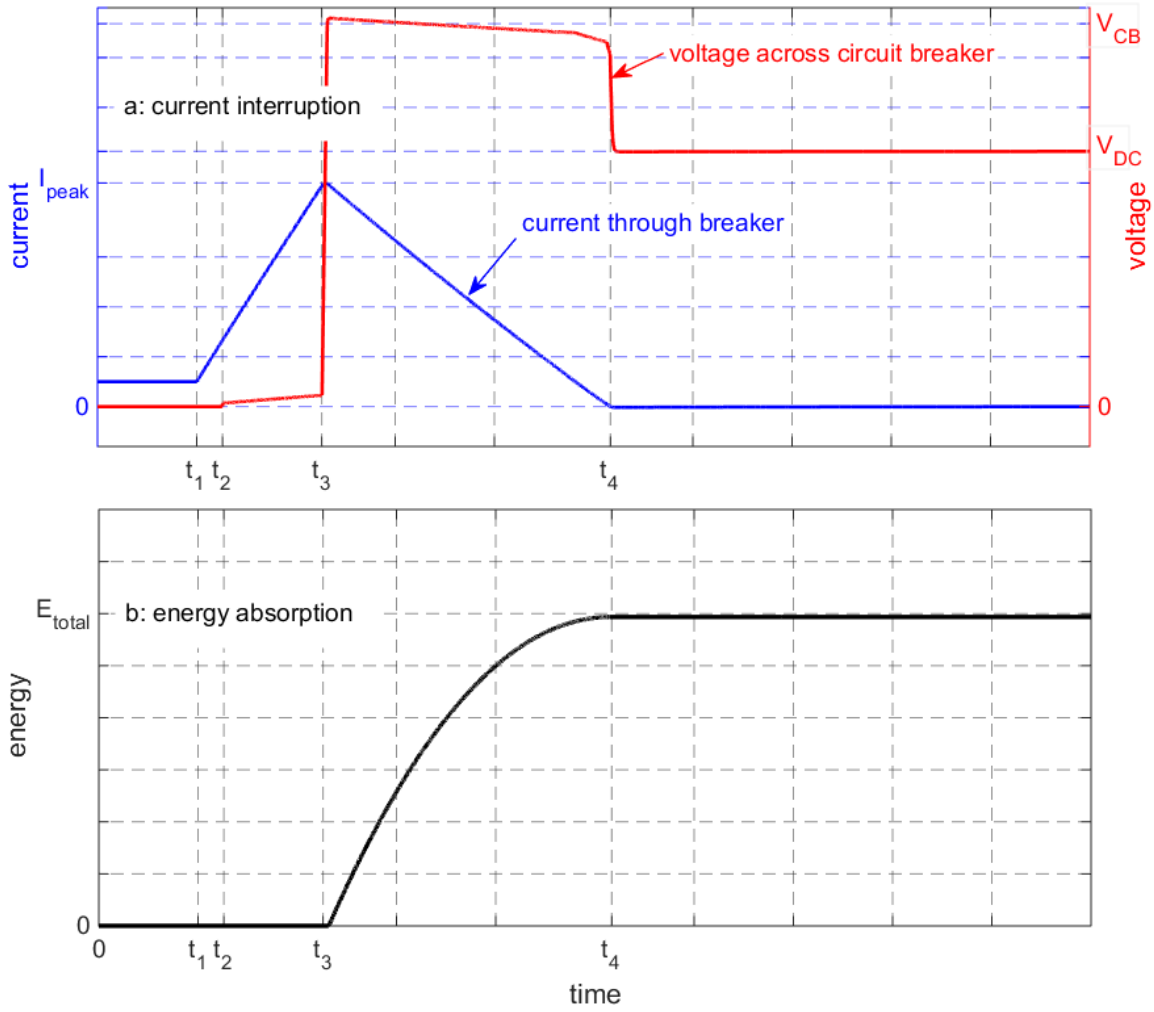

Figure 4-1: Generic graph showing test requirements for HVDC circuit breakers. Top graph: current interruption capability, bottom graph: energy absorption capability

It must be noted that when testing ac circuit breakers, it is critical that the TRV is imposed on the circuit breaker by the test circuit. However, for dc circuit breakers the TIV is self-imposed. Therefore, the test circuit is not required to generate this except after current interruption as mentioned in point (4) above.

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Table 4-1: Summary of test parameters for HVDC circuit breakers

Circuit breaker type	Breaker operation time (ms)	Peak interruption current (kA)	Total energy absorbed (MJ)	Maximum current interruption capability
Active current injection	8	12	25	16
Hybrid type I	2	8.3	10	16
Hybrid type II	2	8.1	10	-

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5 CONCLUSIONS

- The magnitude and rate of rise of fault current in the HVDC grid depends on the system topology and parameters.
- The gap between the maximum current interruption capability of a circuit breaker and the system fault current response can be bridged by proper design of DC current limiting reactor. Thus, with the proper choice of current limiting reactor, the HVDC circuit breakers must be designed for handling the worst-case fault condition in terms of the maximum current interruption and maximum energy absorption capability.
- In general, a fault at converter terminal presents the most difficult condition to a circuit breaker in terms of the maximum current interruption as well as the energy dissipation. Especially, a fault at a converter delivering the high power to the rest of the grid and having multiple connection results in the highest rate of rise. Among the connections at converter DC terminal, the link having highest steady state current results in the maximum fault current at the end of fault neutralization time
- During a fault current interruption by an HVDC circuit breaker, the system voltage restores before the fault current is completely cleared. The voltage recovery process starts the moment the circuit breaker begins to generate the counter voltage
- During the fault current suppression period, the HVDC circuit breaker needs to absorb the magnetic energy in the system inductance. Because of the restored system voltage, the circuit breaker must also absorb significant amount of electrical energy coming from the system in the meantime.
- After current is successfully interrupted, the circuit breaker is subjected to the dielectric stress from the system voltage. Depending on the total interruption time of the breaker and the length of cables in the system, there can be higher dielectric stress imposed due to superimposed travelling waves on the system voltage.
- The HVDC circuit breaker needs to be tested for a range of values up to maximum current interruption and maximum energy absorption as well as with proper dielectric stress

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6 APPENDIX

A. WP5 BENCHMARK STUDY GRID DATA

The hypothetical five-terminal meshed offshore HVDC network shown in Figure 6-1 is used as a benchmark network for the study of various fault conditions in this project. All converters are bipole converters with earth return and solid earthing at each converter. The system data for this network is adopted and modified from the DC test network developed by CIGRE WG B4-57 and WG B4-58 [13]. Three of the five terminals namely, C2, D1 and D2 are assumed to be located offshore and are interconnected via submarine cables with radial arrangement. Two converter terminals, namely, A1 and B1 are located onshore and receive power from the offshore network via three DC cables as shown in the Figure 6-1. All converters are of the modular multi-level (MMC) type with half bridge submodules.

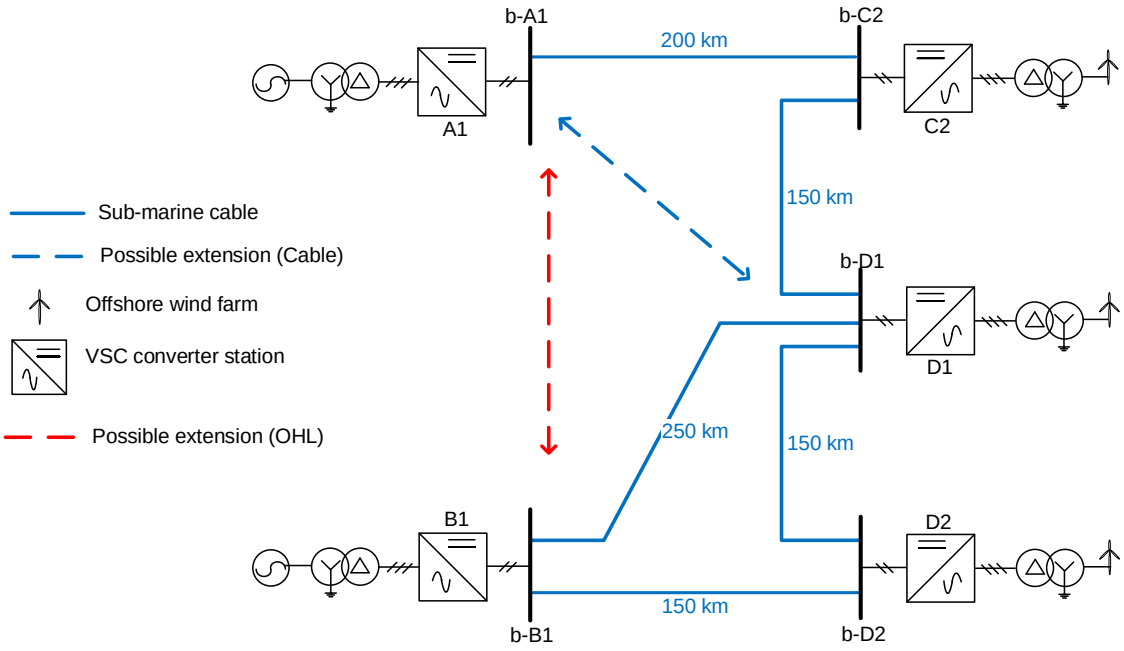

Figure 6-1: Five terminals meshed bipole HVDC Network. C2, D1 and D2 are offshore bipole converters

Network meshing is applied to provide more reliability by ensuring availability of alternative transmission paths of sufficient ampacity in case of a fault in any of the offshore DC links. In other words, unless the fault is within one of the offshore converters itself, a fault on any one of the DC links must not result in the shutdown of one or more of the offshore wind farms. Additional cable links (shown by the blue dotted arrow), and an additional overhead line (shown by the red dotted arrow), can also be connected for further reliability and network

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expansion. Table 6-1 and Table 6-2 show the details of the converter parameters for the network topology of Figure 6-1. In this network a disconnection of any of the links does not result in overloading of the healthy links.

Table 6-1: Converter parameters

Parameter	C-A1	C-B1	C-C2	C-D1	C-D2
DC Voltage (kV)	±320	±320	±320	±320	±320
Converter capacity (MVA per pole)	800	800	400	800	600
AC short circuit power (GVA at PCC)	30	30	3.8	3.8	3.8
Converter transformer primary voltage (kV)	380	380	145	145	145
Converter transformer secondary voltage (kV)	220	220	220	220	220
Transformer leakage reactance	18%	18%	18%	18%	18%
Transformer series resistance	0.6%	0.6%	0.6%	0.6%	0.6%
Conduction losses in arm reactor and converter valves	0.3%	0.3%	0.3%	0.3%	0.3%
Arm reactance	15 %	15 %	15 %	15 %	15 %
Control mode	DC and AC voltage	PV droop	Active and reactive power	Active and reactive power	Active and reactive power

Table 6-2: Converter and system configuration

Converter Type	VSC
Converter Topology	HB-MMC
Number of SMs per arm	160
Converter Model	Detailed Equivalent Model
Modulation technique	NLC (Nearest level control)
Converter Configuration	Bipole (low impedance grounded)
DC reactor	150 mH

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B. CABLE PARAMETERS

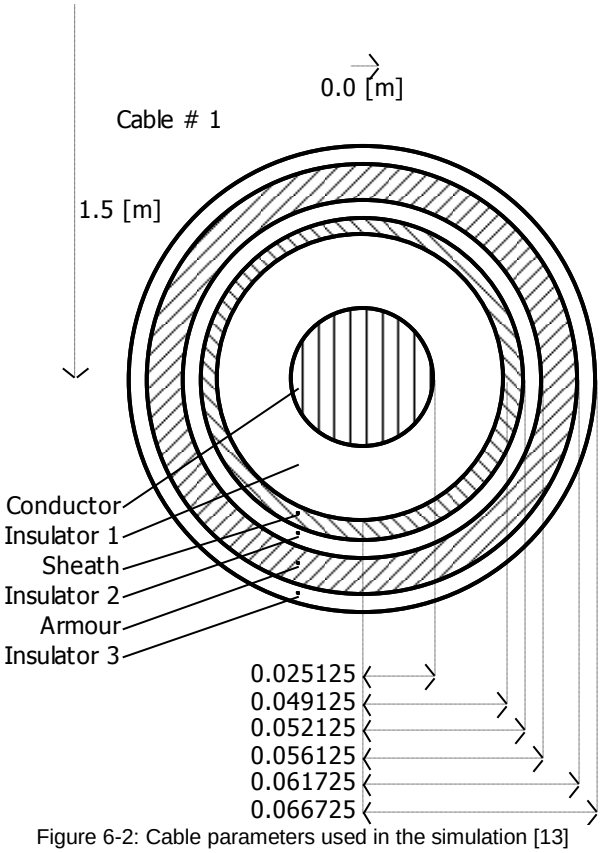

Figure 6-2: Cable parameters used in the simulation [13]

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