PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

D5.7 Realization of Test Environment for HVDC Circuit Breakers

PROMOTioN – Progress on Meshed HVDC Offshore Transmission Networks
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CONTENT

EXECUTIVE SUMMARY

The relative immaturity of HVDC circuit breaker technology and the absence of standardised testing requirements and testing methods are some of the key challenges to the realization of a meshed HVDC transmission network. Work package 5 of the 'Progress on Offshore Meshed HVDC Transmission Networks' (PROMOTioN) project aims to address this challenge by realising a test environment for HVDC circuit breakers. The test environment includes test requirements based on the stresses that occur during DC fault current interruption, test procedures and a high-power test circuit which can provide the test requirements. The ultimate deliverable of work package 5 is a realisation of a test circuit capable of delivering current, energy and voltage stresses in a safe and controlled way. The test circuit is based on reduced frequency AC short-circuit generators and has been realised in DNV GL's KEMA Laboratories.

In this deliverable, the realisation of the reduced frequency AC short-circuit generators based test circuit at KEMA Laboratories is described. A method for tuning the test circuit's variables to achieve the required current and energy test stresses is presented. The implementation of overvoltage and overcurrent protection methods is explained, as well as methods to realize dielectric stress after current suppression. A test program aimed at validating the test circuit's ability to meet the requirements is provided. Test results of prospective current tests, overcurrent and overvoltage protection tests, and of dielectric stress application tests are provided. Simulation results of HVDC circuit breaker models are superimposed onto the experimental results to illustrate the ability of the test circuit to synthesize realistic stresses.

LIST OF CONTRIBUTORS

The names of the partners, who contributed to the present deliverable, are presented in the following table.

PARTNER	NAME
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NOMENCLATURE

ABBREVIATION	EXPLANATION
AC	Alternating Current
CB	Circuit Breaker
D5.3	Deliverable 5.3 (PROMOTioN deliverable)
HVDC CB	Direct Current Circuit Breaker
DCL	DC Current Limiting Reactor
FB	Full Bridge
HB	Half Bridge
HVAC	High voltage AC
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
ITIV	Initial Transient Interruption Voltage
LCC	Line Commutated Converter
MMC	Modular Multi-Level Converter
MTDC	Multi-Terminal HVDC
NLC	Nearest Level Control
OHL	Overhead Line
PCC	Point of Common Coupling
TIV	Transient Interruption Voltage
ITIV	Initial Transient Interruption Voltage
VSC	Voltage Sourced Converter
WP	Work Package
LCS	Load commutation switch
UFD	Ultra-fast disconnector
RCB	Residual current breaker
MOSA	Metal oxide surge arrestor
TO	Test Object
AB	Auxiliary Breaker

2 INTRODUCTION

The relative immaturity of HVDC circuit breaker technology and the absence of standardised testing requirements and methods to validate their ratings and functionality are some of the key challenges to the realization of a meshed HVDC transmission network. Work package 5 of the 'Progress on Offshore Meshed HVDC Transmission Networks' (PROMOTioN) project aims to address this challenge by developing a test environment for HVDC circuit breakers. The test environment will be used to demonstrate the performance of HVDC circuit breakers from Mitsubishi Electric, SCiBreak and ABB in work package 10. A test environment includes test requirements based on the stresses that occur during DC fault current interruption, test procedures and a high-power test circuit which can provide the test requirements. The ultimate goal of work package 5 is the realisation of a test circuit capable of delivering current, energy and voltage stresses in a safe and controlled way. The test circuit is based on reduced frequency AC short-circuit generators and has been realised in DNV GL's KEMA Laboratories.

To define test conditions and test requirements, and characterize suitable test circuits, several studies have been conducted in previous deliverables of WP5:

D5.1	Fault Analysis of HVDC Network
D5.2	HVDC circuit breaker modelling and analysis
D5.3	Fault Stress Analysis of HVDC circuit breakers
D5.4	Test Requirement Specification
D5.5	Definition of test procedures
D5.6	Characterization of candidate test-circuits for HVDC circuit breaker testing

For testing HVDC circuit breakers, theoretically, various test circuits based on different sources can be designed to fulfil the required stresses as discussed in deliverable 5.6 of PROMOTioN [1]. However, AC short circuit generators, which are already in use for testing of AC switchgear, can be used for testing HVDC circuit breaker without significant additional investment. Therefore, the latter is chosen for the test of HVDC circuit breakers in the PROMOTioN project and test circuits that will be used for the demonstration of HVDC CBs in WP10 are designed accordingly. Thus, this deliverable completes WP5 by demonstrating that a test circuit designed based on AC short-circuit generators running at reduced power frequency can supply the required stresses. In this case the main goal is to practically investigate, on one hand, the impact of such a test on the test installation which includes power transformers, AC switchgear as well as the AC short-circuit generators used for this purpose. On the other hand, the deliverable demonstrates whether the necessary stresses for testing HVDC circuit breakers can be supplied by short circuit generators running at reduced power frequency.

2.1 MOTIVATION

Prior to operation, like any power component, the ratings and functionality of HVDC circuit breakers must be verified by means of high power testing, preferably at an independent accredited laboratory. As HVDC circuit breaker technology is still relatively immature, no standardised testing requirements, testing methods and test circuits exist. Several different types of testing circuits have been used by manufacturers. Work package 5 has proposed testing requirements for HVDC circuit breakers, and shown that AC short-circuit generators operated at a reduced frequency can perform as well or better than alternative test methods such as charged capacitor based circuits, especially concerning the ability to directly test the energy dissipation rating of a HVDC circuit breaker. As many independent test labs across the world have AC short-circuit generators as part of their AC equipment testing facilities, the proposed method could potentially be used at minimal additional expense to test HVDC circuit breakers, eventually leading to a cost saving.

In work package 10 of PROMOTioN, different types of HVDC circuit breaker prototypes will be tested with full power DC fault current interruption tests using a reduced frequency AC short-circuit generator based test circuit. Because little experience exists with this method, thorough validation of the test circuits ability to safely and precisely apply test stresses is necessary.

2.2 PURPOSE

This deliverable describes the realisation and demonstration of the reduced frequency AC short circuit generator based HVDC circuit breaker test circuit. It is shown how the variables of such a circuit can be tuned to achieve the required current, energy and voltage stresses. A description of the realisation of the test circuit at DNV GL's KEMA Laboratories is provided along with a test plan aimed at validating the test circuit's performance. Finally, the test results are shared, including DC fault current interruption tests of a Mitsubishi Electric mechanical HVDC circuit breaker with active current injection, illustrating the successful demonstration of the test environment. Simulation results are superimposed onto experimental test results where necessary to extend the demonstration to hybrid HVDC CBs.

2.3 DOCUMENT OVERVIEW

The remainder of this document is organised as follows. In Chapter 3 a recap of the test requirements for HVDC circuit breakers from deliverables D5.3 and D5.4 is provided. A description of how these requirements can be achieved with the AC short circuit generator based test circuit variables is given. An overview of the laboratory equipment available at KEMA Laboratories which is used in the realisation of the test circuit is provided in Chapter 4. Chapter 4 lists the tests and acceptance criteria which are necessary for the validation of the test circuit. The demonstration test results are combined with simulation results are provided and finally concluding remarks are provided in Chapter 6.

3 DESIGN OF AC SHORT-CIRCUIT GENERATOR BASED TEST CIRCUIT

Before discussing HVDC circuit breaker test requirements, a few important timing definitions related with the operation of HVDC CB as presented in [2] are provided. **Fault neutralization time**– the time interval between fault inception and the instant when the fault current starts to decrease, **breaker operation** time– time interval between the reception of the trip order and the beginning of the rise of the transient interruption voltage (TIV) and **fault current suppression** time– time interval between the peak fault current and the instant when the current has been lowered to leakage current level. **Transient interruption voltage (TIV)**- the voltage that a circuit breaker develops (appears across the circuit breaker terminals) during current interruption. These terminologies are described in detail also in previous PROMOTioN deliverables [3].

3.1 TEST REQUIREMENTS OF HVDC CIRCUIT BREAKERS FOR CURRENT INTERRUPTION

The important aspects of HVDC CBs that are to be demonstrated in the PROMOTioN project are current interruption capability within a specified breaker operation time, energy absorption capability as well as voltage withstand capability (both during and post current interruption). Thus, within the breaker operation time, a test circuit needs to supply current up to the maximum breaking capability of the HVDC CB. So far the prototyped HVDC CB technologies have breaker operation time ranging between 2–10 ms with a module voltage rating in the range of 40–120 kV [4], [5], [6], [7]. It is expected that several breaker units (modules) are put in series to achieve full pole voltage rating. Each breaker module interrupts the same current magnitude whereas the energy absorption and the TIV is shared among the series connected modules. For example, the solid traces in Figure 3-1 show fault current interruption simulation results of a meshed HVDC network described in deliverable 5.3 [3]. A test circuit designed based on low frequency AC short-circuit generator (running at 16.67 Hz) is used in this case to synthesize these resulting stresses. Simulation results of the test circuit for a single 80 kV breaker module of active injection mechanical HVDC CB are superimposed in Figure 3-1 (the dashed curves in part a and b). The simulation assumes equal sharing of voltage as well as equal sharing of energy among breaker modules. The peak value of the interrupted current is 11 kA in both system simulation and test circuit simulation.

The other important aspect that needs to be tested is the energy absorption capability of the breaker. From system simulation studies in deliverable 5.3 [3], it is observed that the HVDC CB needs to absorb several MJs of energy. The HVDC CB has the duty to absorb the magnetic energy stored in the current limiting reactor as well as the electric energy injected from the rest of the system during fault current suppression period. In Figure 3-1b the energy absorbed by a single module of 80 kV, HVDC CB in a test circuit simulation is superimposed on to the energy that a full-pole HVDC circuit breaker absorbs in a system simulation. The single module of a breaker absorbs about a quarter (4.5 MJ) of the total energy absorbed in a system simulation.

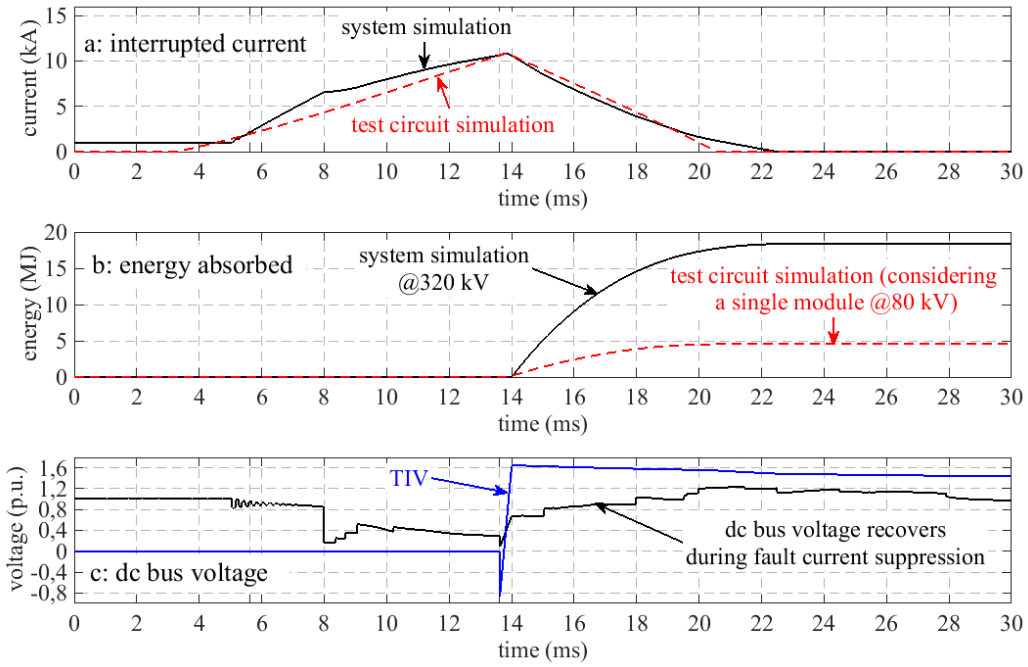

Figure 3-1: Comparison of DC fault current interruption by active current injection HVDC CB. Solid lines depict system simulation results, dashed lines show test circuit simulation results a: interrupted current, b: energy absorbed, c: transient interruption voltage (TIV) and dc bus voltage.

HVDC CBs generate the TIV which is higher than the system voltage to suppress the fault current to the residual current value. Hence, the maximum voltage stress depends on the protection level of the surge arresters installed as part of the breaker. The rate of rise of the TIV is dependent on the type of HVDC CB technology under consideration. It is determined by the size of the capacitor in the injection circuit in an active current injection HVDC CB, and the snubber circuits of the power electronic elements in a hybrid HVDC CB. Therefore, the rate of rise of TIV (dv/dt) and its maximum value are dependent on the CB parameters. Nevertheless, the generation of the TIV by a HVDC CB must be verified during a test. In addition, a complete test requires post interruption voltage withstand capability. Thus, it is necessary to ensure the application of dielectric stress after current interruption.

3.2 DETERMINATION OF AC SHORT-CIRCUIT GENERATOR BASED TEST CIRCUIT PARAMETERS

When using AC short-circuit generators for testing HVDC circuit breakers, there are several parameters which need to be precisely set to achieve the desired stresses for a given test duty. These parameters are:

- Source voltage
- Frequency
- Short-circuit making angle (point on voltage wave at which short circuit is made)

- Circuit inductance: when using AC sources there is always a minimum inductance in the circuit; however, parallel combinations of generators and transformers can be used to reduce this inductance further

Given the frequency (f), circuit inductance (L), making angle (θ) and voltage magnitude of the generator/back e.m.f. ($\hat{V}$), the prospective current (assuming no initial current flow) can be computed from the following mathematical equation,

$$i(t) = \frac{\hat{V}}{|Z|}\left[\sin(\omega t + \theta - \varphi) - \sin(\theta - \varphi)e^{-t/\tau}\right] \quad (1)$$

Where, $\varphi = \tan^{-1}\left(\frac{\omega L}{R}\right)$ is the power factor of the test circuit and $\tau = \frac{L}{R}$ is the circuit time constant. $|Z| = \sqrt{R^2 + (\omega L)^2}$ is the magnitude of the total impedance in the test circuit.

Thus, to achieve certain desired prospective current, a test circuit design procedure involves determining the source voltage, calculation of the necessary impedance in the circuit, setting suitable frequency and determining the making angle (considering supply frequency and fault neutralization period). The impedance is mainly inductive and is needed to store energy during the fault current neutralization period. The source voltage ensures sufficient di/dt during the fault current neutralization period as well as energy supply during the current suppression period. The impedances are distributed among generator sub-transient reactance (X_d''), transformer leakage reactance (X_T) and rail impedances as well as additional adjustable reactors that can be put in series across each phase of a generator (X_{add}), see Figure 3-2. These impedances are all taken into consideration for calculating the total equivalent inductance at the test object. The additional adjustable reactors are used in case the combined impedances of the generators, transformers and the rail cannot make the desired total impedance to limit the current per generator to a desired value.

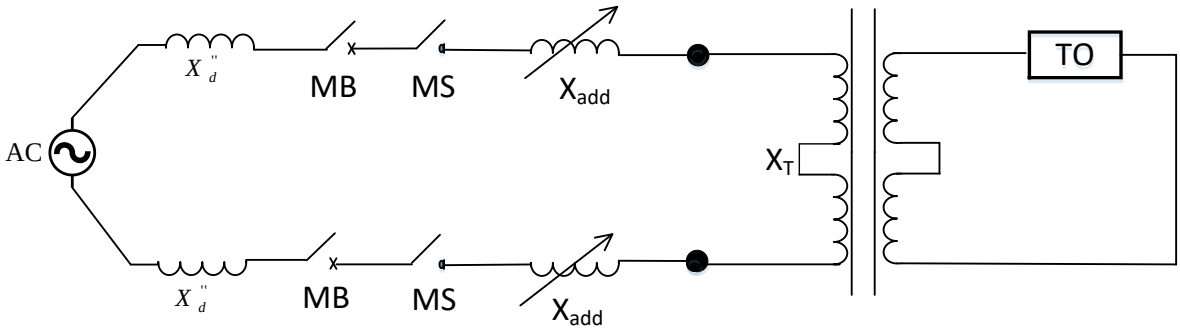

Figure 3-2: Short circuit generator together with step-up transformers and associated components (for single phase testing)

As a rule of thumb, the peak value of the source voltage is set to the rated voltage of the test breaker (module) for which it is intended. The desired voltage can be precisely tuned first by transformation ratio and then by generator excitation control. The impedance and the making angle are adjusted so that the rising current (di/dt), for a given test duty, fits within the fault current neutralization period (t_{FN}).

In general, the average di/dt during the fault neutralization time, is given by

$$\left(\frac{di}{dt}\right)_{ave} = \frac{\hat{V}}{X_{\min}} \frac{\left[\cos(\theta) - \cos(\omega t_{FN} + \theta)\right]}{t_{FN}} \quad (2)$$

Where,

- $\hat{V}$ the peak value of the AC voltage
- ω is angular frequency of the generator
- X_{min} the minimum impedance in the circuit
- t_{FN} fault neutralization time
- θ making angle

As mentioned earlier, there is a minimum impedance in the circuit due to the sub-transient reactance of the generators, the leakage impedance of the step-up transformers and any additional reactances for limiting generator current to ensure there will be no overcurrent damage to the master breaker (MB, see Figure 3-2) of the generators.

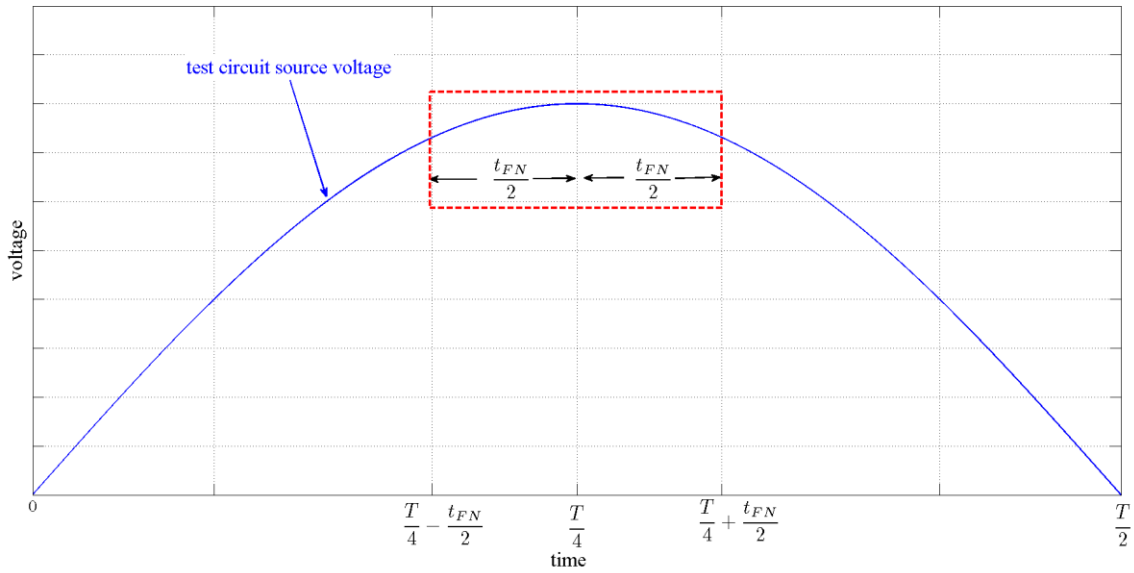

Figure 3-3: The making angle for maximum di/dt within a given fault neutralization period (t_{FN})

Notes:

From the Equation (2), the optimum making angle (θ) for maximum average di/dt depends on the fault neutralization period of the circuit breaker under consideration.

- The optimum making angle for maximum rate of rise of current (di/dt) is always located at $\frac{t_{FN}}{2}$ earlier than the voltage peak (see the marked region in Figure 3-3).

- However, the optimum making angle for di/dt is not optimal for energy supply to the HVDC CB since the source voltage falls the moment energy absorption starts. i.e. at $\frac{t_{FN}}{2}$ after voltage peak.
- Thus, the making angle shall be optimized for both di/dt and the energy absorption of the breaker at the same time. This can be achieved by shifting the fault neutralization window (see Figure 3-3) to the left as shown in Figure 3-4. In other words, shift the making angle so that the peak voltage of the source appears during fault current suppression period (during energy absorption). At KEMA high power laboratory the making angle is precisely controlled through making switches which can ensure making at a resolution of 3º (electrical). Once the desired making angle is set, several test shots can be performed as needed to verify the correct prospective current.

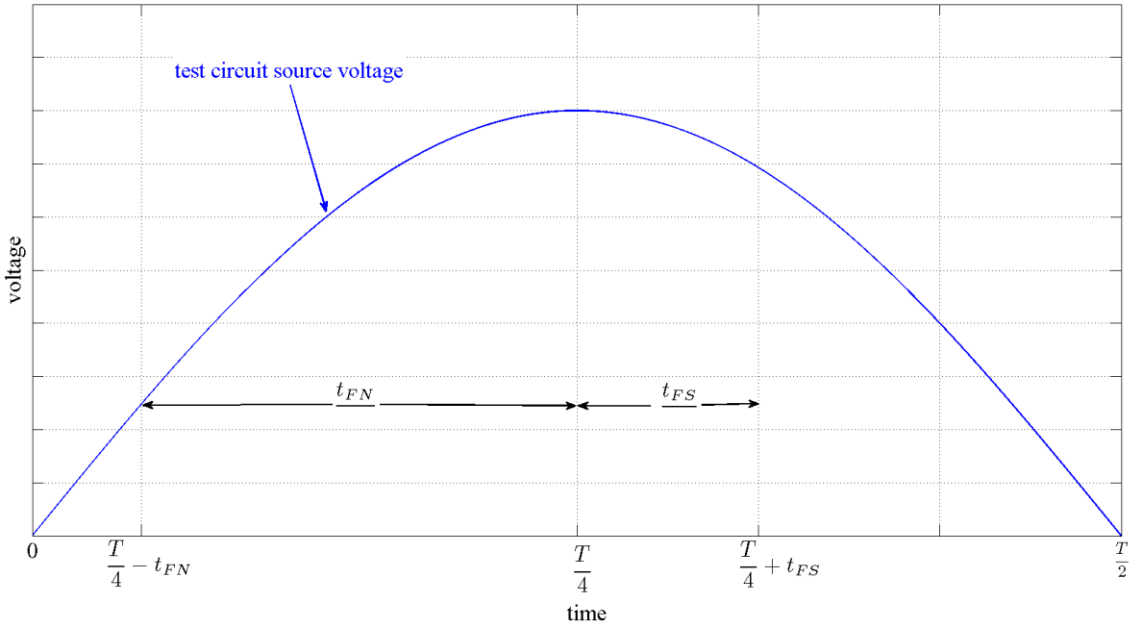

Figure 3-4: Relationship between making angle (θ), fault neutarlization time (t_{FN}) and fault suppression time (t_{FS})

To accommodate the two conditions described above, the generator frequency should be at least $\frac{1}{4f} > t_{FN}$. If the end of a fault neutralization period overlaps with the voltage peak (which is at $\frac{T}{4}$), as shown in Figure 3-4, the desired making angle is computed as,

$$\theta = \frac{\pi}{2} - \omega t_{FN} \tag{3}$$

In this case the expression for the average di/dt reduces to the following,

$$\left(\frac{di}{dt}\right)_{ave} = \frac{\hat{V}}{X_{\min}} \frac{\sin(\omega t_{FN})}{t_{FN}} \tag{4}$$

Under this condition, the energy absorbed by the circuit breaker is given by,

$$E = \frac{1}{2} L i_P^2 + \int_{t_{FS}} \hat{V} \cdot \sin\left(\omega\left(t - t_{FN}\right) + \theta\right) \cdot i(t) dt \quad (5)$$

Where the first term ($\frac{1}{2} L I_P^2$) in Equation (5) represents the energy stored in the circuit inductance at the end of fault neutralization period. The second term represents the energy being injected from the generators during fault current suppression period. As can be seen from this equation, the energy being supplied during the fault current suppression is dependent on the instantaneous voltage of the generator. In case the total energy supplied by a test circuit exceeds the rated energy for which the test breaker is designed; it can be reduced by decreasing the source voltage magnitude and the circuit impdedance proportionally. The other test circuit parameters can be kept the same until the point beyond which adjusting the voltage magnitude and impedance is no longer possible. The test circuit design flow chart is shown in Figure 3-5.

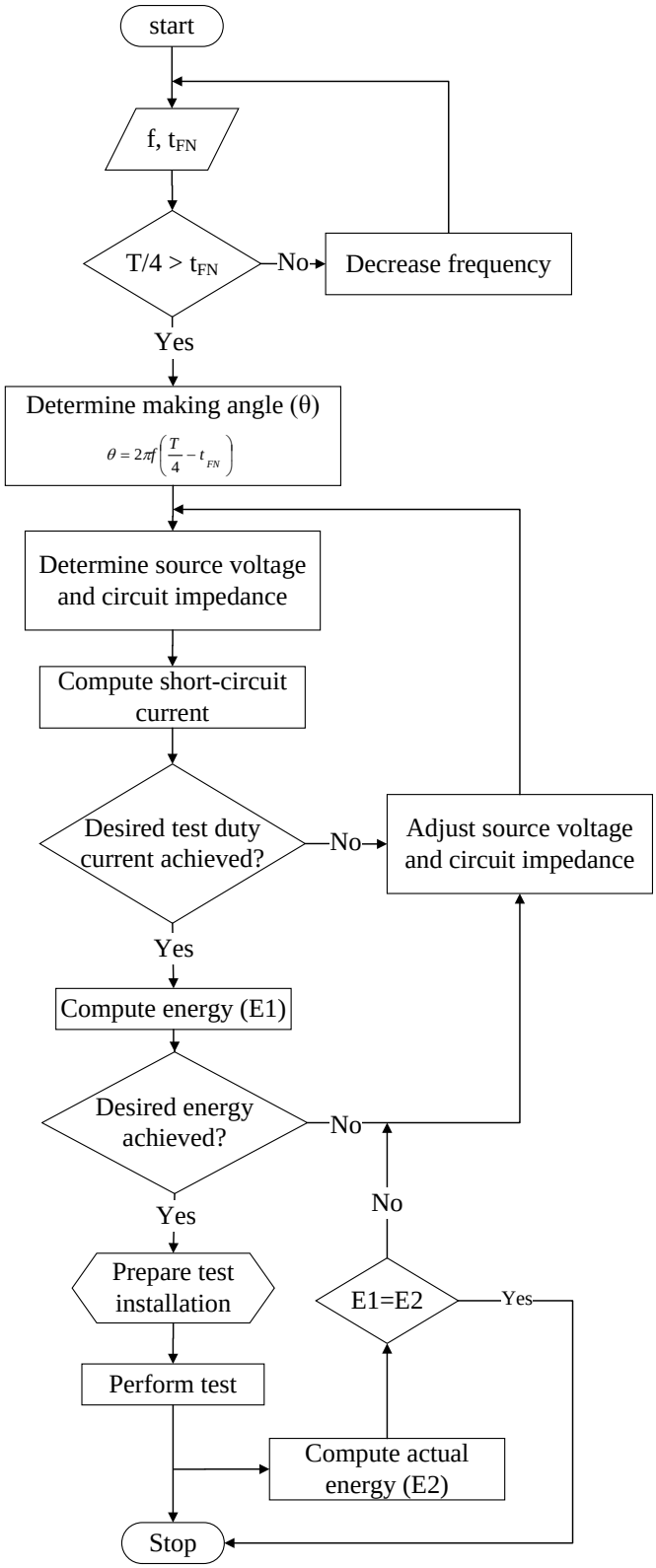

Figure 3-5: Flow chart for designing test circuit based on AC supply. f, frequncy, T, period, t_{FN} fault neutralization period.

4 REALISATION OF TEST CIRCUIT IN KEMA LABORATORIES

4.1 DESCRIPTION OF POWER LABS

In PROMOTiON project, full power tests of prototypes of three different technologies of HVDC circuit breakers are expected to be demonstrated at KEMA high power laboratory. A brief description of the basic equipment required to perform the tests of these breakers are provided in this chapter. Figure 4-1 shows aerial view of KEMA high-power laboratory, Arnhem, the Netherlands.

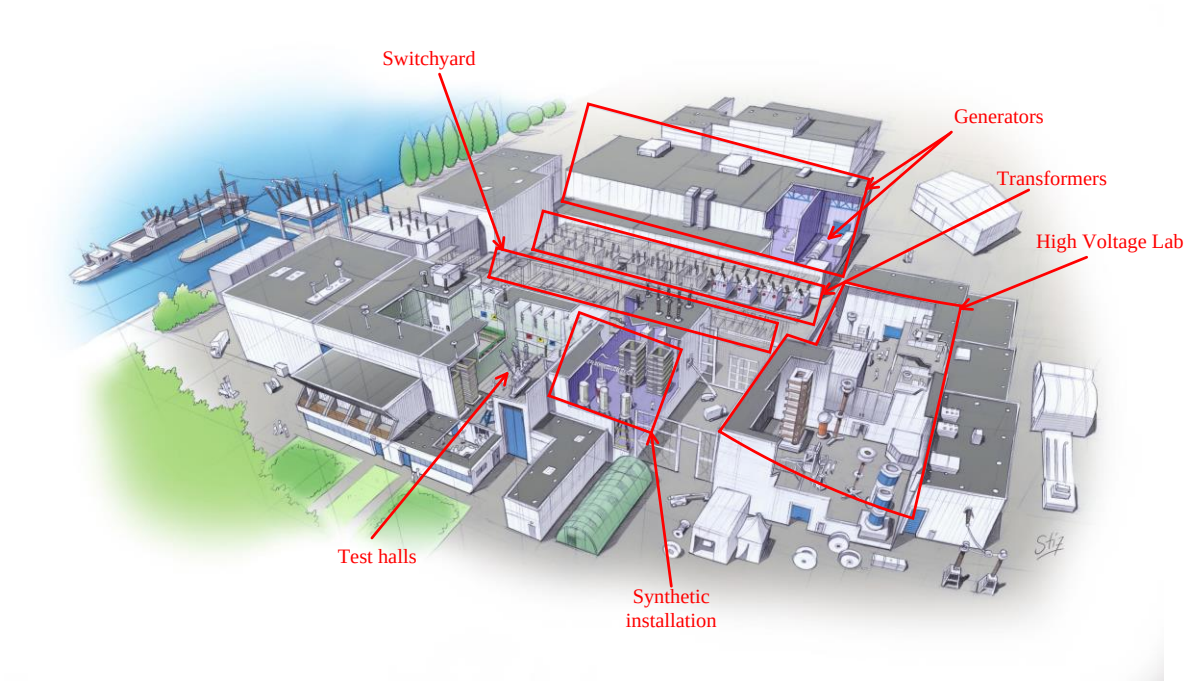

Figure 4-1 DNV GL's KEMA Laboratories

4.2 GENERATORS

At KEMA Laboratory a single short-circuit generator can be excited to generate voltage up to 15.4 kV at 50 Hz. At low frequency, the generator voltage reduces proportional to the frequency. Thus, at 16.67 Hz, a maximum voltage of 5.2 kV can be generated. Each generator can produce short circuit current up to a 100 kA (r.m.s.) at 50 Hz, however, for practical reasons a maximum is limited to 86 kA. There are six such generators available for short-circuit tests at KEMA laboratories. A photo of one of the short-circuit generators is shown in Figure 4-2. The generators can be synchronized and connected in parallel, and are combined with step-up transformers to produce desired current and voltage.

Each phase of the short-circuit generator is equipped with a master breaker that can interrupt AC current as high as 86 kA (r.m.s). In series with each master breaker there is a making switch which provides precise closing at a desired making angle.

Figure 4-2: Short circuit generator at KEMA laboratory (six such generators are available)

In Section 3.2 it was mentioned that when running short circuit generators at low power frequencies, the generator voltage and hence, the short-circuit power, reduces proportional to the frequency. In order to compensate for the reduced power due to low power frequency, several generators are connected in parallel. To compensate for the reduced voltage, several step-up transformers are used as shown in Figure 4-3.

During test, the HVDC circuit breaker is connected between two phases which ultimately reduce to single phase, see Figure 4-3. One of the two phases is grounded to provide reference as shown in Figure 4-3.

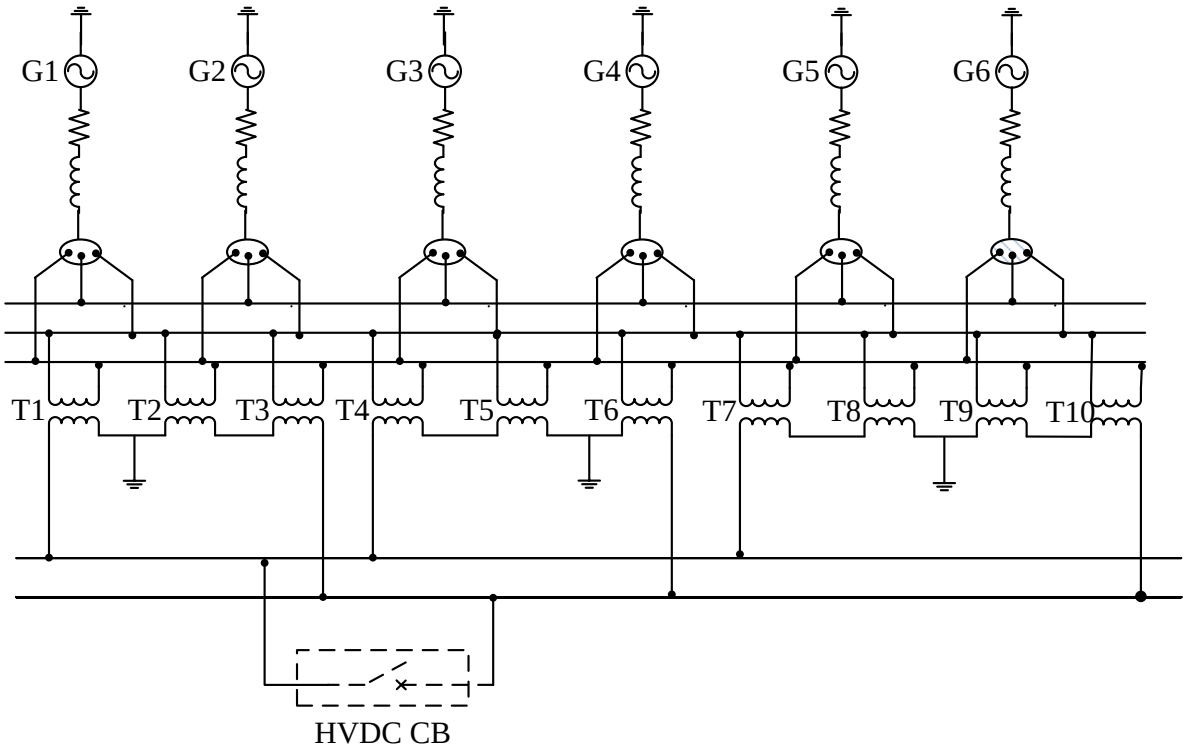

Figure 4-3: Possible test set-up of KEMA high power laboratory

In order to adjust the necessary currents, adjustable reactors for limiting short-circuit currents are added in each phase of the generators. A photo of one of these reactors is shown in Figure 4-4. These reactors have more than 35 tappings to provide different impedances as desired.

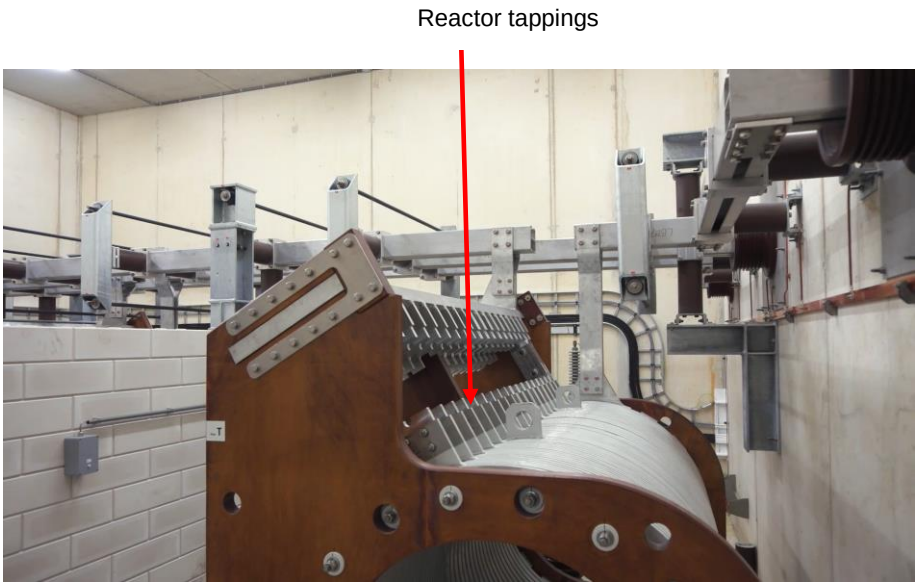

Figure 4-4: Adjustable current limiting reactor

4.3 SWITCHYARD & TRANSFORMERS

The transformers at KEMA laboratories are specially designed to handle short-circuit currents repeatedly. 10 such transformers are available for testing, see a photo in Figure 4-5. Each of these transformers have two windings on the primary side and two windings on the secondary side. The windings on each side can be connected either in series or in parallel independent of one another as shown in Figure 4-6.

Figure 4-5: Short circuit transformers and switchyard at KEMA laboratory

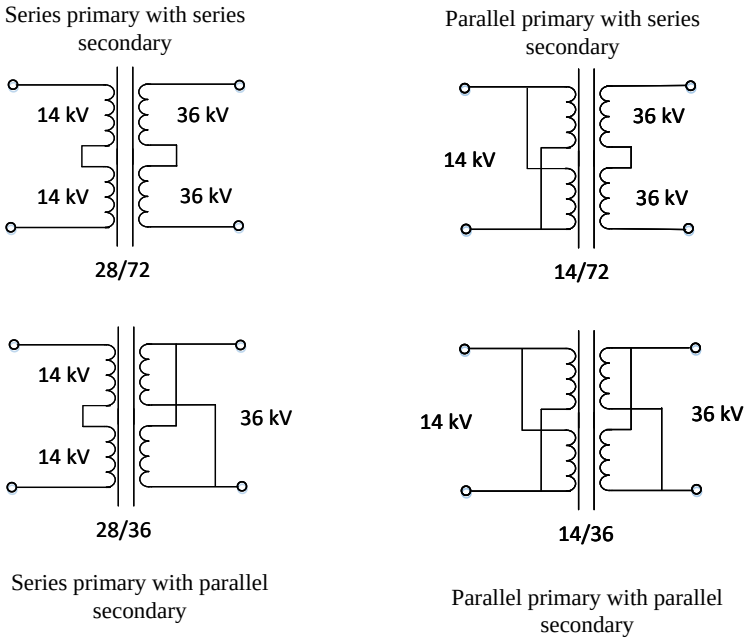

Figure 4-6: possible arrangements of short-circuit transformer windings at KEMA laboratories

4.4 SYNTHETIC INSTALLATION

The use of AC short circuit generators for testing HVDC circuit breakers does not supply DC dielectric stress after current suppression time. Thus, DC dielectric stress is supplied from charged capacitor banks. These capacitor banks should be charged to the maximum operating voltage of the system for which the test breaker is intended. In case dielectric breakdown occurs after current interruption, current is limited by reactors put in series with the charged capacitor banks. The photo in Figure 4-7 shows synthetic installation at KEMA high power laboratory consisting of capacitor banks, DC sources and reactors.

Figure 4-7: Synthetic installation consisting of capacitor banks, charging sources, reactors, resistors. Three synthetic capacitor banks can be charged up to 700 kV each.

4.5 INSTRUMENTATION & CONTROL

Reliable measurement is another crucial part of testing. When testing measurements of current, voltage and rate of rise (di/dt) are measured. Several devices might be needed to measure the same parameter depending on the range and frequency of the parameter to be measured.

4.5.1 HIGH VOLTAGE MEASURMENT

Voltage dividers are used for high voltage measurements. Depending on the magnitude of voltage to be measured, capacitive voltage dividers, resistive voltage dividers and combination of resistive and capacitive divider are used. The resistive voltage dividers are good for voltages up to 100 kV where as capacitive voltage

dividers are used for voltage measurements higher than 100 kV. The photo in Figure 4-8 shows a combined capacitive and resistive voltage divider.

Figure 4-8: Voltage divider (high voltage measurement)

4.5.2 CURRENT MEASUREMENT

Different current measurements are used depending on the range and frequency of current to be measured. Figure 4-9a-d shows various types of current measurement divices.

a) Current transformer: for measurent of high frequency current such as current injection circuit of HVDC circuit breaker
b) Standing shunt: for large current (up to 100 kA) measurent at power frequency
c) Coaxial shunt: for measurent of power frequency short circuit currents up to 100s of kAs
d) Rogowski coil: this measures rate of change of current. This is especially suited for current zero measurent.

a) Current transformer

b) Standing shunt

c) Coaxial shunt

d) Rogowski coil

Figure 4-9: Current measurement equipment

4.6 PROTECTION

Protection in the test environment is needed for the protection of a test object (test breaker), a test installation as well as safe operation in the test environment. A test installation (generators, transformers, switchyard, rails and lines) are protected with several layers of protection systems which automatically act if under any circumstances there occurs overvoltage and/or over current exceeding the rated values of the major

components. However, some components of the test installation (e.g. auxiliary AC circuit breakers) are used together with the test object (HVDC circuit breaker) whose operation is completely different than what the test installation components are designed for. Therefore, if no necessary measure is taken, there might be subsequent damage in the case unforeseen condition occur, for example failure to clear the short circui current. In order to avoid such a condition, overvoltage and overcurrent protection system is designed as part of the test circuit. For this purpose, a customized current level detector is developed to make sure a test object as well as auxiliary breaker used together with the test object are protected by bypassing the current to a different path the moment undesirebale current threshold is reached. For more detail, refer to Section 5.5.

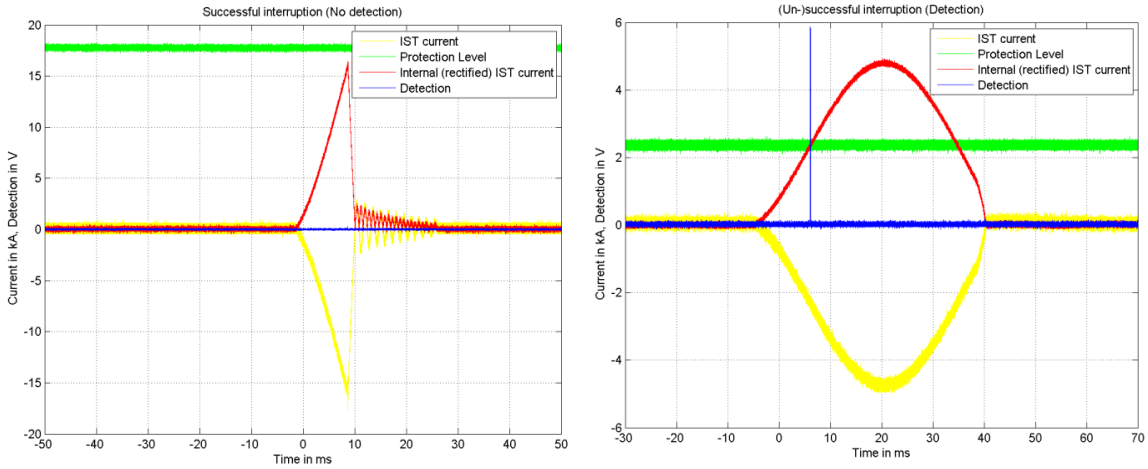

Figure 4-10: Overcurrent protection. a: Protection triggered by pass path and current commutation occurs b: the resulting current if over current protection is not used/failed

4.7 CAPABILITY & LIMITATIONS

What is the minimum impedance at a given voltage that results in safe current per generator? The safe current is a self-imposed limitation that is set to 50 kA (r.m.s) per generator for lower frequencies. Because the master breakers of short-circuit generators are designed for 50 and 60 Hz current interruption, it is decided that the safe current per generator is limited to 50 kA. Thus, with six short-circuit generators, each supplying 50 kA (r.m.s) current, the minimum impedance (inductance) in the circuit, as a function of secondary voltage (peak value) is computed considering the actual installation at KEMA laboratory. The result is depicted in Figure 4-11a at different frequencies.

Now, assuming $t_{FN} = 2\,ms + t_{BO}$, where t_{BO} is the breaker operation time, the maximum average rate of rise of current is computed as per Equation (4) of Section 3.2 considering optimization for energy absorption as well. It must be noted that if the average di/dt is greater than the desired value for a given test duty, additional reactors can be added to limit the rate of rise of current to within the rated breaking current of the breaker. Figure 4-11a and b show the maximum achievable rate of rise of current considering fault neutralization period of 4 ms and 10 ms, respectively.

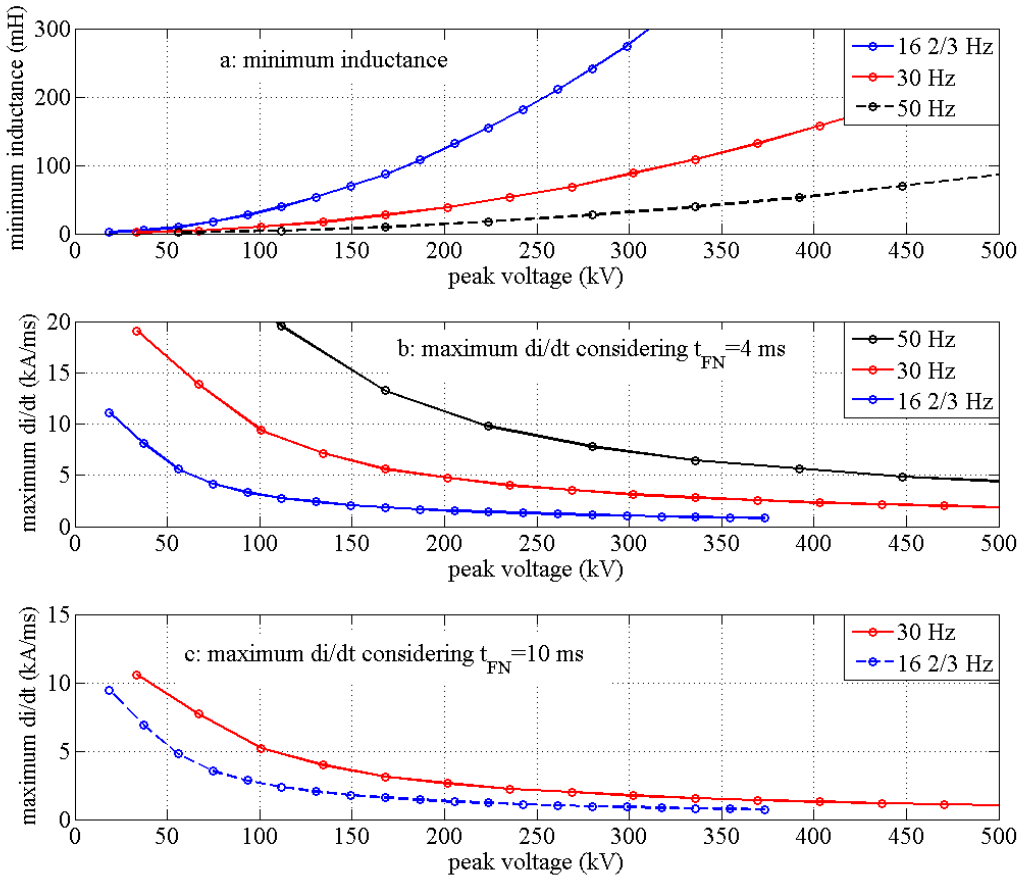

Figure 4-11: **Top graph**: minimum inductance as a function of (peak) voltage at different frequencies; **middle and bottom graphs**: the maximum average rate of rise of current (di/dt) as a function of voltage at different frequencies assuming fault neutralization period of 4 ms and and 10 ms, respectively. In all cases six generators used in the computation.

A few of the capabilities depicted in Figure 4-11 are demonstrated in KEMA highpower laboratory. The tests are performed by running six short-circuit generators with parameters described above and different number short-circuit transformers based on desired magnitude of source voltage. The resulting total inductance in the circuit at different source voltage are depicted in Figure 4-11a. If reduction of rate of rise of curren at a given voltage is intended, it can be done by inserting additional reactors in the circuit.

Figure 4-12 shows the test results where the rising short-circuit current and the source voltage causing this current. Four different points on graphs of Figure 4-11 are demonstrated considering different technologies of HVDC circuit breaker. Assuming fault neutralization time of 4 ms (Figure 4-11b), two tests at 30 Hz (Figure 4-12a) and b)) and one test at 16.67 HZ (Figure 4-12c)), are performed. Figure 4-12a) shows test result where source voltage is 200 kV. As predicted in Figure 4-11b) (see the trace for 30 Hz) current rising, on average within fault neutralization period, at a rate of 5 kA/ms is obtained. The making angle is in this case is 46.8º chosen based on approach described in Section 3.2. Similarly, a test is conducted with a source voltage of 100

kV at 30 Hz and the results are depicted in Figure 4-12b). In this case short-circuit current rising at a rate of 10 kA/ms is achieved. Figure 4-12d) displays test results of a test performed at 16.67 Hz considering fault neutralization of 10 ms. In this case source voltage of 155 kV is used and the average rate of rise of current is 1.8 kA/ms (this perfectly matches what is predicted in Figure 4-11c). In general, these are sufficient number of samples to demonstrate the maximum capability as in all the cases the graphs in Figure 4-12 are accurately predicted with calculation results in Figure 4-11.

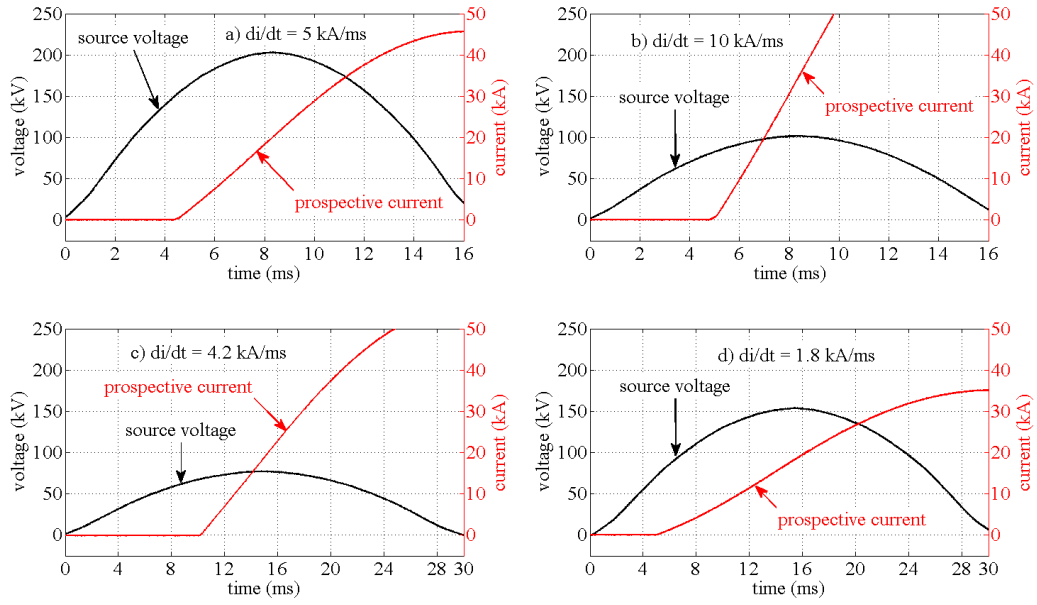

Figure 4-12: Experimental demonstration of prospective currents considering maximum capability at different source voltage and frequency

Current interruption of these fault currents by models of HVDC circuit breaker is performed via simulation. For example, Figure 4-13 shows test results considering active current injection HVDC circuit breaker with current interruption capability of 16 kA and assuming fault neutralization period of 10 ms. Simulation results are superimposed on the test results as shown in Figure 4-13. A model of active current injection HVDC circuit breaker rated for 160 kV is used in the simulation. Figure 4-14 depicts the energy absorbed by the breaker when interrupting the fault current of 16 kA with other parameters just described. The energy absorbed in this case is 20 MJ.

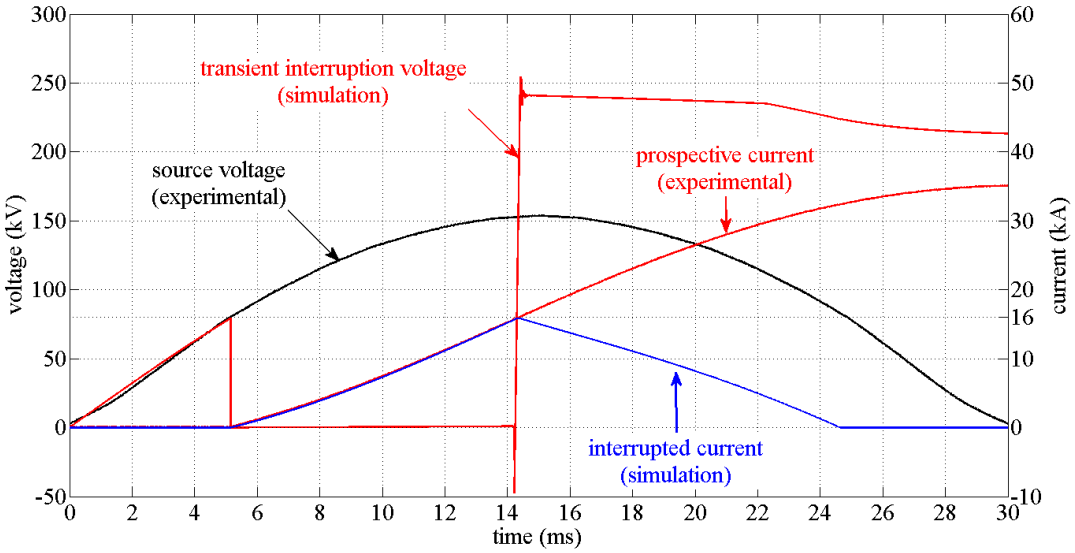

Figure 4-13: Current interruption assuming two active injection HVDC CB units (rated for 160 kV). The experimental results obtained by running six short circuit generators at 16.67 Hz

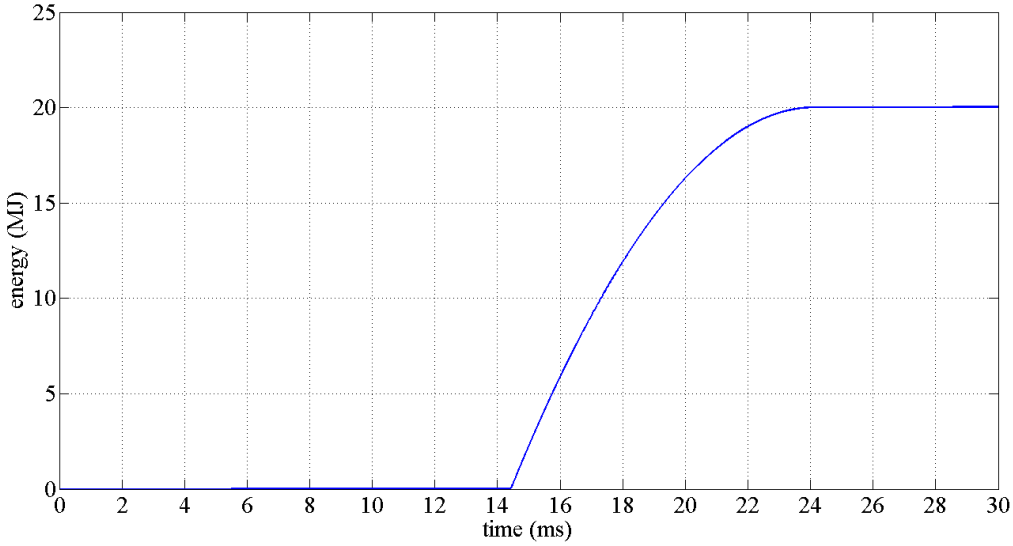

Figure 4-14: Energy absorption by active injection HVDC CB rated for 160 kV

5 TEST CIRCUIT VERIFICATION PLAN

5.1 INTRODUCTION

A complete test circuit designed based on AC generator supply is shown in Figure 5-1. The designed test circuit consists of four different parts serving different purpose as described below,

1. Power source

This is a part providing necessary the current, voltage and energy during current interruption test of HVDC circuit breaker. It consists of short-circuit generators and transformers. Each of the generators has a master breaker (MB) and a making switch in each phase. In addition, there is adjustable reactor to limit the short-circuit current from the generator in each phase. Power transformers are needed to step-up test voltage to a desired level. Each of the short-circuit transformers has two primary windings and two secondary windings where each side can be put in series or parallel independently. Besides, individual transformers can be put in series or parallel to adjust overall transformer impedance.

2. Protection

This is a part added to the test circuit for protecting a test breaker as well as a test installation in the case undesirable conditions occur during testing. It consists of triggered spark gap (TSG1) and auxiliary breaker (AB1). The function of this part is discussed in detail in Section 5.5.

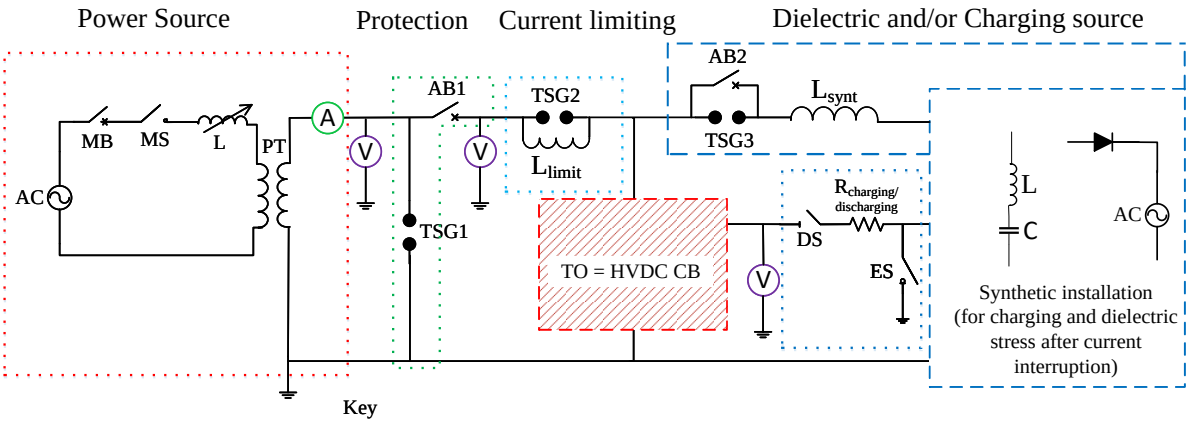

Figure 5-1: Test circuit set-up for HVDC CB

3. Current limiting

This part consists of triggered spark gap TSG2 and the initial current limiting reactor L_{limit}. This part is used only when testing hybrid HVDC circuit breakers and its purpose is described in Section 5.4.1.

4. Dielectric and/or charging circuit

This part provides charging of the test breaker's capacitor in case it is needed. This is also the part that supplies DC dielectric stress right after current interruption. It consists of capacitor banks and charging circuits, reactors (L_{synt}), triggered spark gap TSG3, auxiliary breaker AB2. In the case charging of the test breaker capacitor is needed, this part also includes charging and discharging resistance, earthing switches for safety, etc.

5.2 VERIFICATION PLAN

After a test circuit is designed as shown Figure 5-1, validation of its performance consisting of four different demonstration is planned. These demonstrations focus only on one of the parts described above at a time and combination of these parts in some cases. The demonstration plans are,

1. **Demonstration of prospective current test** – this is conducted in the absence of any HVDC circuit breaker in a test circuit. The objective is to check whether the desired current with desired rate of rise can be supplied using AC short circuit generators. Tests have been conducted considering different technologies of HVDC circuit breakers having breaker operation time in the range of 2-10 ms. Simultaneously, the capability to supply sufficient source voltage, which is required to control the energy stress, is verified. Simulation results of different HVDC CB technologies are superimposed on the experimental results to illustrate the resulting behavior during test.
2. **Demonstration of over current and overvoltage protection** – the main purpose in this case is on how to prevent possible damages to a test breaker as well as to a test installation when a test breaker fails to clear. Additional features and/or components are included to prevent overcurrent and/or over voltages during the actual test. Similarly, additional features which are required to safely test hybrid HVDC CBs are demonstrated. These breakers, due the presence of semi-conductors have a thermal limit on magnitude and duration of through-current.
3. **Demonstration of current interruption with HVDC circuit breaker**[1] – in this case a test circuit is designed to supply currents for different test duties. For convenience, four test duties, having similar nomenclature as AC circuit breaker test duties (T10, T30, T60 and T100), have been defined. The main objective in this case is to ensure whether adequate energy stress can be supplied in addition to the desired test current. A Mitsubishi Electric Mechanical HVDC CB with active current injection will be used in WP10 as test object for the purpose of demonstrating the test circuit's performance. Energy

[1]It must be noted that the main purpose of tests in WP5 is not the test of HVDC circuit breaker but demonstration of the test circuit. However, the HVDC circuit breaker is inevitably tested although it is not intended to verify the maximum capability of the breaker. In WP10, which is a continuation of WP5, the purpose is to verify the rated capabilities of circuit-breakers in terms of maximum current interruption, minimum breaker operation time, maximum energy absorption, etc.

supply in the range of **1.0-3.6 MJ** will be demonstrated. In addition to demonstration of the necessary stresses during test, the impact of the stresses imposed by the test breaker on the test circuit components as well as its interaction with the test installation is investigated.

4. **Demonstration of application of dielectric stress** – Two methods to supply a dielectric stress shortly after current is interrupted by a test breaker are investigated in this demonstration. One method, charge trapping, will be suitable for mechanical HVDC circuit breaker which use injection capacitors that remain charged after current suppression. The other method, suitable for hybrid breakers, relies on the injection of DC voltage stress by an external charged capacitor.

   Note that: the demonstration of charge trapping in mechanical HVDC circuit breakers is a provisionary solution since it implies testing using part of the test object itself. However, the impact of the trapped charge and its interaction with external dielectric source is investigated.

5.3 TEST PROCEDURE

During preparation for testing of HVDC circuit breaker, two check procedures are performed before conducting the actual current interruption test. The first part is pre-test check of a test breaker. This is intended to make sure whether the test breaker is properly installed and its controls can be operated as desired. In addition, if the test breaker requires the charging of its internal capacitor, as is the case for mechanical HVDC circuit breaker, this is performed as part of a test breaker preparation. The second part is calibration of a test circuit i.e. to check and verify proper settings of test parameters and make necessary adjustments in case there are deviations from required test parameters. Test circuit preparation procedures are described briefly below.

5.3.1 TEST CIRCUIT PREPARATION PROCEDURE

After the test breaker (test object, TO) is checked for its readiness, the test circuit components are adjusted and test parameters are calibrated. First the desired test circuit parameters are calculated via simulation and/or analytical calculation as described in Section 3.2. For example, the test circuit parameters for different test duties of active current injection HVDC circuit breaker is shown Table 1. Circuit elements corresponding to the calculated parameters are set-up. Note that: the resistances shown Table 1 are not lumped elements, rather parasitic resistances in the circuit. Also, the test circuit is designed with the maximum energy at T100 of 1.5 MJ.

Table 1: Test circuit components and corresponding parameter values

Test duty	Circuit parameters		Test parameters		Transformation ratio	Voltage at TO **(rms, kV)**	Symmetric current **(rms, kA)**
	Inductance **(mH)**	Resistance **(ohm)**	Current **(kA)**	Energy **(MJ)**			
T100	10.41	0.055	16	1.5	3.86	13.44	12.31
T60	16.67	0.0875	10	0.98	3.86	13.44	7.687
T30	33.36	0.1749	5	0.5	3.86	13.44	3.84
T10	167.23	0.8769	2	0.5	7.71	26.87	1.53

Once the test circuit is prepared, calibration procedure begins as, for instance, is described below for parameters of T60 stated in Table 1.

Step 1. Frequency calibration

Adjust the rotational speed of the generators as per the desired frequency. The desired frequency in this case 16.7 Hz. (See Figure 5-2).

Step 2. Voltage calibration

Given that test circuit components are arranged as specified in Table 1, set the excitation voltage of the generator(s), in this case to 3.48 kV. This results in 13.44 kV-rms (19 kV peak) open circuit voltage at the test object (TO, see Figure 5-2).

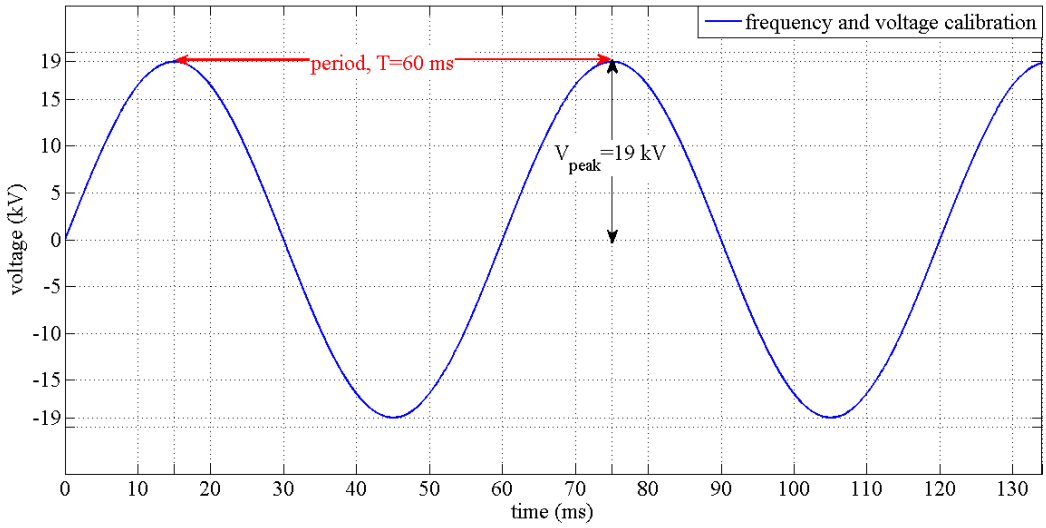

Figure 5-2: Illustration of frequency and voltage calibration for T60

Step 3. Current calibration

After proper settings for frequency and voltage are obtained, the next step is to calibrate the test current as per the desired duty. Unless otherwise it is desired to increase energy stress (where significant changes to impedance and transformation ratio is needed), test circuits are designed in such a way that the parameters which should be changed from one test duty to another are minimized. For example, by keeping voltage and frequency, the desired currents at different duties are varied by changing the circuit impedance. Only if sufficient circuit impedance cannot be obtained transformation ratio as well as circuit impedance are varied. In Table 1 the source voltage for T10 is changed from 13.44 kV to 26.87 kV (r.m.s) since the required impedance for producing T10 duty current cannot be achieved with the former circuit.

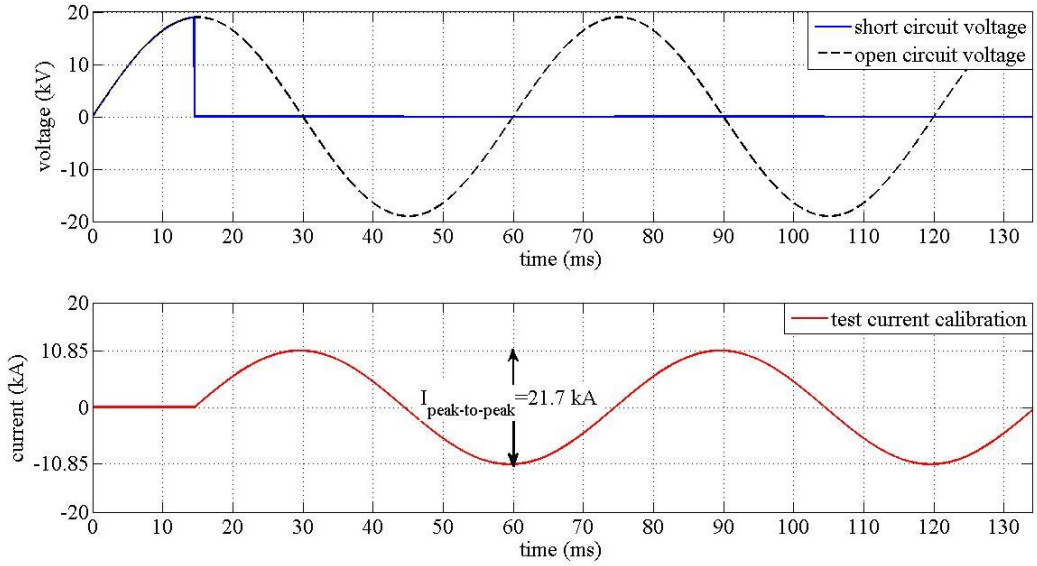

Figure 5-3: Test current calibration step

Step 4. Making angle calibration

The making angle is dependent on the fault current neutralization period (see Section 3.2). The making angle in Table 1 (39^0 (electrical)) is determined assuming fault neutralization time of 10 ms. That is at 39^0 from voltage zero which corresponds to t_1=6.5 ms, see Figure 5-4. For T60, this results in the duty current of 10 kA at 10 ms from the moment of short-circuit making. Thus, T=t_1+10 ms is the moment at which the test breaker is expected to generate the counter voltage so that the current starts to decrease. In other words, if the breaker operates to interrupt the current, the peak of the interrupted current appears at time T. Since during the actual test there are deviations from the desired parameters including the making angle and frequency, it is agreed that ±0.5 ms deviation is acceptable. That is the desired test duty current should be achieved within 10±0.5 ms from the moment of short circuit making. Thus, T=t_1+10±0.5 ms as shown in Figure 5-4. Therefore, as part of calibration process, the time T at which the test duty current is reached (10 kA for T60) is to be noted from prospective current during test.

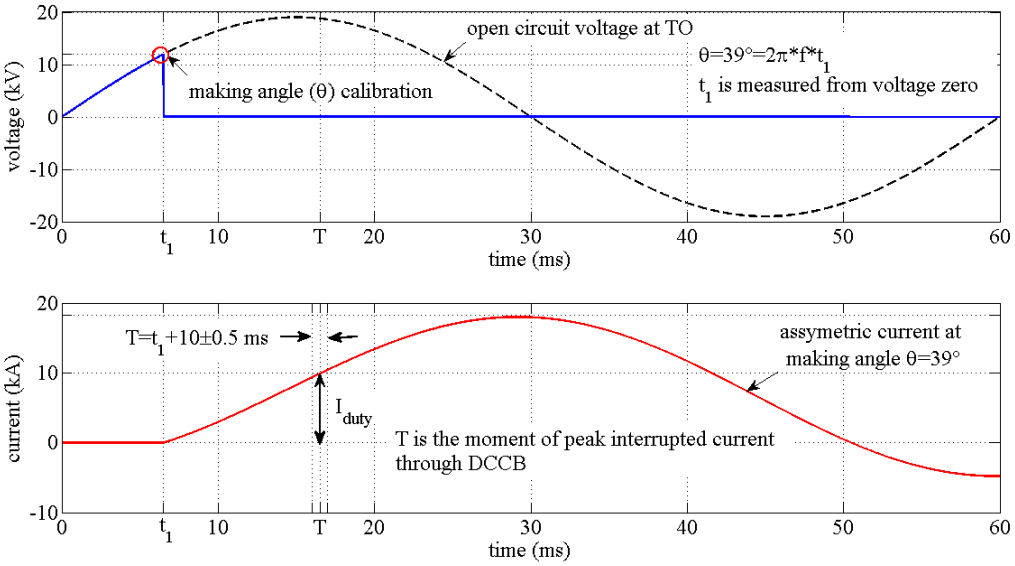

Figure 5-4: Making angle calibration

Step 5. Set the trip signal timer

After noting the time (T) at which the desired duty current is achieved, the time at which trip signal must be sent to the test breaker is determined. This time is dependent on the breaker operation time ($t_{breaker\ operation}$) of the test breaker. The breaker operation time is provided by the manufacturer of the test breaker. The trip order timer is set at $T\text{-}t_{breaker\ operation}$ as shown in Figure 5-5.

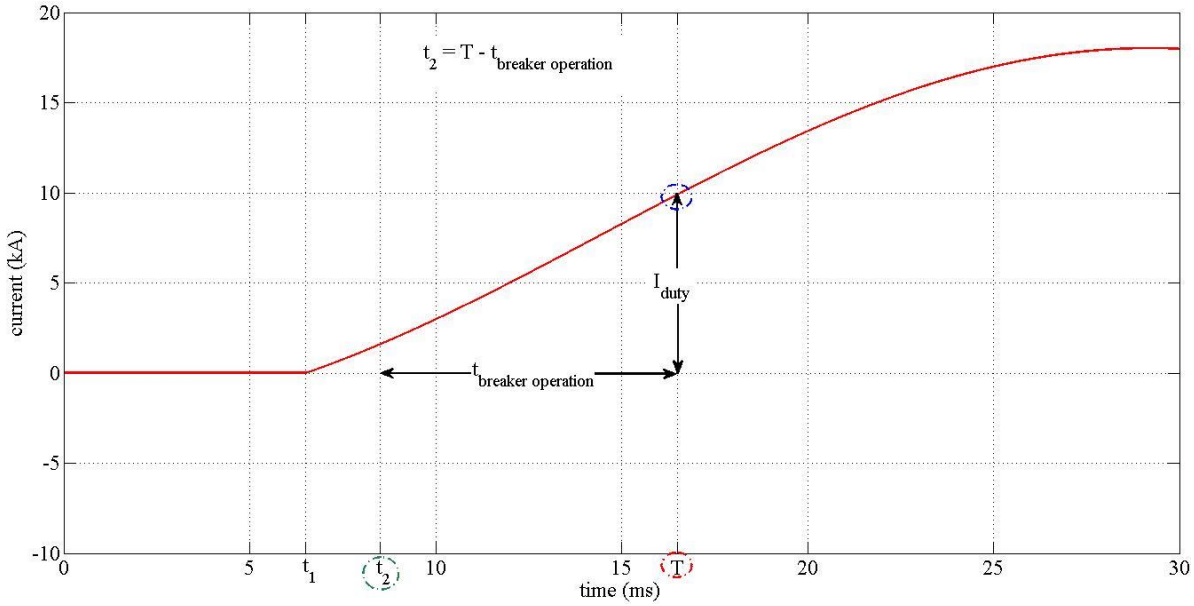

Figure 5-5: Setting trip signal timer

5.3.2 TESTING

For convenience, four test duties, having similar nomenclature as AC circuit breaker test duties (T10, T30, T60 and T100), having the following values have been defined for testing the performances of HVDC circuit breakers. For a HVDC circuit breaker with a fault current interruption rating of 16 kA, the following values result:

1. T100 – 16 kA interruption current
2. T60 – 10 kA interruption current
3. T30 – 5 kA Interruption current
4. T10 – 2 kA interruption current

The breaker operation time of the test breaker is independent of the test current and always remains the same.

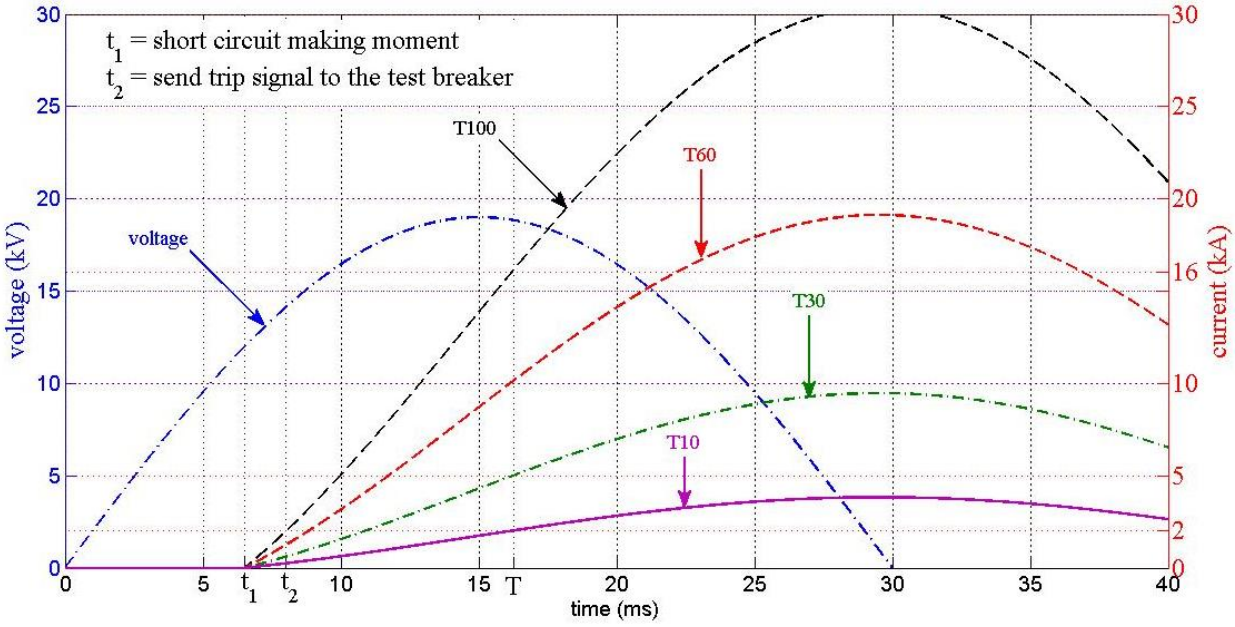

Figure 5-6: Prospective currents of the four test duties considering active current injection HVDC CB

5.4 DEMONSTRATION OF PROSPECTIVE CURRENT TEST

This is conducted in the absence of any HVDC circuit breaker in the test circuit. The objective is to check whether the desired current with desired rate of rise can be supplied using AC short circuit generators. This has been conducted considering different technologies of HVDC breakers with breaker operation times in the range of 2-10 ms.

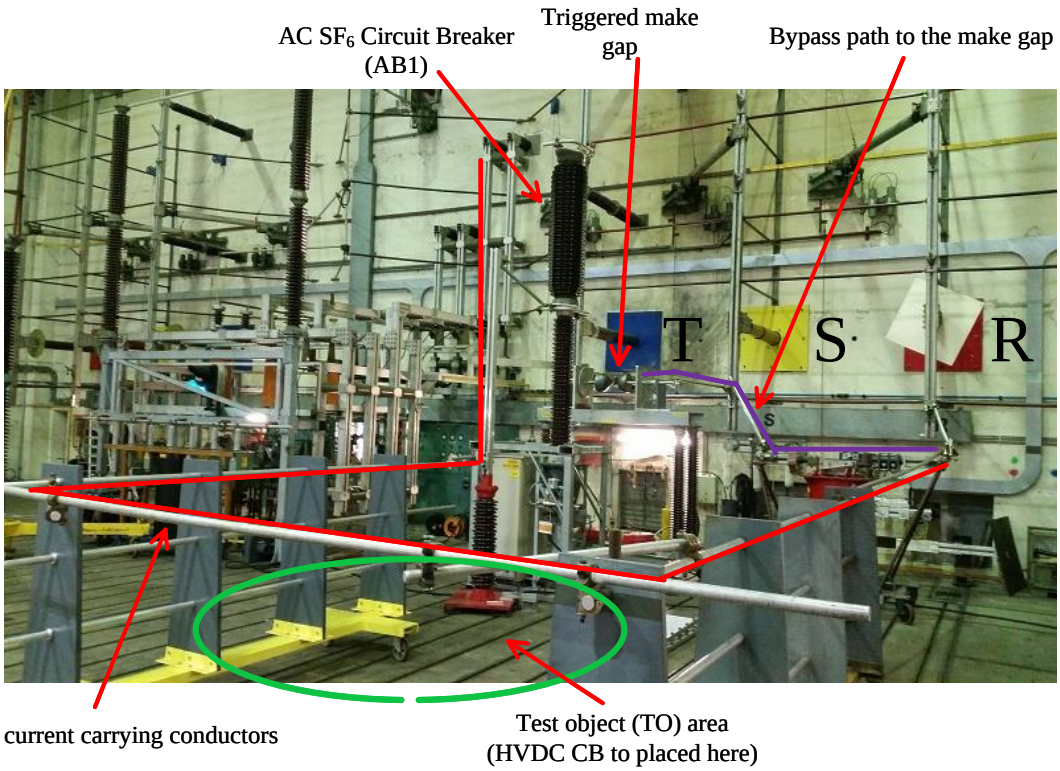

Figure 5-7: Actual HVDC CB test set-up in the high-power laboratory (Generators and transformers behind the wall). A test object to be connected between two phases, R and T.

A preparation test in the absence of an HVDC CB (when HVDC circuit breaker is not operating) has been conducted to verify if current with sufficient di/dt can be achieved. A test circuit has been set up as shown in Figure 5-7. Several tests have been conducted considering HVDC CBs with different breaker operation times as well as considering different test duties.

5.4.1 PROSPECTIVE CURRENT FOR HYBRID HVDC CIRCUIT BREAKER

Prospective tests have been conducted considering hybrid HVDC circuit breakers with a breaker operation time of 2 ms. The graph in Figure 5-8a shows a typical prospective current from the actual test result (see the red trace) performed considering hybrid HVDC circuit breaker. In case the HVDC circuit breaker does not suppress the current, the prospective current increases to a peak value of 39.5 kA which is much higher than the fault current interruption rating of the HVDC CB. The voltage measurements are shown in Figure 5-8b. The prospective voltage at the terminals of the hypothetical HVDC CB has a peak value of 80.5 kV. The experimental results are obtained by running four short-circuit generators in combination with six transformers at a power frequency of 18 Hz.

To get an insight in the phenomena occurring during test, current interruption by a (simulation) model of hybrid HVDC CB in a test circuit with parameters as the actual installation at the test facility is simulated and plotted

(blue and black curves) on top of the experimental results (red curves) in Figure 5-8. A breaker operation time of 2 ms for hybrid breaker is assumed in the simulation.

First the prospective current is interrupted when the rising current reaches 10 kA (see solid blue trace in Figure 5-8a). In this case the breaker receives a trip signal when current reaches 4 kA. Thus, the load commutation switch (power electronic components in normal current path) of the hybrid breaker commutates 4 kA to the main breaker. 2 ms second later the main breaker interrupts 10 kA and current commutates to the energy absorption branch. In this case about 4 MJ energy is absorbed by the HVDC circuit breaker.

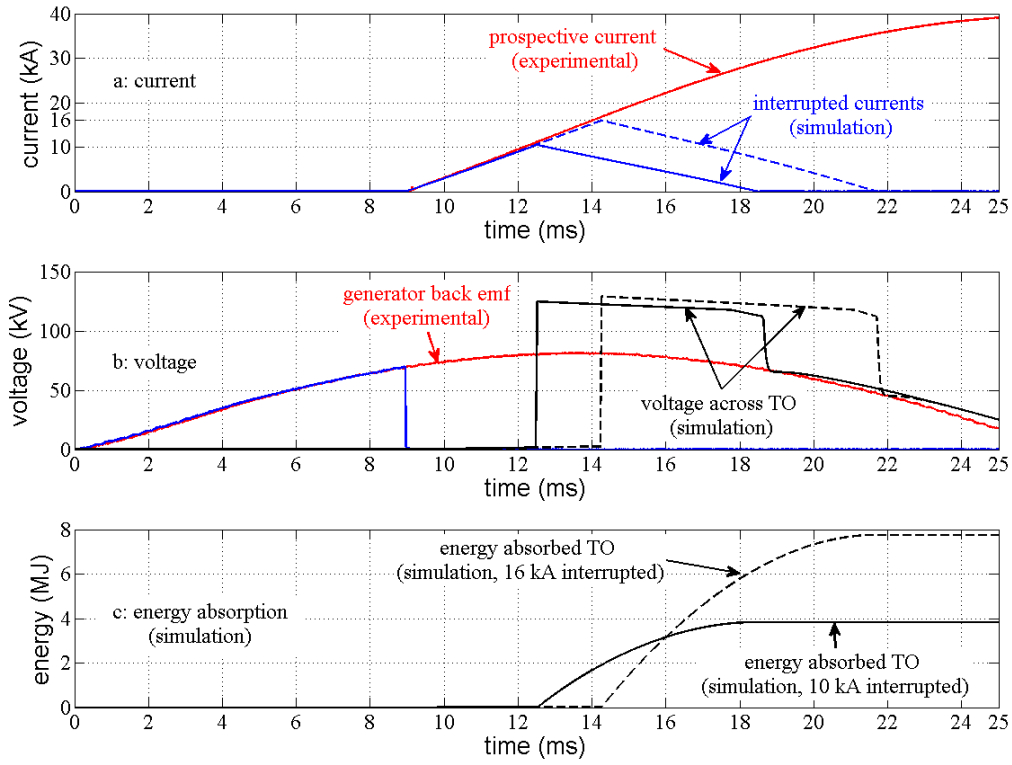

Figure 5-8: a: Demonstration of prospective current for hybrid HVDC circuit breaker (red trace). Simulation results of current interrupted by a model of HVDC circuit breaker is superimposed (blue traces). b: source voltage (experimental result) and circuit breaker TIV (from simulation result). c: energy absorbed by simulation model of hybrid breaker.

In addition, Figure 5-8 shows the same prospective current but interrupted at 16 kA which is possible by increasing the fault current neutralization period while keeping the breaker operation time 2 ms. In such a case the power electronic components in the normal current path need to commutate approximately 10 kA into the main breaker path (refer to [3] for the terminologies). However, if the power electronic components in the normal current path cannot handle 10 kA, there is a need to increase the rate of rise of current.

Moreover, to isolate the source side from the test breaker, an auxiliary AC breaker (AB1 in Figure 5-1) is used. AB1 is a standard SF_6 AC circuit breaker rated for 245 kV, with a minimum rated arcing time in the range of 10-15 ms. However, the rapid current interruption by the test breaker may result in shorter arcing time of this device. It must be noted that this AC breaker does not actually interrupt current. Rather it will disconnect the source side from the dielectric supply side once current has been suppressed to zero (by the test breaker or otherwise) so that the test breaker is subject to only dielectric stress after current suppression. Thus, to increase the total arcing time for the auxiliary breaker whilst maintaining an electrical connection through an arc, the test current is initially limited by an additional large reactor and this reactor is bypassed by a triggered spark gap (TSG2 Figure 5-1) at a later making angle. Prior to the by-passing of the large reactor, the low rising current is sufficient to maintain the arc whilst the auxiliary breaker achieves its contact separation. The moment of by-passing is done according to the previous considerations to to create adequate di/dt for the test breaker. Figure 5-9 shows the concept just described.

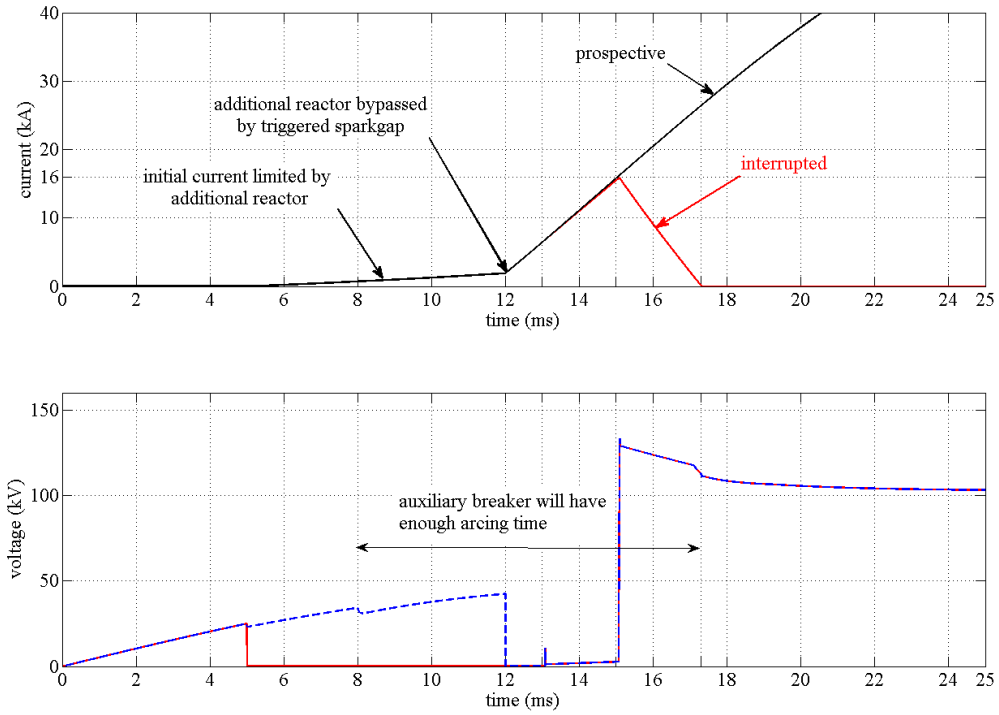

Figure 5-9: Current limitation by additional reactor and dielectric stress after current for hybrid HVDC circuit Breaker (simulation result)

5.4.2 PROSPECTIVE CURRENT FOR ACTIVE CURRENT INJECTION HVDC CIRCUIT BREAKER

Similarly, prospective current tests considering active current injection HVDC circuit breaker have been performed and results are depicted in Figure 5-10. As for hybrid HVDC circuit breakers, a simulation of the current interruption of an active current injection HVDC circuit breaker is used to get an insight in the phenomena during current interruption. It can be seen from Figure 5-10a that about 16 kA current is interrupted by the HVDC CB. Figure 5-10b depicts the expected TIV of the breaker. Superimposed on this graph is also

disconnection of the source side from the test breaker by the auxiliary breaker AB1 in Figure 5-1. Thus, the TIV of the breaker remain constant after current suppression as can be seen by blue trace in Figure 5-10b. This is described in further in Section 5.6.1. Figure 5-10c shows the energy that would be absorbed by the test breaker when interrupting the current at 16 kA. About 5 MJ of energy is absorbed by the breaker and this is related to the energy stored in circuit inductance (27.5 mH) as well as supplied by the generators during the fault suppression period. If increased energy stress is needed, the generator voltage can be increased. In order to keep the breaking current the same (16 kA), the circuit inductance must be proportionally increased. The dashed trace in Figure 5-10c shows the energy absorbed by the HVDC CB when the generator voltage is increased from 46.5 kV (peak) to 70 kV (peak). The same current is interrupted in both cases, however, about 9.2 MJ energy needs to be absorbed in the latter case.

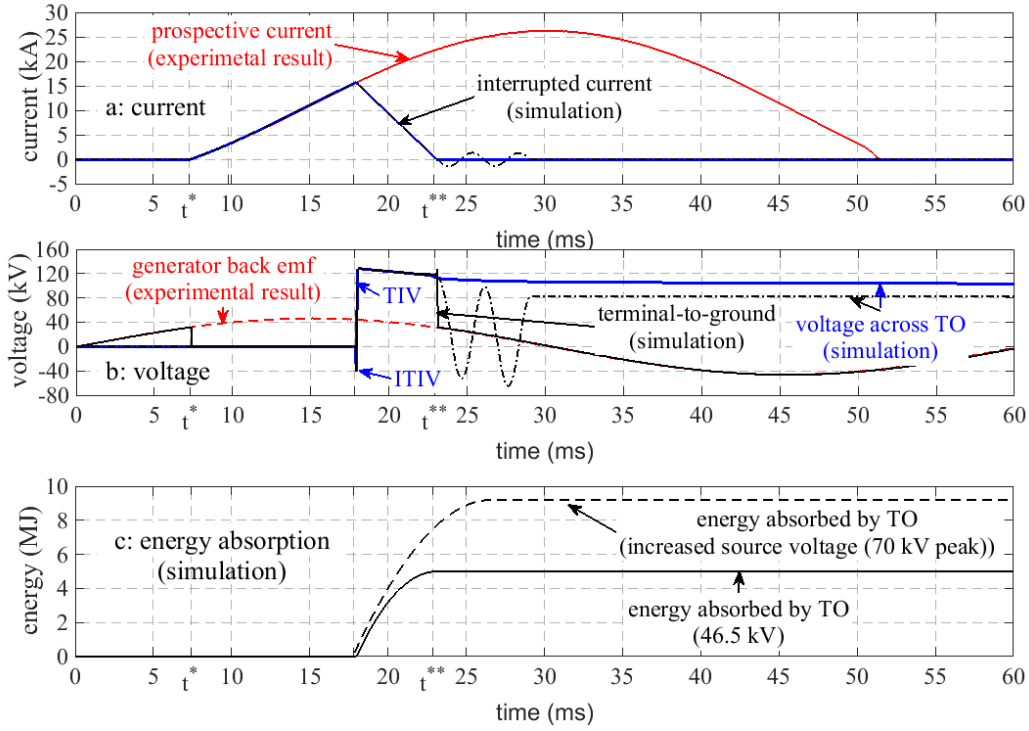

Figure 5-10: a: Experimental demonstration of prospective current for active current injection HVDC circuit breaker (red trace). Simulation results of current interruption by active current injection is superimposed (blue trace). b: source voltage (red trace), breaker TIV during current interruption (blue and black dash-dotted traces). c: energy absorbed by circuit breaker at different source voltage

5.5 DEMONSTRATION OF OVER-CURRENT AND OVER-VOLTAGE PROTECTION

The main purpose in this case is on how to prevent possible damage to the test breaker as well as to the test installation when the test breaker fails, for whatever reasons, to clear. Additional features and/or components (see Figure 5-1) are included to prevent overcurrent and/or over voltages during the actual test.

A major challenge of using AC short-circuit generators for testing HVDC CBs is the fact that a large current will flow in case the test breaker fails to clear. This will result in two undesirable conditions. First, the test breaker may not be able to withstand the large current and could subsequently be damaged if proper protection against such a situation is not prepared. Second, it may damage the AB1 especially because of the long arc duration due to the low frequency. The former issue becomes critical when HVDC CBs having power electronic components are tested. Such breakers have a short breaker operation time leading to a requirement of high di/dt to reach the maximum breaking current within the breaker operation time. If such a breaker fails to clear, much larger current flows than these components can handle. For example, the prospective current having di/dt of 3.5 kA/ms is demonstrated in Figure 5-9, [8]. It can be seen from the same figure that the peak prospective current of 39.5 kA results if the test breaker fails to clear.

Therefore, to avoid damage to both the test breaker and to the auxiliary breaker, a parallel path provided by a triggered make (spark) gap as shown in Figure 5-1 (see its implementation Figure 5-7, magenta path) is proposed. The make gap is triggered only if a predefined current threshold beyond which the test breaker cannot clear is reached. A triggered level detector has been developed especially for this purposes as described in section 3.6. The proposed technique is experimentally verified and the test result is shown in Figure 5-11 where 25 kA current commutates from the path of the test breaker (TO) into the triggered make gap bypass path. Sufficient voltage drop is needed in the test object loop for commutation to take place. This is sufficiently provided by the arcing voltage of the AC auxiliary breaker (AB1).

The impact of the gap length was also investigated. Increasing the gap length slightly increased the commutation time. Moreover, the use of triggered make gap can serve double purpose. The gap length can also be set for overvoltage protection to protect the test installation. During the actual test of the HVDC CB, the gap length must be set for an overvoltage sufficiently higher than the TIV of the test breaker with adequate margin so that it does not interfere during the normal interruption process. The gap length was set to 15 cm for the test shown in Figure 8 and this is sufficient to a withstand voltage up to 275 kV.

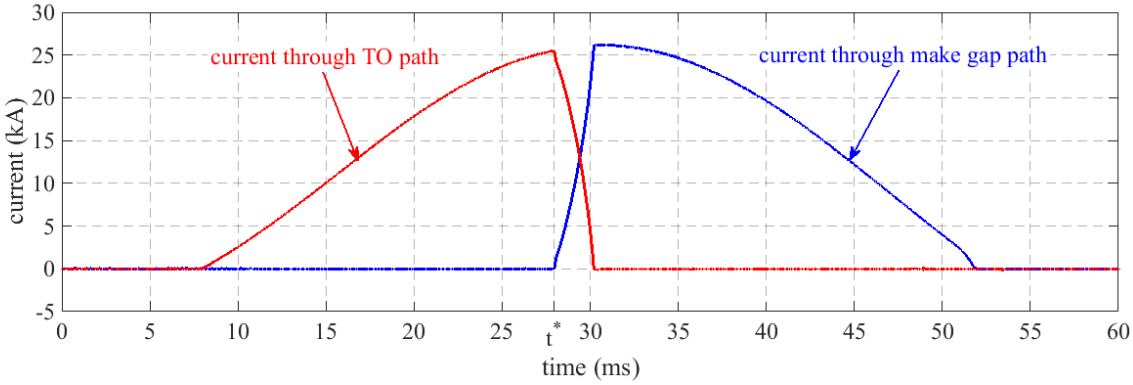

Figure 5-11: The test result showing current commutation from test object (TO) path to triggered make gap path

5.6 APPLICATION OF DIELECTRIC STRESS AFTER CURRENT INTERRUPTION

Since the source voltage is supplied by the AC generator, it cannot provide long duration DC dielectric stress after successful current interruption. However, some HVDC CBs, for example, the active current injection HVDC CB have capacitors as part of the CB which remain charged during the current interruption process. This capacitor remains charged during the entire energy absorption period to a value equal to the TIV of the breaker. This can be used to provide dielectric stress after interruption. The other solution is to apply dielectric stress after current interruption by a separate DC voltage source. However, practically this poses several challenges which must be carefully addressed. The two different approaches are discussed in the next subsections.

5.6.1 CHARGE TRAPPING METHOD

After current is suppressed to (nearly) zero by the test breaker, there is a damped oscillation between the charged capacitor of the active current injection circuit breaker and the circuit inductance (see). The magnitude of the oscillating current is determined by the difference between the voltage of the charged capacitor and the instantaneous voltage of the generator the moment current is suppressed to zero and the frequency is determined by the capacitance and the total inductance in the circuit including the inductance in the injection branch of the breaker. The frequency of oscillation being,

$$\boldsymbol{f = \frac{1}{2\pi\sqrt{LC_p}}} \tag{6}$$

Where $L = L_p + L_{circ}$, L_p is the inductance in the counter injection branch of the test breaker, L_{circ} is the inductance in the rest of the circuit, and C_p is the capacitor of the test breaker.

It must be noted that for each test duty the frequency of this oscillation changes as the circuit impedance changes at each duty. Since a source voltage with a peak value of 19 kV (which is very low compared to 120 kV TIV) is used, a significant current could still be flowing after current suppression period. Currents with a peak value up to 2.5 kA oscillating at frequency f (in Equation (6) is observed. The voltage across the breaker oscillates superimposed on the generator voltage (the axis of oscillation is the generator voltage).

Table 2: Oscillation frequency, peak-to-peak current and capacitor voltage after current interruption by active injection HVDC circuit breaker

Test duty	Oscillation frequency (Hz)	Peak-to-peak current (kA)	Peak-to-peak-voltage (kV)
T100	548.84	5.1	184.7
T60	434.3	4.1	185.5
T30	307.64	2.8	186.63
T10	137.56	1.1	162.65

Now, if the auxiliary AC breaker (AB1 in) interrupts to disconnect the source side from the test breaker the moment the short-circuit current is suppressed to zero, the remaining charge on the capacitor of the HVDC CB can be used to provide dielectric stress to its main interrupter. This can be seen by blue traces in a and b. The voltage across the capacitor is slightly decaying since it is discharging through the surge arrester. In order to interrupt current at the moment it reaches zero, the contacts of the AB1 must be separated and arcing at least the minimum arcing time before current is interrupted by the HVDC circuit breaker.

5.6.2 SYNTHETIC DC VOLTAGE INJECTION METHOD

This is achieved by connecting a separate DC source immediately after current suppression to supply dielectric stress. Therefore, before connecting a DC source for dielectric stress, current suppression by the test breaker must be detected. The duration of the fault current suppression period depends the amount of energy the breaker absorbs.

To demonstrate the concept, two capacitor banks (so-called synthetic installations) are used; one as dielectric source and the other as test object capacitor (in the absence of test breaker). The idea is, upon detection of current interruption by a test breaker, a triggered spark gap (TSG3 in Figure 5-1) is activated. The implementation of the test circuit is shown in Figure 5-12. It must be noted that just before triggering TSG3, the auxiliary breaker (AB1, in) should have isolated the source (generator) side from the test breaker.

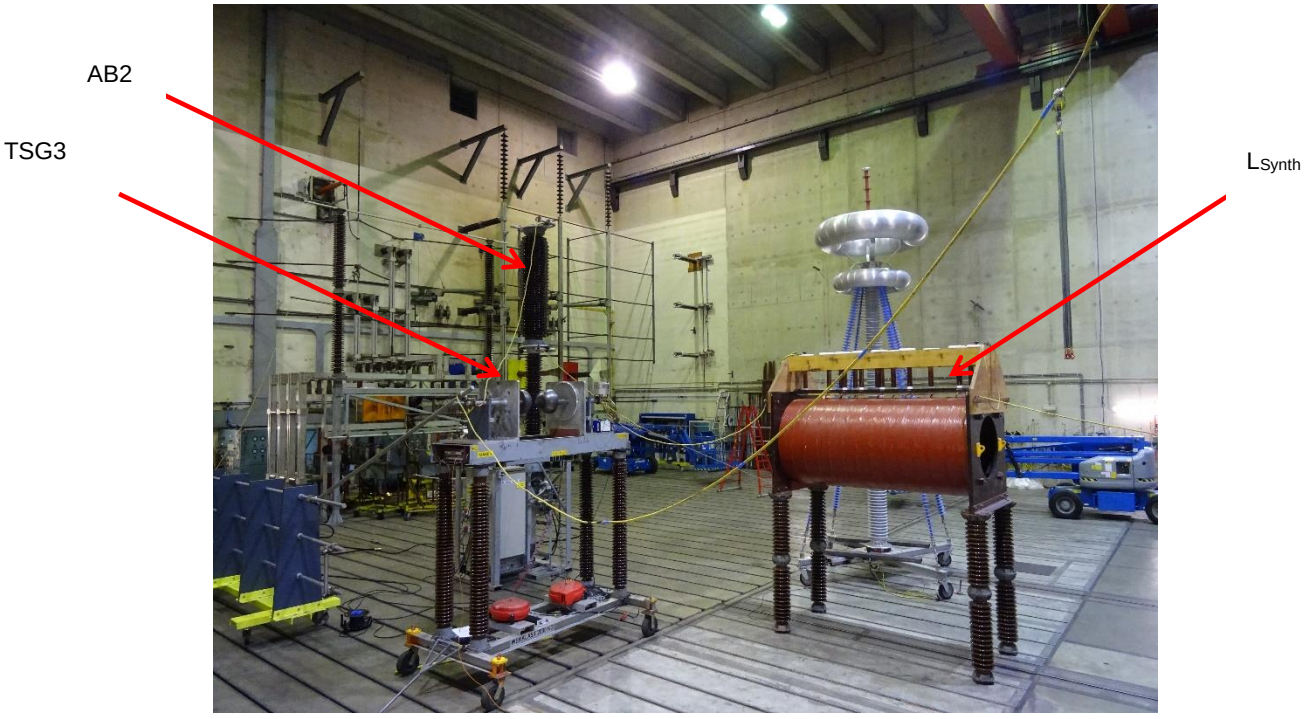

Figure 5-12: Actual circuit set-up for dielectric injection (reactor is used between dielectric source and ‘virtual’ test object)

By triggering TSG3, there will be interaction between the two charged capacitors since both are charged at different voltages. This is demonstrated in Figure 5-13 where one capacitor is charged to 80 kV whereas the other is charged to 96 kV. Because of parasitic resistive damping in the circuit, the oscillation (charge transfer) between the two capacitors stops after a while, see Figure 5-13. The capacitors' charges will balance out, thus stopping the conduction of the spark gap. When a triggered spark gap is no longer conducting, it cannot provide a galvanic connection. Thus, the dielectric stress cannot be applied to the test breaker under this condition. In order to ensure galvanic connection after the capacitors' charge balance is reached, an additional auxiliary breaker (AB2) in parallel with TSG3 is closed, (see Figure 5-1 and its implementation Figure 5-13). The requirement of the triggered spark gap TSG3 is to switch rapidly after a trigger is generated at the moment of suppression by a test breaker. This can be done with the developed level detector.

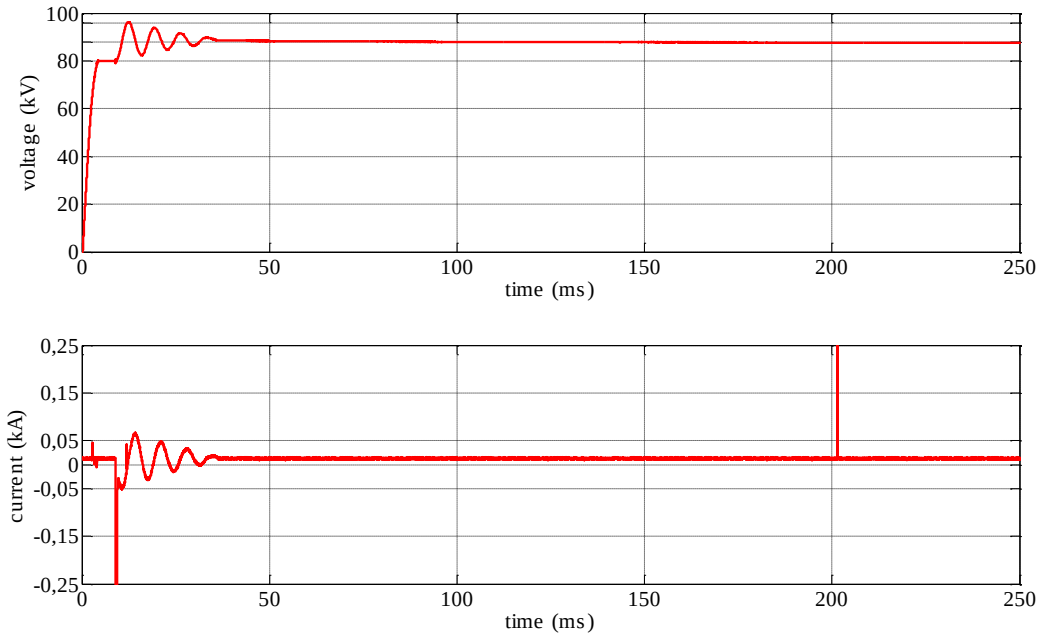

Figure 5-13: Voltage Injection initiated by triggered spark gap (note that galvanic connection is lost the moment current stops flowing through the spark gap) and the auxiliary breaker AB2 is closed by this time.

6 CONCLUSION

In this deliverable, the realisation of the reduced frequency AC short-circuit generators based test circuit at KEMA Laboratories is described. A method for tuning the test circuit's variables to achieve the required current and energy test stresses is presented. The implementation of overvoltage and overcurrent protection methods is explained, as well as methods to realize dielectric stress after current suppression. A test program aimed at validating the test circuit's ability to meet the requirements is provided. Test results of prospective current tests, over current and overvoltage protection tests, and of dielectric stress application tests are provided. Simulation results of HVDC circuit breaker models are superimposed onto the experimental results to illustrate the ability of the test circuit to synthesize realistic stresses. Finally, simulation of full power test results of DC fault current interruption tests on both a hybrid as well as a mechanical HVDC circuit breaker with active current injection are presented. The reduced frequency AC short-circuit generator based test circuit for HVDC circuit breakers has been successfully demonstrated.

7 BIBLIOGRAPHY

[1] PROMOTioN Deliverable 5.6, "Software and analysis report on candidate test-circuits and their effectiveness," PROMOTioN Project, 2017.

[2] CIGRÉ JWG A3/B4.34 TB 683, "Technical requirements and specification of the state-of-the-art HVDC switching equipment," CIGRÉ, 2017.

[3] PROMOTioN Deliverable 5.3, "Fault Stress Analysis of HVDC Circuit Breakers," 2016.

[4] J. Häfner and B. Jacobson, "Proactive Hybrid HVDC Breakers - A key innovation for reliable HVDC grids," in *CIGRÉ Symposium* , Bologna, Italy , Sep 2011.

[5] W. Zhou, X. Wei, S. Zhang, G. Tang, Z. He, J. Zheng, Y. Dan and C. Gao, "Development and test of a 200kV full-bridge based hybrid HVDC breaker," in *17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, Switzerland, 2015.

[6] K. Tahata, S. Ka, S. Tokoyoda, K. Kamei, K. Kikuchi, D. Yoshida, Y. Kono, R. Yamamoto and H. Ito, "HVDC circuit breakers for HVDC grid applications," in *CIGRÉ AORC Technical meeting*, Tokyo, Japan, 2014.

[7] W. Grieshaber, J.-P. Dupraz, D.-L. Penache and L. Violleau, "Development and test of a 120 kV direct current circuit breaker," in *CIGRÉ session 45*, Paris, 2014.

[8] N. A. Belda and R. P. P. Smeets, "Test Circuits for HVDC Circuit Breakers," *IEEE Transactions on Power Delivery,* vol. 32, no. 1, pp. 285-293, 2017.

[9] F. N. L. Name, Test Test Test, Berlin, 2016.

[10] M. K. Bucher, "Contribution of Fault Current Sources in Multiterminal HVDC Cable Networks," *IEEE Transactions on Power Delivery,* vol. 28, no. 3, pp. 1796-1803, July 2013.

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