PROJECT REPORT

PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

Task 6.1 Develop system level model for hybrid DC CB

PROMOTioN – Progress on Meshed HVDC Offshore Transmission Networks
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LIST OF CONTRIBUTORS

Work Package and deliverable involve a large number of partners and contributors. The names of the partners, who contributed to the present deliverable, are presented in the following table.

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Content

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EXECUTIVE SUMMARY

This report presents the results of task 6.1 of the work package WP6 “HVDC circuit breaker performance characterization”. The main objective of this task is developing system level models for selected hybrid DC CBs in PSCAD and EMTP. These models will be used in DC grid protection studies in WP4, WP5 and WP9 and also in wider community as public deliverable.

Based on the technology status and literature review, two hybrid DC CBs (IGBT and thyristor based) are selected. These two DC CBs have some similar components but are completely different in their current breaking strategies. Both DC CBs are composed of three principal branches; one for conducting the current in normal operation (load branch), the other for commutating the fault current (commutation branch) which may consist of several parallel current paths, and the last one for energy absorption and extinguishing the fault current.

Both hybrid DC CBs are studied in some depth including design and selection of parameters. It is concluded that this system level model should include:

1. The normal current branch and its main components,
2. The main breaker branch(es) with all main components,
3. Energy absorption branch
4. The residual current breaker,
5. The opening sequence controller,
6. The closing sequence controller,
7. The self-protection which incorporates overcurrent and thermal protection,

Both DC CBs are modelled in PSCAD and EMTP. The performance of these DC CBs are simulated under the following circumstances:

- Opening on grid order
- Closing/Reclosing on grid order
- Reclosing in fault
- Opening on self-protection
- Simulation with different parameters

The test system includes a fixed DC voltage supply, the DC CB and a load. The switching signals, the currents and voltages of the branches and the junction temperature of the IGBT and thyristor modules are monitored and results confirm good model accuracy. Some parameter variation is also tested, including extreme values for series inductance and responses confirm that models are adequately robust.

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ABBREVIATIONS

ABBREVIATION	EXPLANATION
DC	Direct Current
AC	Alternating Current
CB	Circuit Breaker
DCCB	Direct Current Circuit Breaker
HDCCB	Hybrid Direct Current Circuit Breaker
HVDC	High Voltage Direct Current
DCL / DCR	DC Current Limiting Reactor
IGBT	Insulated Gate Bipolar Transistor
VSC	Voltage Sourced Converter
WP	Work Package
UFD	Ultra-Fast Disconnector
RCB	Residual Current Breaker

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1 INTRODUCTION

Equation Chapter 1 Section 1

1.1 BACKGROUND

DC circuit breakers have not been used at transmission levels since almost all the VSC-HVDC systems have been developed as point to point systems [1]-[4]. A DC fault in a point-to-point HVDC can be isolated by tripping the AC circuit breaker at both terminals. Since all the VSC-HVDC links except Caprivi link, operate with DC cables, DC faults are permanent and therefore tripping of the AC circuit breaker will not further undermine the availability of a VSC-HVDC.

Recently however, there has been growing interest in developing DC transmission grids [1]-[5]. DC grids are becoming very attractive when multiple HVDC systems are being installed in close proximity. The operating flexibility and power security are enhanced if Multi-terminal DC or dc grid technologies are used. Total power loss and total transmission assets are reduced compared with multiple point-to-point HVDC system. The market participation and power flow interchange between different TSOs (transmission system operators) also become more flexible.

The DC grid concept confronts the challenge of DC fault detection and DC fault isolation [6]-[7]. Since the reactance of DC cables is negligible, a DC fault at any point in the DC grid will cause wide spread voltage collapse, DC overcurrent and VSC converter tripping if the DC fault is not cleared timely. Fast and low-loss DC circuit breakers are essential technology to facilitate reliable DC grids.

In recent years, transmission level DC Circuit Breakers have become commercially available [7]-[9]. There are three different DC CB technologies: Semiconductor-based DC CBs [10], mechanical DC CBs [11]-[13] and a combination of the semiconductor and mechanical DC CBs (the hybrid DC CB) [7]- [9],[13]-[18]. This report presents only the study and modelling of hybrid DC CBs, which are most suitable for DC grids and require most complex models. Task 6.2 covers study and modelling of active current injection mechanical DC CBs.

1.2 MOTIVATION AND MODEL APPLICATION

The models presented in the literature are very simple and may not be sufficiently accurate to represent factors such as subsystem parameters, dynamics and component limits, internal control limitations and interlocks, or self-protection of DC CB. In [19], the DC CB is modelled as a time delayed ideal switch. In [20] and [21], a simplified model of hybrid DC CB considering commutation process from the commutation branch to the load branch is used. In [22], the DC CB is modelled as an ideal switch with 90mH series reactor.

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Because of complexity of hybrid DC CBs, and the significance of DC grid protection, DC grid developers are looking for sufficiently detailed and accurate DC CB models. The models should be able to represent DC CB interaction with the DC grid. Therefore the internal components and control system should be sufficiently detailed to enable EMT-type (Electro Magnetic Transient) studies such opening/closing operation, repeated operations, transient currents and voltages, changes in parameters, exposure to operating conditions beyond design limits, and failures in grid-level protection system.

This task aims to develop accurate system-level model for hybrid DC CBs to facilitate DC grid fault study, protection system development and transient studies involving protection operation. More detailed component-level modelling will be performed in subsequent tasks.

1.3 REPORT OVERVIEW

The remainder of this report is organized as follows. In chapter 2, a brief study on DC grids, faults and DC CBs to isolate faults in DC grids is presented, but also the main aspects of IGBT-based and thyristor-based hybrid DC CBs. Chapter 3 presents the IGBT- based hybrid DC CB including the breaker's structure, components' characterisation, opening and closing sequences (under normal and fault conditions) and simulation results. The thyristor-based hybrid DC CB design, opening and closing sequences and simulation results are presented in chapter 4. The conclusion is presented in chapter 5.

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2 DC CIRCUIT BREAKERS IN DC GRIDS

2.1 INTRODUCTION

Equation Chapter (Next) Section 1

HVDC links have many advantages compared to AC systems for long-distance power transmission such as higher power transfer over longer distance and lower losses.

The primary motivation for DC grid development is the need to interconnect multiple HVDC links located in close proximity, and to enable power trading between all terminals. This brings benefits of better utilization of assets, better reliability and security of power transfer, better efficiency, enhanced power trading and operating flexibility, all the advantages of interconnected systems (reserve sharing, control, etc.) [26].

2.2 DC GRID PROTECTION

The main challenge in DC grid development is the protection system, which is much more challenging compared with AC systems.

Because of capacitive discharge of cables and converters in DC grids, the DC fault current rises very fast and reaches a very high value within few milliseconds. In order to prevent the fault to spread over a wide region, the protection system in a DC grid should be very fast in detecting and isolating the fault. Additionally, the selectivity of the protection system is another important criterion, i.e. it should be able to trip only the faulty part alone so that the remaining part of the DC grid can still survive and transmit power [26].

2.3 DC CBS IN DC GRIDS

DC CBs are essential building blocks for DC grids whenever selective protection is required. Without fast-acting breakers capable of interrupting and isolating DC faults, the DC system voltage will collapse and the effects of the fault will propagate deep throughout the grid due to the low resistive network. Even if the fault current is limited by means of active converter control, the faulted section of the network must still be isolated until the DC system voltage is re-established and power transfer can resume [30].

Tripping the converter AC breakers is equally unattractive since all connected converter stations' AC breakers must be tripped to clear a single DC fault. This would imply an interruption of electrical power transfer at all rectifying (feeding) or inverting (receiving) terminals in the DC network which for most network configurations would be unacceptable [30].

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Semiconductor based DC breakers easily overcome the limitations in operation speed but generate large transfer losses typically in the range of 30% of the losses of a voltage source converter station. Hybrid DC breakers are proposed to overcome these obstacles in HVDC grid applications [26], [29].

2.4 IGBT-BASED HYBRID DC CB

Figure 2.1 shows bi-directional IGBT- based hybrid DC CB [7]. The IGBT- based hybrid DC CB combines the switching capability of power electronics (IGBTs) with the low losses of mechanical switchgear in that the current does not traverse the semiconductors in the main breaker unless it should be interrupted. This is achieved by means of a mechanical bypass path consisting of an ultra-fast disconnecting switch (UFD) and a load commutation switch (LCS) connected in series. The load commutation switch commutates the current from the bypass branch into the parallel main breaker prior to interruption and ensures that the UFD can separate its contacts at virtually zero current stress [30].

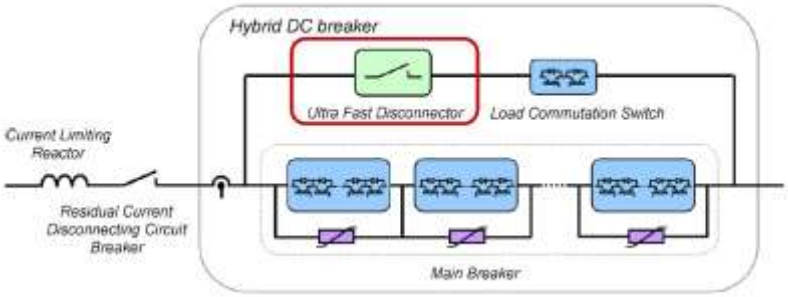

Figure 2.1 The schematic of IGBT- based hybrid DC CB [7]

2.5 GE HYBRID DC CB

The thyristor-based hybrid DC CB includes the same components of the IGBT- based DC CB for the load branch (UFD and LCS), the current limiting reactor and the residual current breaker (RCB). Figure 2.2 shows unidirectional thyristor-based DC CB [29]. The main difference between the thyristor-based and IGB-based DC CBs is in the main breaker branch. The thyristor-based DC CB uses several parallel branches of thyristors in the main breaker. Each branch has its own capacitor bank and builds up the Transient Interruption Voltage in a series of stages. The surge arrester across each capacitor limits the voltage level of each branch. The last branch with the main surge arrestor across extinguishes the fault current.

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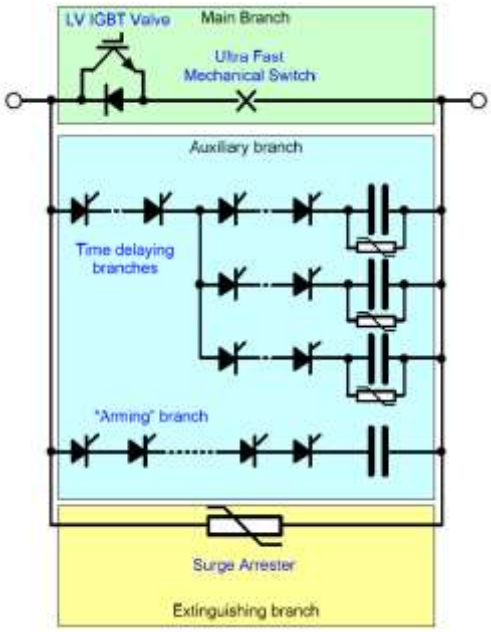

Figure 2.2 The schematic of thyristor-based hybrid DC CB [16]

2.6 DC CB SELF-PROTECTION

The self-protection should trip the DC CB if the temperature reaches (or is expected to reach) levels that will likely lead to destruction of some of the DC CB subunits. This may happen if

1. the grid-level protection failed to operate under DC fault conditions, or
2. if there is prolonged overload, or
3. if open-close cycle is too short.

The self-protection is required with hybrid DC CBs because of limited rating and high cost of DC CB components. It should be considered in basic DC CB modelling since it can interfere with grid protection systems.

Self-protection is activated based on both:

1. The fault current level which is relevant for fast current rise with low-impedance faults, and
2. The junction temperature of the semiconductor switches which is relevant for high-impedance faults or for high-frequency open-close operation.

The self-protection which operates on fault current level trips the breaker for low-impedance faults (including internal DC CB faults) when the fault current rises very fast and the valves in the commutation branches will be mostly stressed. For a given maximum interrupting current I_{trip_sp} the trip level I_{pk_sp} is then calculated internally based on the nominal DC voltage V_{dcN}, the current limiting inductor L_{dc} and the fault current interruption time T_{int}:

$$I_{pk\_sp} = I_{trip\_sp} - T_{int} V_{dc} / L_{dc} \quad (1.1)$$

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Tripping the DC CB at the above level guarantees the fault current is kept below maximum interrupting current accounting for all delays in the DC CB operation.

The junction temperatures of the semiconductors are calculated based on their internal power loss and transient thermal impedance. If the calculated junction temperature exceeds the limit 120ºC, the DC CB will be tripped to prevent burning the semiconductors.
Also, closing sequence can not commence unless valve temperatures are suffcienty low (belwo T_{limit}). This self-protectipon check is necessary to ensure that DC CB is ready for the next open command.

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3 MODELLING IGBT-BASED HYBRID DC CB

Equation Chapter (Next) Section 1

3.1 STRUCTURE OF IGBT-BASED HYBRID DC CB

Figure 3.1 shows the structure of IGBT- based hybrid DC CB. It is composed of the following main components:

- An ultra-fast Disconnector (UFD) S_1
- A residual current breaker (RCB) S_2
- Load commutation switch (LCS) (IGBT valve T_1)
- Main Breaker (MB) (IGBT valve T_2)
- surge arrester across valve T1 as nonlinear resistors with specified I-V table,
- Energy absorption element (Main surge arrester as nonlinear resistor with specified I-V table)
- A series inductor L_{dc} to limit the DC fault current

Note that the snubber circuit of the IGBT modules are not modelled here and will be considered in this system-level modelling.

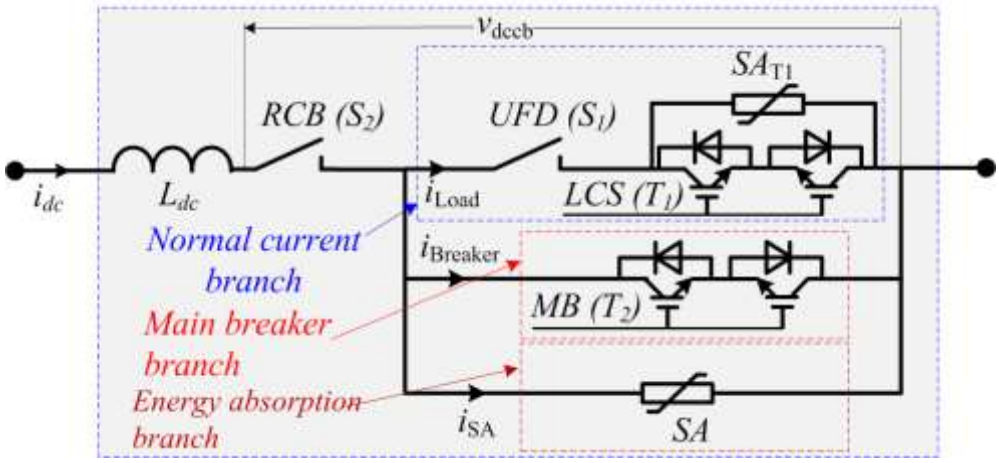

Figure 3.1 Structure of IGBT- based hybrid DC CB

In normal operation, both switches S_1 and S_2, and also valves T_1 and T_2 are closed. However, because of much smaller resistance of load branch compared to commutation branch ($R_{T1} << R_{T2}$), the DC current passes through the load branch; i.e $i_{breaker} \approx 0$ and $i_{load} \approx i_{dc}$.

On receiving the trip order from grid protection system, the valve T_1 is turned off and the fault current commutates to the commutation branch. The UFD S_1 will be opened when it's current drops below residual

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chopping current I_{res}. The valve T_2 will then be opened when S_1 is fully opened and the fault current commutates to the surge arrester SA. The fault current will be finally extinguished by the counter voltage of the arrester and the RCB S_2 interrupts the arrester leakage current when it drops below I_{res}.

The closing sequence is in reverse order. All valves and switches are open. The closing sequence would be S_2, T_2, S_1 and T_1.

The detailed description of these sequences and the system design of the components are given later in this chapter.

3.2 COMPONENT CHARACTERISATION

3.2.1 ULTRAFAST DISCONENCTOR S_1

This switch is an ultrafast mechanical switch with operating time around $T_{mec} \approx 2\ ms$. This switch can open only if its current, $i_{breaker}$, is below residual (chopping) current I_{res} which is commonly around $I_{res} \approx 0.01\ kA$.

3.2.2 RESIDUAL CURRENT BREAKER S_2

The RCB S_2 is a slow mechanical switch with operating time $10\ ms < T_{res} < 30\ ms$ and the chopping current I_{res} similar as with S_1.

3.2.3 LOAD COMMUTATION SWICTH (VALVE T_1)

The IGBT valve T_1 is the main valve that passes the DC current in both normal operation and early stage of DC fault. Therefore, the current rating of T_1 should be larger than breaker rated current. The voltage rating of T_1 is determined by the voltage drop across T_2 under the maximum DC fault current. Therefore the voltage rating of T_1 should be at least $R_{T2}*I_{fpk}$ where I_{fpk} represents the maximum DC fault current and R_{T2} is the ON state resistance of valve T_2.

Usually a 3X3 matrix configuration of IGBTs is used for valve T_1.

3.2.4 MAIN BREAKER (VALVE T_2)

The IGBT valve T_2 should pass the fault current for at least the opening time delay of S_1 (T_{mec}). The fault current would rise typically from around 2 p.u. up to the interrupting current. Although this current is high, the time is very short. The self-protection monitors the junction temperature of T_2 and blocks when the temperature exceeds the limit. The voltage rating of T_2 is determined by the grid DC voltage level and the arrester protection level. Usually a high number of IGBTs should be connected in series to achieve the required voltage rating of T_2

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in HVDC applications. A press pack design helps to reduce stray inductance in such applications with a high number of series IGBTs.

The valve design for IGBT hybrid DC CB has undergone two stages:

1. Intially, standard IGBT switches StackPak IGBT 5SNA 2000K450300 (4.5kV, 2.0kA) were used [7]. This switch has approximately 0.85mOhm ON-state slope and enables peak current interrupotion of around 9kA.
2. In the improved deign, new BIGT (Bimode IGBT) switches were employed [31], [32]. They consist of 6 pararllel connected submodules giving total current of 3kA with around 0.43mOhm ON-state slope. This switcth enables peak current interruption of over 16kA. This improved deisgn will be assumed in the report.

The design of valves T_1 and T_2 can be illustrated by an example. Assume that the voltage rating of the hybrid DC CB is 320 kV with nominal load current 2kA. If the ABB BIGT (Bi mode IGBT) (4.5 kV and 3.0 kA) [31] module is adopted, the number of series IGBTs in valve T_2 would be N=(320/4.5)*2=71.1*2.25=160 (with voltage margin 2.25). Note that this number will be doubled if the breaker is bidirectional. Considering the ON resistance R_{on}=0.43 mΩ [31] for each single IGBT/diode, the ON resistance of valve T_2 is equal to

$$R_{T2} = NR_{on} = 160 * 0.00043 = 0.069\Omega \tag{2.1}$$

Considering on-state voltage u_{CE0}=1.6V for each single IGBT/diode, and peak interrupting current I_{pk}=16 kA, the maximum voltage drop across T_2 (voltage stress on T_1) is

$$V_{T2\_\max} = Nu_{CE0} + R_{T2}I_{pk} = 160 * 0.0016 + 0.068 * 16 = 1.34kV \tag{2.2}$$

This implies that one BGBT would suffice in the valve T_1 in each direction in order to meet the voltage requirement. A 3x3-matrix configuration of IGBT module is usually used in valve T_1. This 3x3-matrix IGBT configuration ensures sufficient voltage margin for turn off transients and reduces the power loss of T_1 at the increased capital cost. Considering the ON resistance and on-state voltage of the selected IGBT, the conduction loss for load commutation swicth T_1 would be

$$P_{T1} = 9 * \left(u_{CE0} \left(I_{dcN} / 3 \right) + R_{ON} \left(I_{dcN} / 3 \right)^2 \right) \approx 11.3kW \tag{2.3}$$

3.2.5 SURGE ARRESTERS SA AND SA_{T1}

The two surge arresters SA and SA_{T1} will be assumed with the same per-unit I-V characteristics (given as default characteristics in PSCAD) but with different voltage rating. Table 3.1 gives the I-V characteristics data for the arresters and Figure 2.2 shows the corresponding I-V curve. The rated voltage of the surge arrester is 1 p.u. which corresponds to leakage current of around 0.9A. The clamping voltage of the surge arrester is at voltage 1.948 p.u. and current 2.8 kA.

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Table 3.1 I-V characteristics of surge arresters

I (kA)	0.001	0.01	0.1	0.2	0.38	0.65	1.11	1.5	2.0	2.8	200.0
V (p.u.)	1.100	1.600	1.700	1.739	1.777	1.815	1.853	1.881	1.910	1.948	3.200

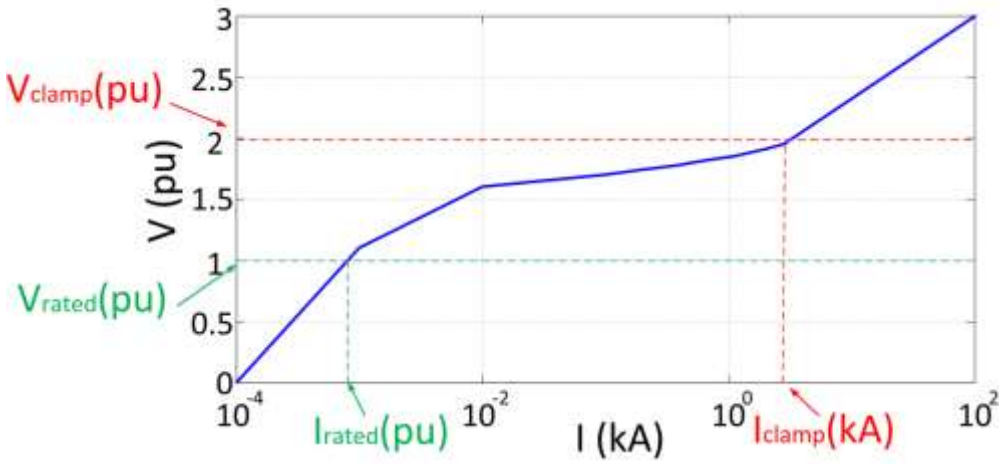

Figure 3.2 I-V curve of surge arresters

The voltage rating of SA (across T_2) is selected in such way that it's clamping voltage (~2 p.u.) equals around 1.5 times of the nominal DC line voltage. The clamping voltage of SA_{T1} should be below the voltage rating of T_1 to protect the valve from overvoltage damage. On the other hand, it should be higher than a minimum voltage level to keep the current in the UFD S_1 less than I_{res} to allow the switch to open when T_1 is OFF. This minimum voltage level is determined by the I-V characteristics of the SA, the mechanical time delay of UFD S_1 and the stray inductance of the valve.

When the valve T_1 is turned off, the current of UFD S_1 keeps increasing for some time due to stray inductance of connections to the valve T_1. Usually the lower voltage rating of SA_{T1} shortens the time that the SA_{T1} reaches to its smaller piece-wise resistances for the same stray inductance current. If the voltage rating of SA_{T1} is selected too low, the current of the stray inductance puts the SA_{T1} on its smaller resistance segment. If this small resistance of SA_{T1} is comparable to R_{T2}, the current in the load branch rises more than I_{res} before the contacts of S_1 separate. This prevents S_1 to be fully opened and the fault current will not be interrupted.

Simulation results show that the voltage rating of SA_{T1} (with PSCAD default I-V characteristics) should be higher than 5 kV to keep the current in S_1 below I_{res} after tripping T_1. The voltage rating of T_1 (as a 3x3 block of IGBT with the IGBT module 5SNA 2000K450300) is 13.5 kV. Therefore, the voltage rating of SA_{T1} can be selected at 6 kV.

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The surge arrester energy is calculated by integrating its power during the conduction time T_{ON}, and should be lower than the maximum rated energy of the surge arrester

$$E_{SA} = \int_0^{T_{ON}} v_{SA} i_{SA} dt \tag{2.4}$$

Where T_{ON} is the conduction time of the surge arrester. The surge arrester rated energy must be higher than E_{SA}.

3.2.6 SERIES INDUCTOR L_{DC}

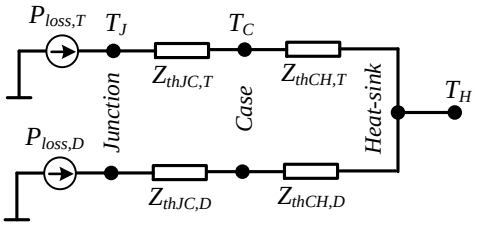
The series inductor L_{dc} is used to limit the rate of rise of the DC fault current. The inductance prevents the fault current to exceed DC CB rated interrupting current considering delays (relay time and internal current commutation time) in DC CB opening. DC CB design imposes minimum value for L_{dc}. In addition, inductance L_{dc} is an important parameter in DC grid protection. DC grid protection may require larger L_{dc}.

3.2.7 THERMAL MODEL FOR VALVES

This section provides a simple thermal model of the IGBT valves T_1 and T_2. The current for the two valves T_1 and T_2 are different; the current of T_1 is almost constant load current with a small peak at very short time while the current of T_2 is almost zero with a large peak for duration of around 2 ms (T_{mec}). In addition, T_1 is usually equipped with water cooling system while T_2 uses air-cooling system. These assumptions result in different junction temperatures for the IGBT modules of the two valves.

Figure 3.3-a shows a simplified equivalent thermal model of an IGBT module [33]. The $P_{loss,T}$ and $P_{loss,D}$ are the power loss of IGBT and diode. The $Z_{thJC,T}$, $Z_{thCH,T}$, $Z_{thJC,D}$ and $Z_{thCH,D}$ are the thermal junction-case and case-heatsink impedances for IGBT and diode. The T_J, T_C and T_H are respectively the temperature of junction, case and heatsink.

Considering that the thermal impedances for IGBT and diode are almost equal ($Z_{thJC,T}=Z_{thJC,D}$ and $Z_{thCH,T}=Z_{thCH,D}$,), the model can be simplified further as is shown in Figure 3.3-b. The P_{loss} is the maximum power loss of the IGBT module because the current passes only through either IGBT or diode ($P_{loss}=\max(P_{loss,T},P_{loss,D})$) and the impedances are $Z_{thJC}=Z_{thJC,T}$ and $Z_{thCH}=Z_{thCH,T}$.



(a) Simplified equivalent thermal model of an IGBT module

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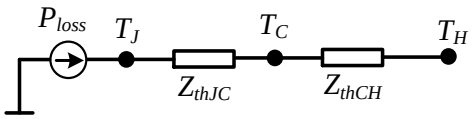

(b) Further simplified equivalent thermal model of an IGBT module

Figure 3.3 Equivalent thermal circuit diagram for an IGBT module (water cooling system)

When a water cooling system is employed (for valve T_1), the heatsink temperature is usually assumed to be constant. The thermal impedances $Z_{thJC,T}$, $Z_{thCH,T}$, $Z_{thJC,D}$ and $Z_{thCH,D}$ can be found in the IGBT data sheet provided by the manufacturer. The exact thermal data for new BIGT can not found but the thermal impedances for a similar conventional IGBT module are [34]:

$Z_{thJC} = Z_{thJC,T} = Z_{thJC,D} = 4$ k/KW

$Z_{thCH} = Z_{thCH,T} = Z_{thCH,D} = 1$ k/KW (2.5)

The IGBT power loss for valves T_1 and T_2 contains just conduction loss (no switching loss). The instantaneous and average conduction losses of IGBT can be calculated as:

$$P_{loss}(t) = u_{CE0} \cdot i_{IGBT}(t) + R_{ON} \cdot i_{IGBT}^2(t)$$
$$P_{loss\_ave} = U_{CE0} \cdot I_{IGBT\_ave} + R_{ON} \cdot I_{IGBT\_ave}^2 \quad (2.6)$$

Where R_{on} is the ON resistance for each BIGBTswitch (R_{on}=0.435 mΩ,) and U_{CE0} is the ON-state voltage (U_{CE0}=1.6V).

If the average load current of the HYBRID DC CB is 2 kA, and assuming a matrix of 3x3 BIGBT switches in valve T_1 and equal sharing of load current between the parallel IGBTs, the current of each BIGBT will be 0.67 kA. The power loss of each BIGBT switch is calculated using (2.6) as P_{loss_ave}=1.26kW.

Considering that the heatsink temperature is fixed at 40 ^oC (T_H = 40 ^oC), the junction temperature will be

$T_J = P_{loss} * (Z_{thJC} + Z_{thCH}) + T_H = 46.3\ ^oC$ (2.7)

which is much lower than the maximum junction operating temperature T_{J_max} =125 ^oC.

The above calculation adopts steady-state thermal impedance that is valid if the power loss is constant. For transient power loss when current is commutating between T_1 and T_2, the transient thermal impedance should be used. Figure 3.4 shows the transient thermal impedances Z_{thJC} for conventional IGBT/diode of IGBT module 5SNA 2000K450300 [34]. It is seen that the impedances are settled to 4 K/KW (consistent with earlier mentioned values) for time longer than 2s and to lower values for shorter times. For example, the impedances are 10 times smaller (0.4 k/KW) if the IGBT current passes only for around 2 ms. It is also seen that the impedances are almost equal for IGBT and diode.

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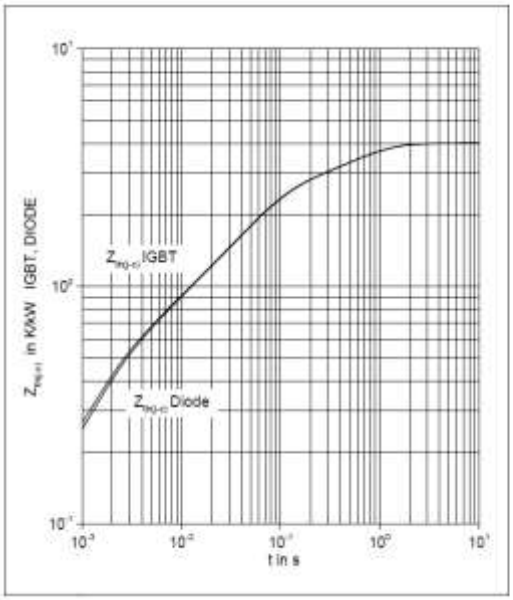

Analytical function for transient thermal impedance:

$$Z_{th\,(j\text{-}c)}(t) = \sum_{i=1}^{n} R_i\left(1 - e^{-t/\tau_i}\right)$$

	i	1	2	3	4	5
IGBT	R_i in K/kW	1.601	1.765	0.358	0.328	
	τ_i in s	0.581	0.059	0.006	0.001	
DIODE	R_i in K/kW	1.606	1.759	0.357	0.323	
	τ_i in s	0.584	0.059	0.006	0.001	

Figure 3.4 Thermal impedance Z_{thJC} vs time [34]

Figure 3.5 shows the block diagram of the junction temperature calculation. The power loss P_{loss} is multiplied with the IGBT transient thermal impedance representing by 4 first-order filters. The gain and time constant of these filters are given in Figure 3.4. The filter output is multiplied by gain K_1 to consider either the impedance Z_{thCH} (for T_1 with water cooling system) or K_1=1 (for T_2 with air cooling system). The result will then be added with T_0 which is either the heatsink temperature for T_1 or the air temperature for T_2.

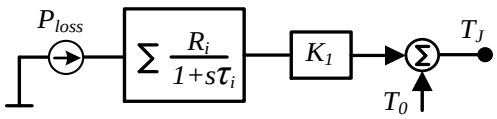

Figure 3.5 Dynamic junction temperature for an IGBT module

3.3 OPENING SEQUENCE

The opening sequence starts when the hybrid DC CB is in normal operation (all switches and valves are closed) and a trip order is received. This trip order comes from grid-level, self-protection or driver-level. The self-protection trip order is issued when the junction temperature of the IGBT modules goes over 120 ºC and/or the fault current rises over specified threshold, which is commonly 90% of peak interrupting current (I_{pk_SP}=14.4 kA). The driver level protection order is the last-defence protection order which trips the breaker when the fault current rises to peak interrupting current (I_{pk}=16 kA). Activation of driver level protection will diseable DC CB, and may lead to destruction.

The opening sequence is comprised of four main steps as summarized in Table 3.2.

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Table 3.2 Opening sequence of IGBT- based hybrid DC CB

	Inputs measurement	Action	Comment
1	Is trip order received? (from grid-level or self-protection or driver-level)	Open T_1	The fault current commutates to T_2.
2	(Is T_1 OFF?) & ($i_{breaker}$<I_{res}?) & (Is S_1 closed?)	Open S_1	A mechanical delay T_{mec} is applied in model as S_1 takes T_{mec} to be fully open. The condition "Is S_1 closed?" bypasses the T_{mec} delay in the model if S_1 has been already opened. This might happened if the DC CB tries to reclose in fault condition.
3	Is S_1 fully opened?	Open T_2	The fault current commutates to the surge arrester SA. The fault current will be extinguished because of counter voltage of SA.
4	(Is T_2 OFF?) & (i_{dc}<I_{res}?) & (Is Reclosing disabled?)	Open S_2	With the condition "Is Reclosing disabled?" the S_2 is kept closed in anticipation of closing signal shortly. A mechanical delay T_{res} is applied in model as S_2 takes T_{res} to be fully opened.

Figure 3.6 shows the flowchart of the opening sequence. The sequence might be triggered by grid protection, self-protection or driver-level protection. The condition "Is S_1 already opened?" bypasses the T_{mec} delay if S_1 has been already opened. This might happen if the DC CB closes (T_2) in fault condition and needs to open immediately.

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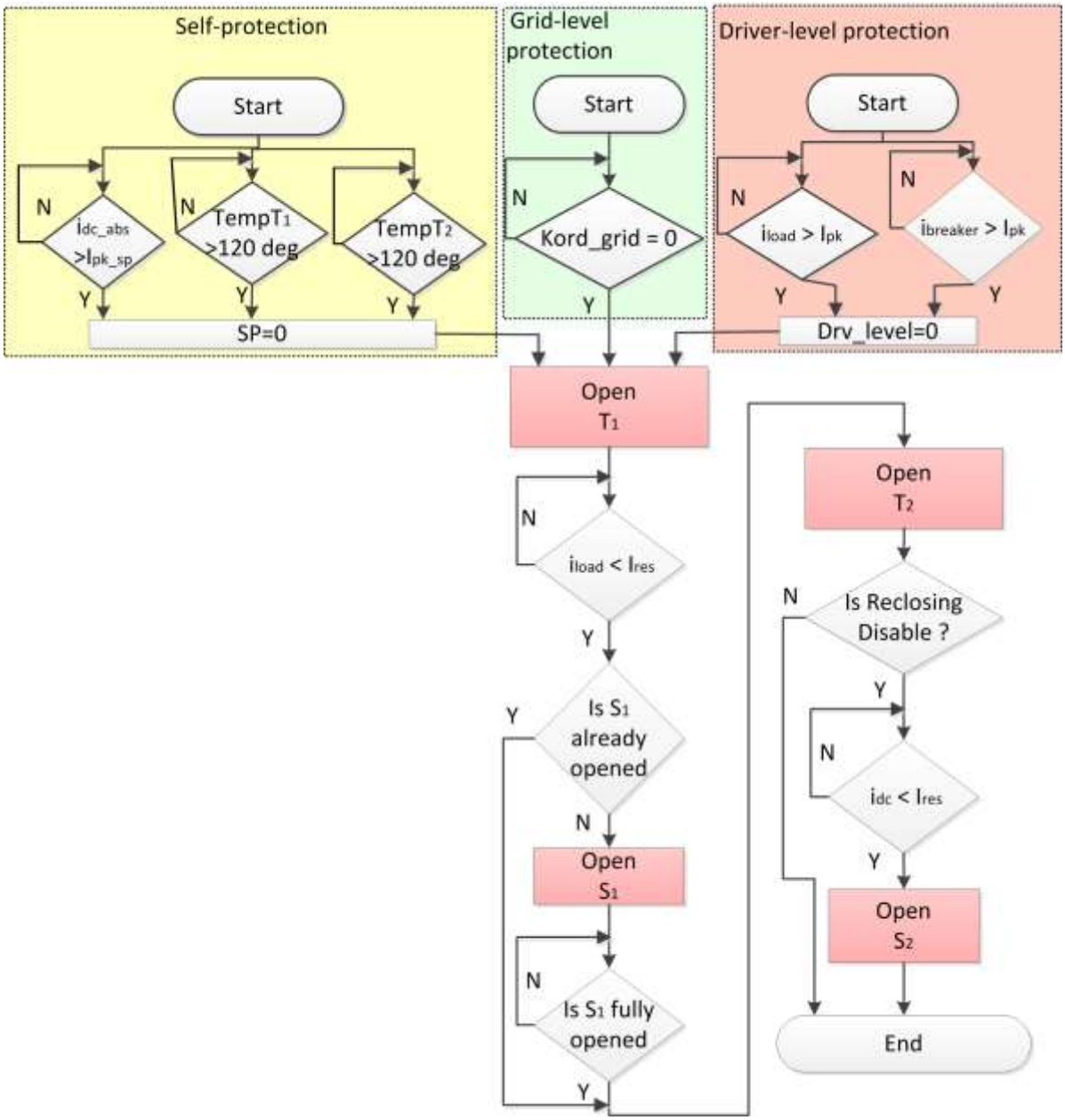

Figure 3.6 Opening sequence flowchart of IGBT- based HYBRID DC CB

Figure 3.7 shows the schematic of the hybrid DC CB for different steps of opening sequence with the corresponding typical current and voltage curve. It is assumed that reclosing is disabled. Figure 3.7-a shows the schematic of the hybrid DC CB for normal operation (and early stage of DC fault) and the typical current and voltage curves. The black lines indicate the branches that pass the current (either load or fault current) while the grey lines represent the off links. The ON and OFF modules are shown respectively in green and grey. The current is nominal load current and the voltage across the hybrid DC CB is zero. The current in T_2 does exist but is negligibly small compared with T_1 current.

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The DC fault is applied at t=0s and the current starts to increase. Once the current hits a limit, a trip order is sent to valve T_1 at $t=t_0$.

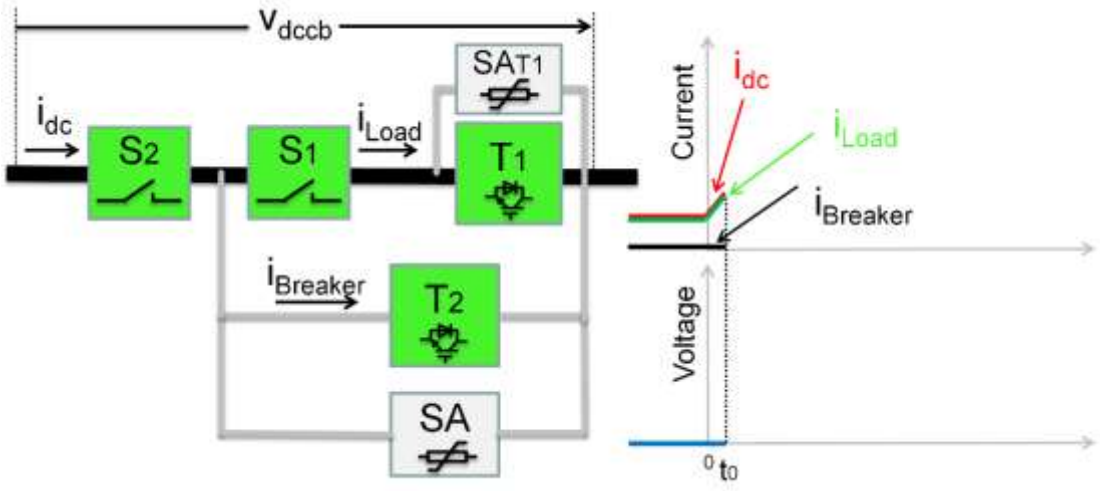

Figure 3.7-a Schematic of IGBT- based hybrid DC CB and corresponding current and voltages curves in normal operation and initial stage of opening sequence.

On receiving the trip order at $t=t_0$, the valve T_1 is opened and the current commutates to valve T_2 as is shown in Figure 3.7-b. The surge arrester SA_{T1} absorbs the inductive energy from the stray inductance in the main path and its voltage rises to the arrester voltage rating (few kV). The ultrafast mechanical UFD S_1 is triggered to be open when $i_{breaker} < I_{res}$ at $t \approx t_0$. The opening process lasts around 2 ms (T_{mec}). During this time, the fault current (in the valve T_2) increases as is shown in Figure 3.7-b. The orange colour of block S_1 indicates that it is opening.

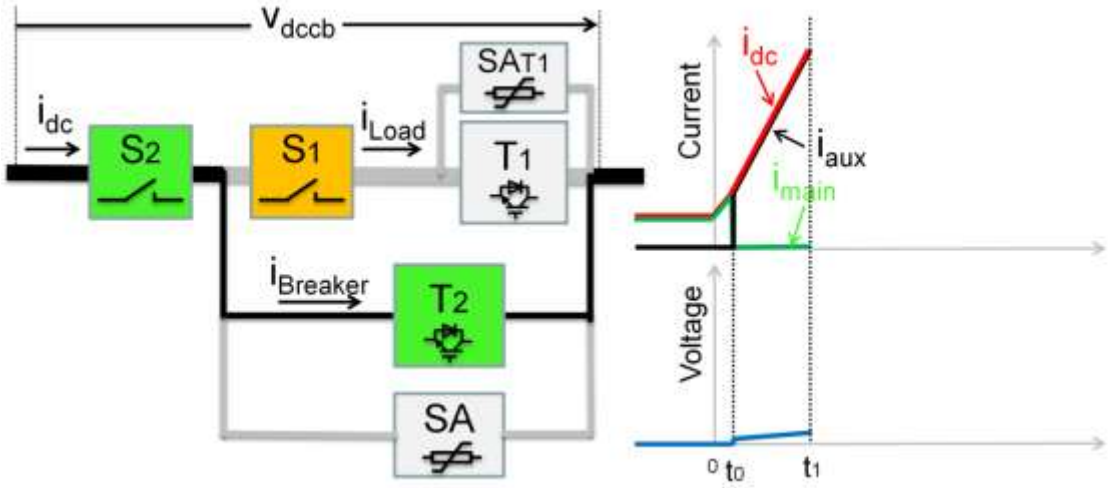

Figure 3.7-b Schematic of IGBT- based HYBRID DC CB and corresponding current and voltage curves in opening sequence (S_1 is opening)

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The valve T_2 is opened at $t=t_1$ when S_1 is fully opened. The fault current commutates into the surge arrester SA and the DCCB voltage jumps to around 2 p.u. The fault current will be extinguished by the counter voltage of the SA and the DCCB voltage decreases as is shown in Figure 3.7-c.

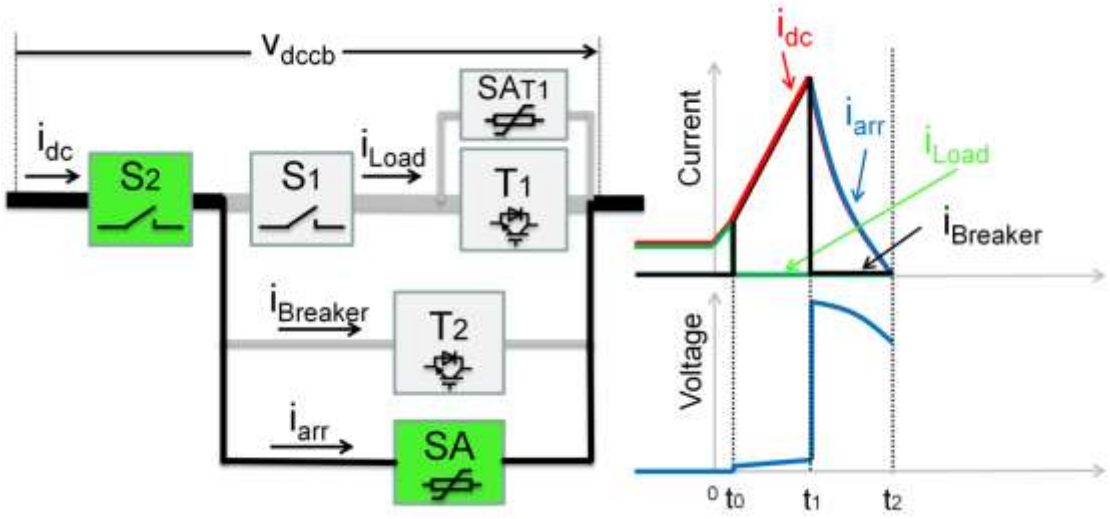

Figure 3.7-c Schematic of IGBT- based HYBRID DC CB and corresponding current and voltage curves in opening sequence (the surge arrester SA is conducting)

The RCB S_2 is triggered to be open when $i_{dc}<I_{res}$ at $t=t_2$ as shown in Figure 3.7-d. The opening process lasts around 30 ms (T_{res}). During this time, the fault current is very small (the leakage current of the SA). When the RCB S_2 is completely opened at $t=t_3$, no current passes through the DCCB as shown in Figure 3.7-e.

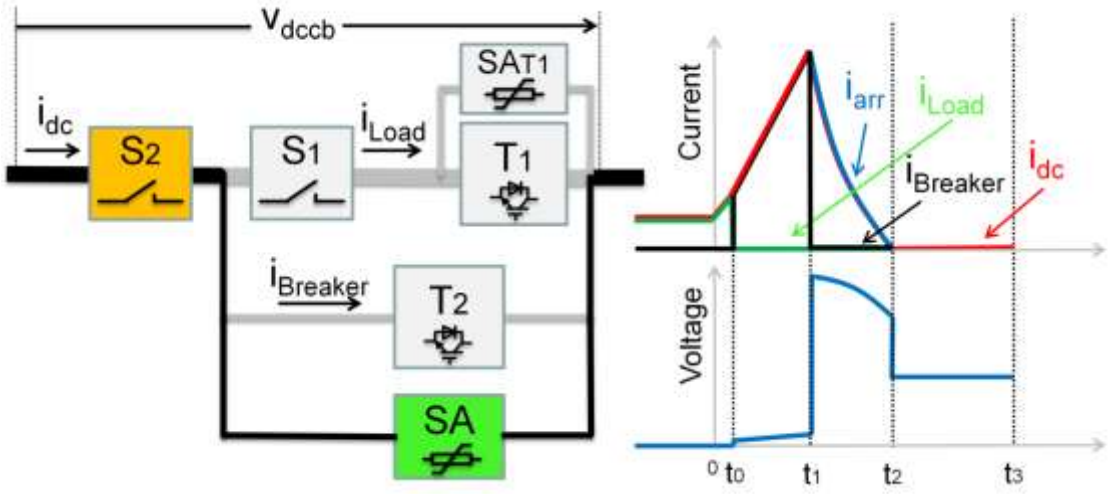

Figure 3.7-d Schematic of IGBT- based HYBRID DC CB and corresponding current and voltage curves in opening sequence (S_2 is opening)

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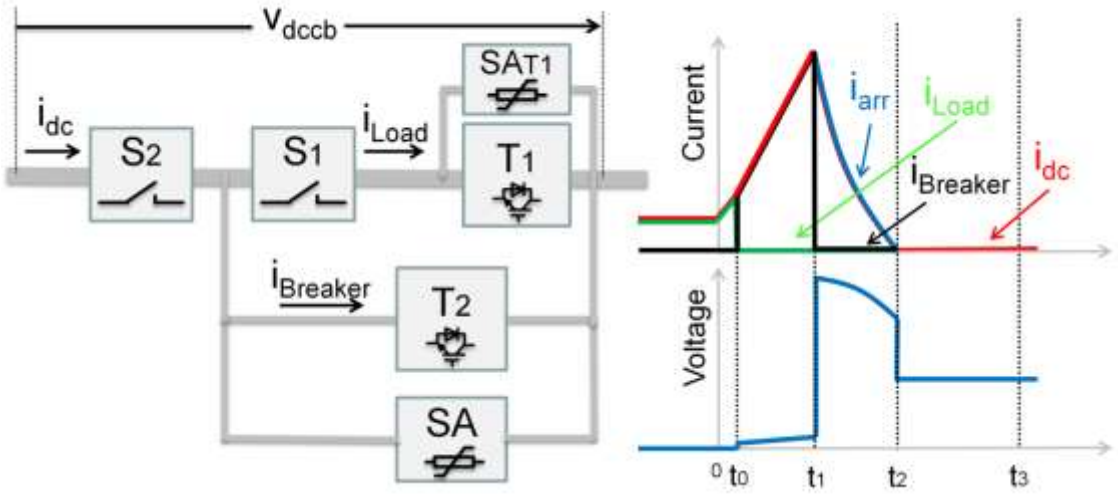

Figure 3.7-e Schematic of IGBT- based HYBRID DC CB and corresponding current and voltage curves in opening sequence (the HYBRID DC CB is fully open)

3.4 CLOSING SEQUENCE

The closing sequence starts when the hybrid DC CB is in fully open state (all switches and valves are open) and a closing order from grid-level is received. The closing/reclosing sequence is in reverse order of opening sequence, and it is summarized in Table 3.3.

Table 3.3 Closing sequence of IGBT- based HYBRID DC CB

	Inputs measurement	Action	Comment
1	Is closing order (Kord_grid) received? & (i_{dc}<I_{res}?) & (The junction temperature of T_1 and T_2 are below T_{limit}?)	Close S_2	A mechanical delay T_{res} is applied in model as S_2 takes T_{res} to be fully opened The condition (T_{T1} & T_{T2} < T_{limit}?) prevents closing if the junction temperature of the valves are still high.
2	Is S_2 fully closed?	Close T_2	The current starts to increase in T_2 branch
3	(Is T_2 ON?) & ($i_{breaker}$<I_{res}?)	Close S_1	A mechanical delay T_{mec} is applied in model as S_1 takes T_{mec} to be fully opened.
4	Is S_1 fully closed?	Close T_1	The current commutates to T_1

Figure 3.8 shows the flowchart of the closing sequence. The sequence is triggered if grid-protection order is received and there is neither self-protection nor driver-level protection trip. If the DC CB had been already tripped on receiving self-protection (SP=0) or driver-level protection (Drv_level=0), the closing will be blocked.

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The intial temperature check is required to ensure that DC CB will be ready for next open command. The value for T_{limit} is assumed as 50deg.

The time delay T_{delay} (which is calculated based on L_{dc}, V_{dcN} and the fault current level) is applied to check whether the closing is under fault or not. If it is under fault, a separate opening sequence is triggered (when the fault current hits the limit) and the fault signal becomes “1” again. This turns off T_2 while the closing sequence is waiting for T_{delay} thus avoiding next closing steps.

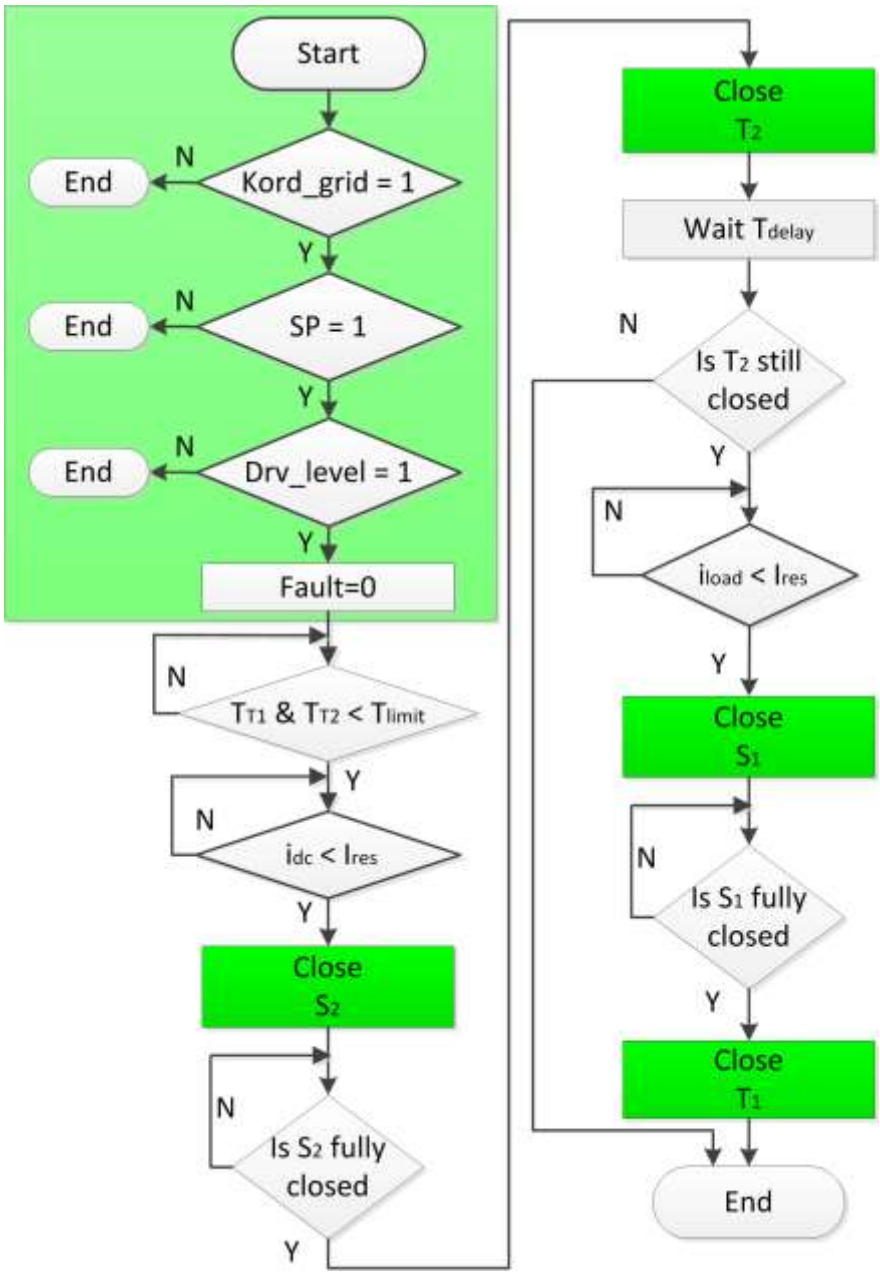

Figure 3.8 Closing sequence flowchart of IGBT- based HYBRID DC CB

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Figure 3.9 shows the schematic of the hybrid DC CB for different steps of closing under normal operation (no fault) sequence with corresponding current paths. If the reclosing is initiated under fault, the sequence will be terminated at Figure 3.9–b as mentioned in Figure 3.8 and the opening sequence will be triggered.

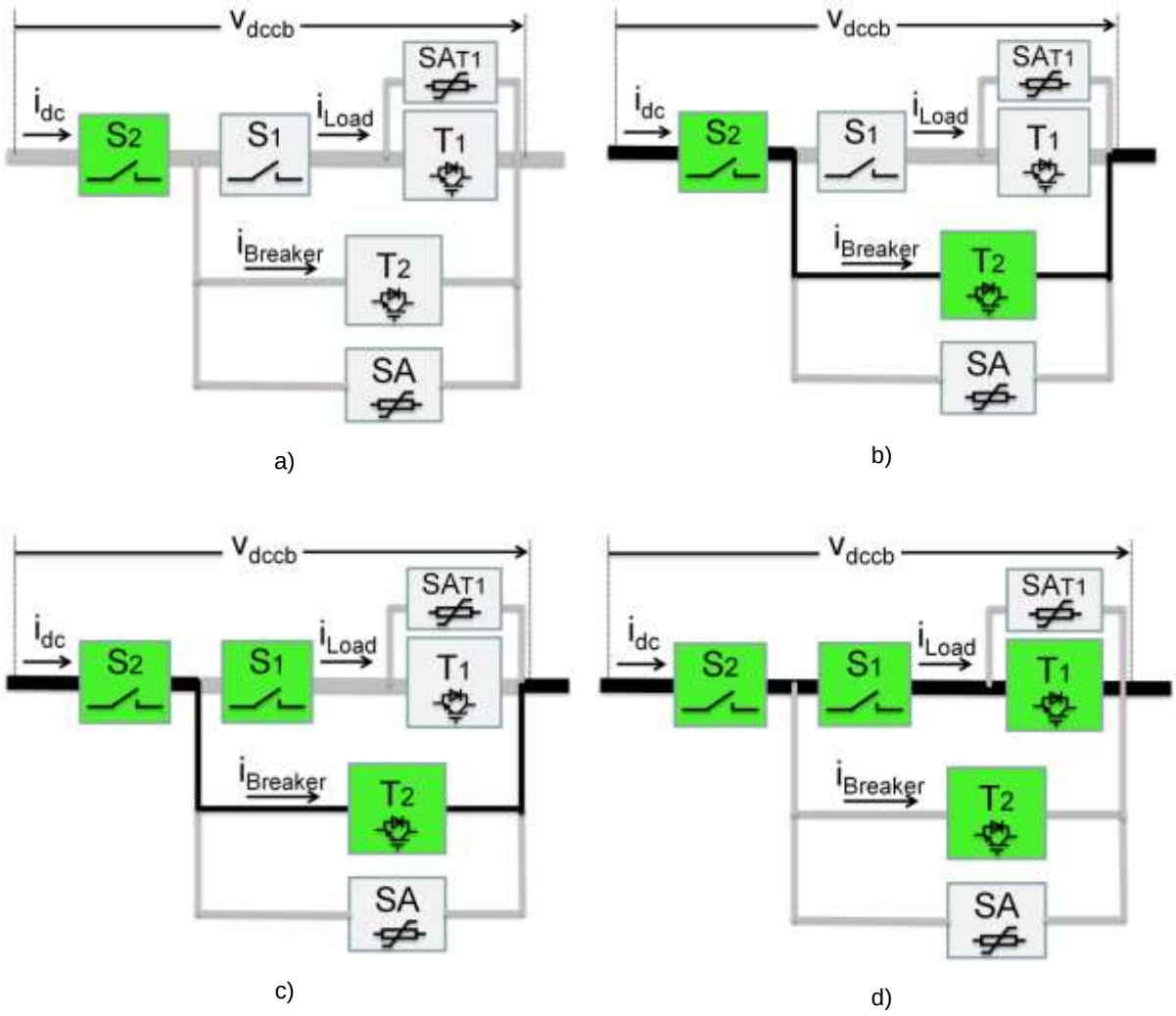

Figure 3.9 Block diagram of IGBT- based HYBRID DC CB in closing sequence

3.5 RECLOSING SEQUENCE

The reclosing sequence is initiated only if reclosing option is enabled. The open sequence (with reclose enabled) is similar to the open sequence but without opening S_2 as it is kept close in anticipation of closing order shortly. The grid protection sends the actual reclose signal.

In case of reclosing operation, the reclosing period T_{rec} is specified (typically T_{rec}=0.3s). The residual arrester current runs through S_2 for T_{rec} duration and this current increases the energy loss in the main surge arrester. If

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reclosing time is very short, then there could be a constraint on switch temparture, considering that cooling of valves may take several miliseconds.

3.6 PROACTIVE BREAKING

The proactive breaking capability has been reported with hybrid DC CB [7] however it has not been used much in system-level studies. It is decided that this function will not be included in the task 6.1 because of complexity, lack of information on component data, and complex interaction with grid-level protection.
It will be studied and modelled in the forthcoming task (T6.3) of WP6.

3.7 FAULT CURRENT LIMITING

The Fault current limiting has been reported with hybrid DC CB, but there is very limited information in public domain. This function will be studied and modelled in the next task (T6.3) of WP6.

3.8 MODEL USER INTERFACE

The IGBT- based hybrid DC CB consists of a number of series connected basic DC CB modules with ratings 80 kV and 2 kA. Considering the selected BIGBT module (4500V and 3000A) for this DC CB, the valve T_1 is usually composed of a matrix 3x3 of IGBTs, and the valve T_2 is comprised of 40 series IGBTs to withstand the voltage level 80 kV. The voltage rating of the main surge arrester is 60 kV (giving clamping voltage of 120kV).

The voltage rating of the DC CB can be increased by connecting a number of the main breaker (valve T_2) in series with one main surge arrester across each valve. For example, for a 320 kV HVDC, the IGBT- based hybrid DC CB is composed of one load branch (one valve T_1 and one UFD S_1) and four valves T_2 in series with a surge arrester across each valve T_2.

Table 3.4 shows the IGBT- based hybrid DC CB parameters and user is able to change each of these parameters using a user interface panel.
The basic data for IGBT are provided from a separate data file and can not be changed.

Table 3.4 IGBT- based hybrid DCCB parameters

Variable	Default value
V_{dcN} (Line DC voltage level)	320 kV
I_{dcN} (Normal DC current)	2.0 kA
Number of series IGBT in T_1	3
Number of parallel IGBT in T_1	3
Number of series IGBT in T_2	160

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I_{pk} (maximum interrupting current)	16 kA
I_{pk_sp} (self protection trip level)	14.4 kA
I_{res} (residual current for S_1 and S_2)	0.01 kA
T_{mec} (S_1 mechanical delay)	2 ms
T_{res} (S_2 mechanical delay)	30 ms
L_{dc} (DC series inductor)	0.15 H
Rated voltage (calmping voltage) of surge arrester SA_{T1}	6 kV (12 kV)
Rated voltage (calmping voltage) of main surge arrester SA	240 kV (480 kV)

3.9 RANGE OF PARAMETERS

Although user is able to change all the parameters of Table 3.4, some of them are usually implied by the DC grid ratings and the DC CB manufacturers determine others.

The series inductance L_{dc} is an important parameter that impacts DC CB operation but also the protection system. For a given DC CB, different L_{dc} may be used for different protection strategy, or as grid topology changes over time.
It is therefore important that DCCB model operates correctly for a range of L_{dc} values. It is expected that L_{dc} can be varied from a very low value of 50-80mH to a very large value 500-800mH. No minimal limit for L_{dc} is forced in the model. If user selects to small L_{dc}, then current will rise very fast and the DC CB will likely operate on self-protection or driver-level protection. Operation on driver-level protection or high-temperature should not be allowed in a good system design. Too high value for L_{dc} will give excessive heat dissipation.

3.10 SIMULATION VERIFICATION

Figure 3.10 shows the simple test system. Table 3.4 gives the test system and the hybrid DCCB parameters.

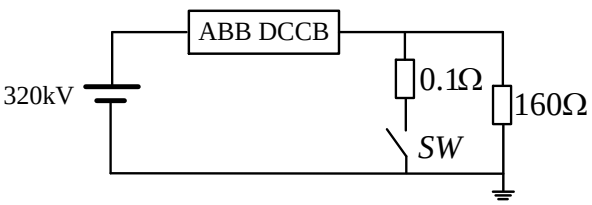

Figure 3.10 Test system

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The performance of the IGBT-based hybrid DC CB model is verified for following test cases:

- Opening on grid order
- Opening on self-protection order
- Closing on grid order
- Reclosing in fault
- Simulation with different parameters (L_{dc})

3.10.1 OPENING ON GRID ORDER

Figure 3.11 shows the switching signals of the opening sequence on receiving grid order. The DC fault is applied at 0.5s and grid-level protection sends trip signal when fault current exceeds 4 kA.

K_{grid} is the grid level signal. It is “1” in normal operation (closed) and becomes zero “0” if trip signal is sent. The signals SP and D_{rv_P} have the same range of values but detect the fault from self-protection and driver-level protection. The signal K_{ord} is logical AND of the above three signals and generates the fault order (if it becomes “0”). The switching signals T1, S1s, T2 and S2s represent the corresponding valve/switch status. The logic “1” represents the closed status and logic “0” is for open status.

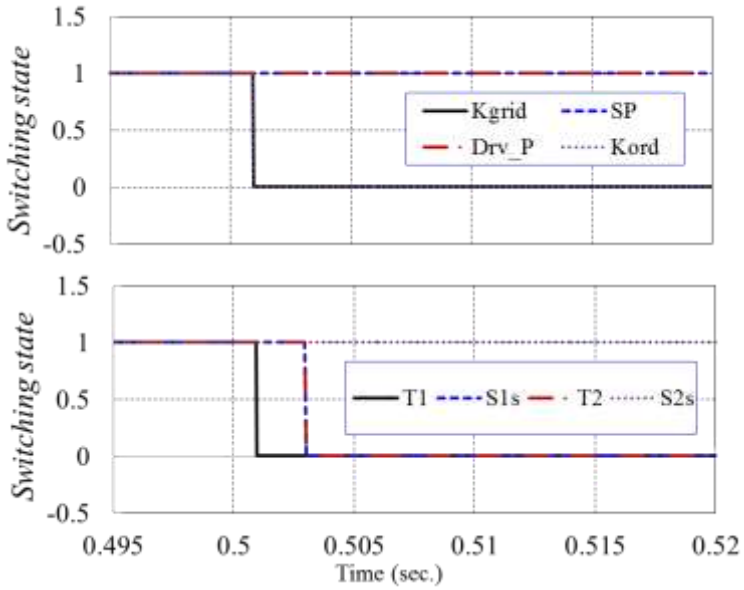

Figure 3.11 Switching signals (Opening on grid order)

Figure 3.12 shows the currents and voltages of the IGBT- based HYBRID DC CB of the opening sequence on receiving grid order. The labels for currents and voltages are shown in the circuit diagram in Figure 3.1.

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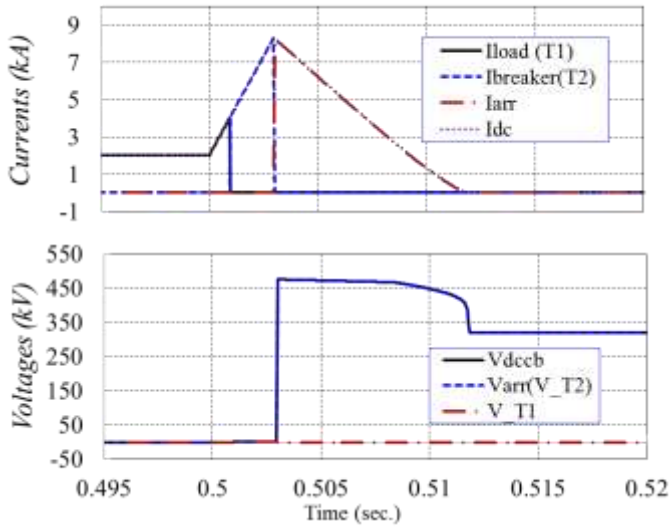

Figure 3.12 Currents and voltages (Opening on grid order)

Figure 3.13 shows the junction temperature of each IGBT module of valve T1 and T2 of the opening sequence on receiving grid order. The junction temperatures are calculated in PSCAD (and EMTP) based on the equations given in sections 3.2.7. It is seen that the temperatures are well below the limit 120 ºC.

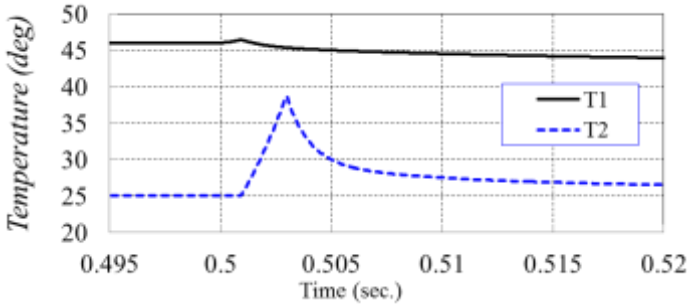

Figure 3.13 Junction temperature of the IGBT modules (T1 and T2) (Opening on grid order)

3.10.2 OPENING ON SELF PROTECTION

The DC fault is applied at 0.5s and the grid protection is disabled. Self-protection sends trip signal when fault current exceeds the threshold limit, anticipating that peak current will reach Ipk_sp=14.4kA accorindg to (1.1). Figure 3.14 shows the switching signals of the opening sequence on receiving self-protection order. It is seen that the signal Kgrid remains “1” and signal SP becomes “0” implying that the DC CB is tripped on self-protection. This can also be seen in Figure 3.15, which shows that the DC CB operating mode changes from “0” to “2” implying that the DC CB is tripped on self-protection at around t=0.504s.

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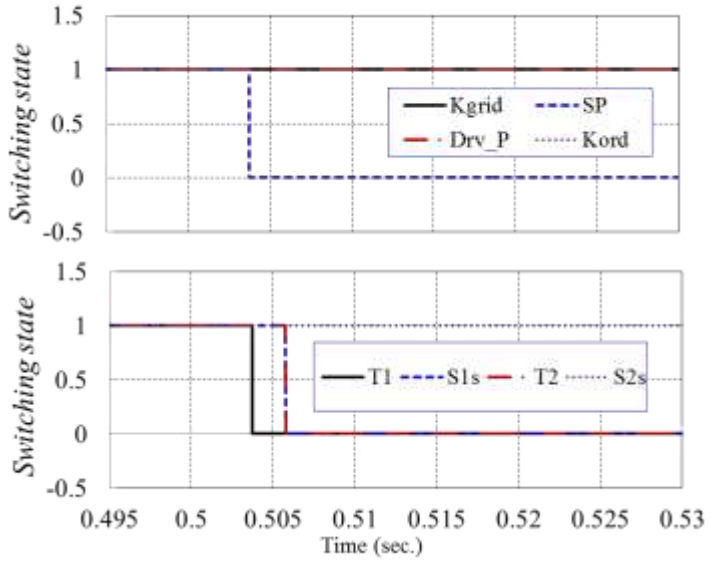

Figure 3.14 Switching signals (Opening on self-protection order)

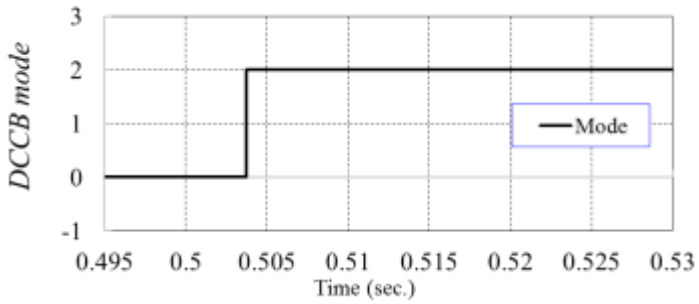

Figure 3.15 Operating mode (Opening on self-protection order)

Figure 3.16 shows the currents and voltages of the IGBT- based HYBRID DC CB of the opening sequence on receiving self-protection order. It is seen that the current commutates from the load branch to the commutation branch when it exceeds 9 kA. This trip level for self-protection is calculated internally based on the nominal DC voltage, L_{dc}, T_{mec} and the maximum current limit I_{trip_sp} (defined by user) as explained in section 2.6. This current limit is usually much higher than the grid order trip value (around 4 kA in previous tests). It is seen that the fault current remains below the user defined current limit I_{trip_sp} =14.4 kA. In case that grid protection is slow, or if L_{dc} is small, then self-protection may interfere with grid protection operation.

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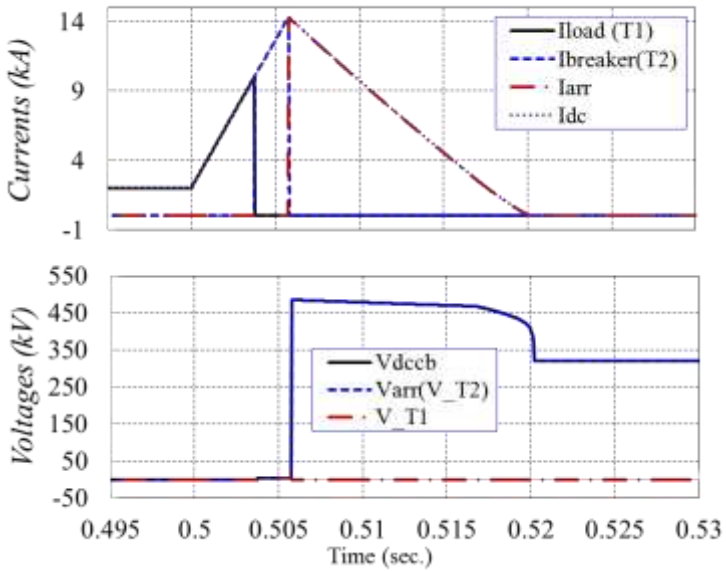

Figure 3.16 Currents and voltages (Opening on self-protection order)

Figure 3.17 shows the junction temperature of each IGBT module of valve T1 and T2 of the opening sequence on receiving self-protection order. The temperature of T2 reaches higher value compared to the results of opening on grid order (Figure 3.13) as expected. The fault current increases for approximately 2ms which leads to higher heat dissipation.

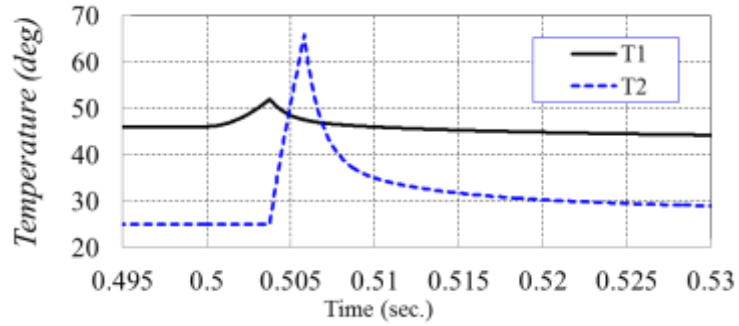

Figure 3.17 Junction temperature of the IGBT modules (T1 and T2) (Opening on self-protection order)

3.10.3 CLOSING ON GRID ORDER

The closing order is sent by grid at 0.8s by changing Kgrid to “1”. Figure 3.18 shows the switching signals of the closing sequence on receiving grid order which confirms correct operation as presented section 3.4 .

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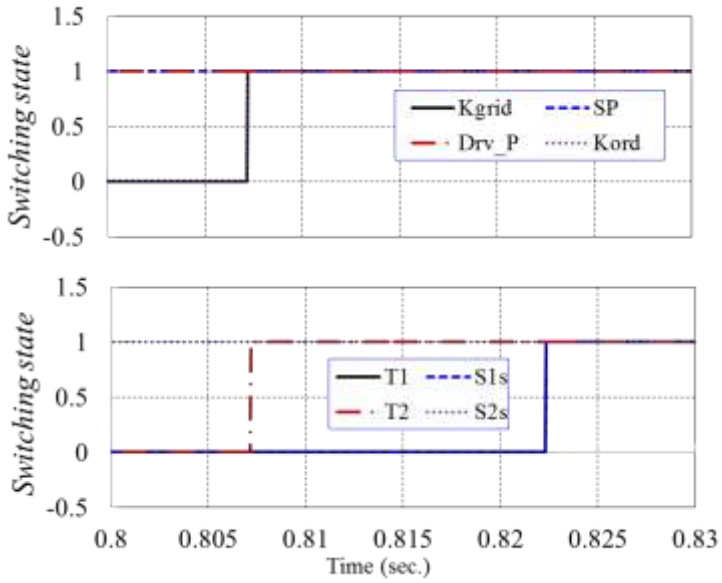

Figure 3.18 Switching signals (Closing on grid order)

Figure 3.19 shows the currents and voltages of the IGBT- based HYBRID DC CB of the closing sequence on receiving grid order.

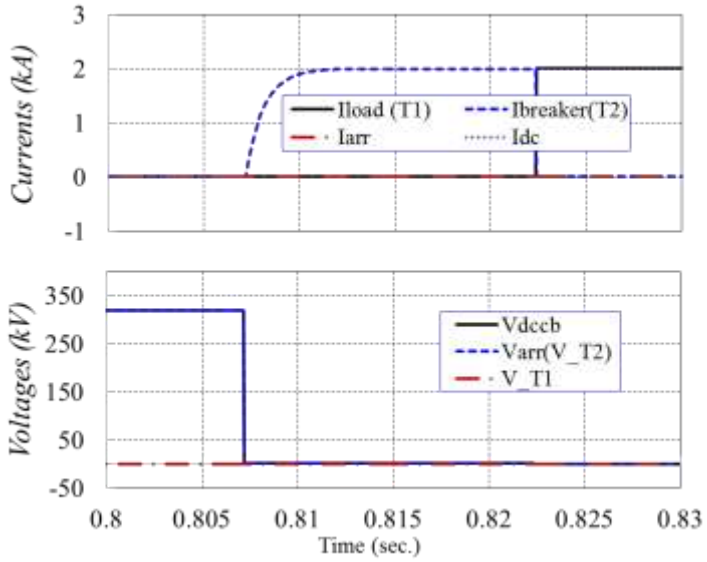

Figure 3.19 Currents and voltages (Closing on grid order)

3.10.4 RECLOSING IN FAULT

Figure 3.20 shows the switching signals when the DC CB is reclosing in fault. DC CB opens at 0.5s and grid sends the reclosing order at t=0.8s (T_{rec}=0.3s after opening). The fault is still present and the grid protection is made inactive (assumed that it cannot detect existing fault when DC voltage is zero). Therefore DC CB self-protection should trip on reclosing into a fault.

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It is seen that S_2 is kept closed at the end of opening, and T_2 turns on immediately on reclose command. After a T_{delay}, and when the current hits I_{pk_sp} (shown in Figure 3.22), self-protection is activated and trips the DC CB. It is also seen that T1 and S1 are kept open in this sequence. Figure 3.21 shows the DC CB operating mode. The logics “0”, “1” and “2” respectively mean the DC CB is closed, tripped by grid order and tripped by self-protection order.

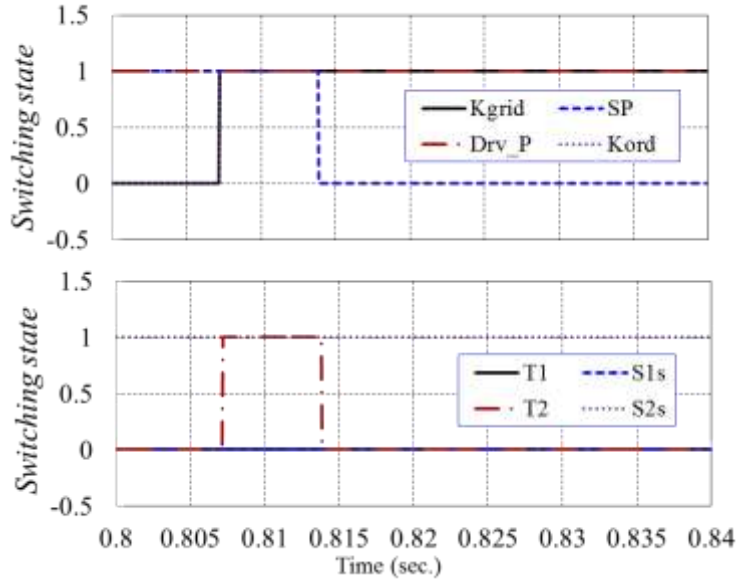

Figure 3.20 Switching signals (Reclosing in fault)

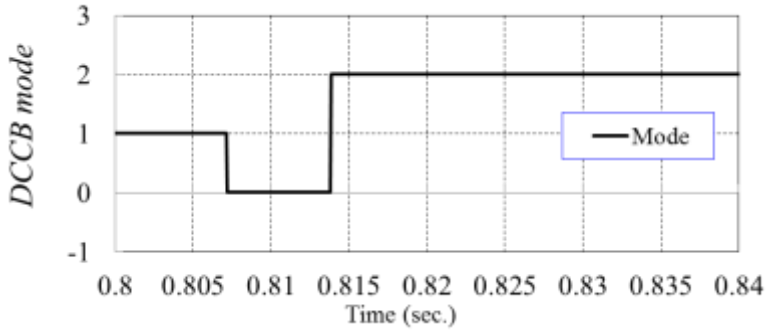

Figure 3.21 Operating mode (Reclosing in fault)

Figure 3.22 shows the currents and voltages of the IGBT- based hybrid DC CB when the breaker is reclosing in fault. It is seen that current reaches high value which is consistent with selected self-protection level (I_{pk_sp}=14.4 kA)

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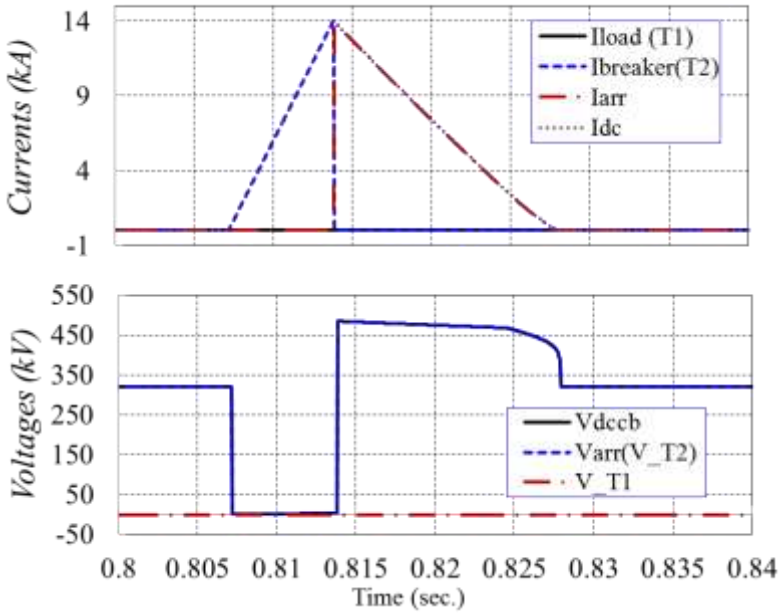

Figure 3.22 Currents and voltages (Reclosing in fault)

Figure 3.23 shows the junction temperature of each IGBT module of valve T1 and T2 for reclosing in fault. The temperature of T_2 reaches higher value as expected.

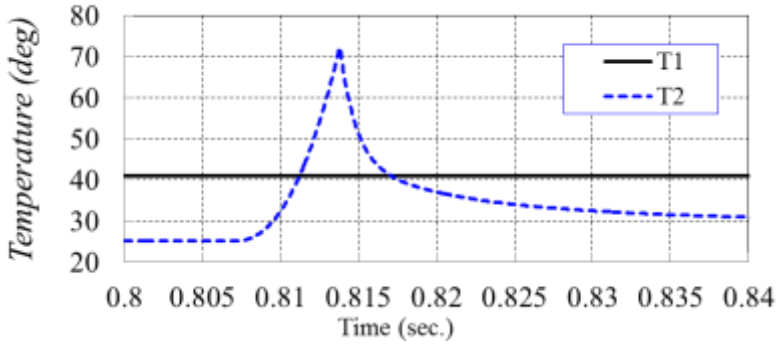

Figure 3.23 Junction temperature of the IGBT modules (T1 and T2) (Reclosing in fault)

3.10.5 SIMULATION WITH DIFFERENT PARAMETERS

The performance of the IGBT- based DC CB model is verified for a wide range of different parameters. After DC CB installation, Grid operator may want to change L_{dc} inductor to satisfy protection requirements. DC CB should operate well for a range of L_{dc}. Here two of the above tests (opening on self-protection and reclosing in fault (as two most severe test cases) with two extreme series inductor L_{dc} are given. The other parameters are same as in previous tests, and as given in Table 3.4.

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- **Opening on self-protection with L_{dc}=0.05 H**

The DC fault is applied at 0.5s and the grid protection is disabled. The L_{dc} is selected very small (L_{dc}=0.05 H) to investigate its impact on the breaker operation.

Figure 3.24 shows the switching signals of the opening sequence on receiving self-protection order with L_{dc}=0.05 H. It is seen that the SP signal becomes "0" first and then the Drv_P signal drops to zero. This means the DC CB tripping is triggered by self-protection but DC CB operation is not fast enough for the rate of current rise and current will reach the driver protection level. Driver level protection is activated which in practice may mean some component destruction.
It can be seen in Figure 2.1 that the DC CB operating mode changes from "2" (trip by self-protection) to "3" (trip by drive-protection)

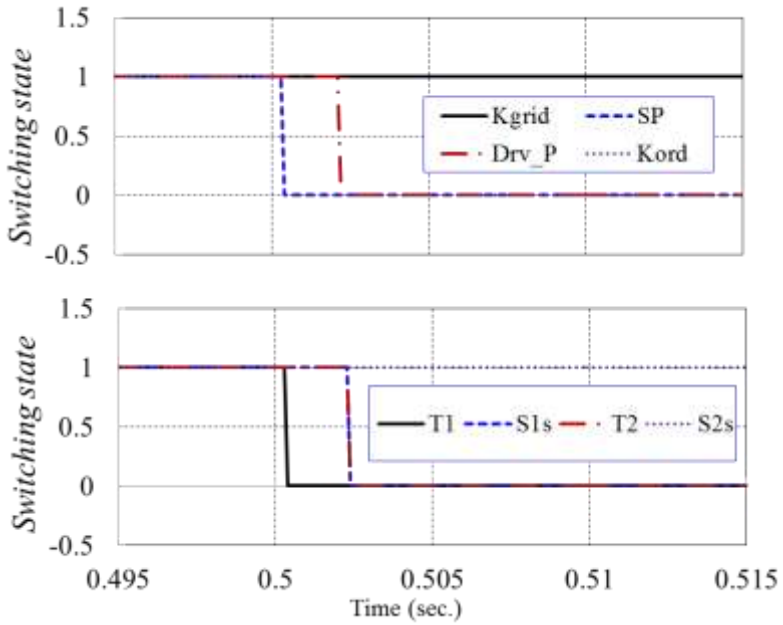

Figure 3.24 Switching signals (Opening on self-protection, L_{dc}=0.05 H)

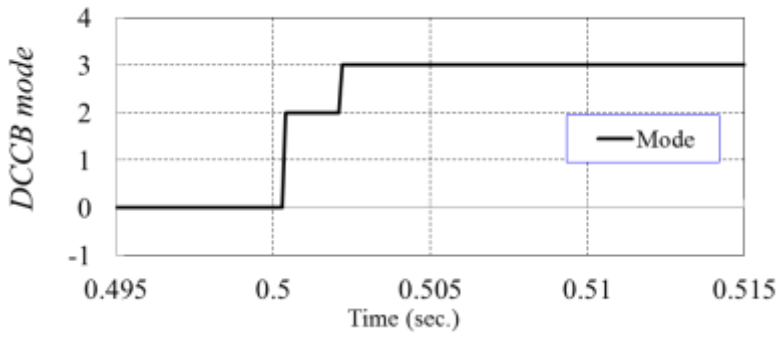

Figure 3.25 Operating mode (Opening on self-protection, L_{dc}=0.05 H)

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Figure 3.26 shows the currents and voltages of the same opening sequence. It is seen that the self-protection trips the DC CB when fault current exceeds I_{pk_sp}=4 kA which is the same fault current limit of the grid protection. In fact, the calculated I_{pk_sp} for this case is lower than 4 kA but a minimum lower limit of 4 kA is applied to prevent interference with normal operation.

It is also seen that the fault current exceeds I_{pk}=16 kA. This implies that the inductor L_{dc}=0.05 H is too small and a larger inductor should be selected. Simulation results show that the fault current remains below I_{pk}=16 kA and the driver protection is not activated if $L_{dc} \geq$ 55 mH is selected.

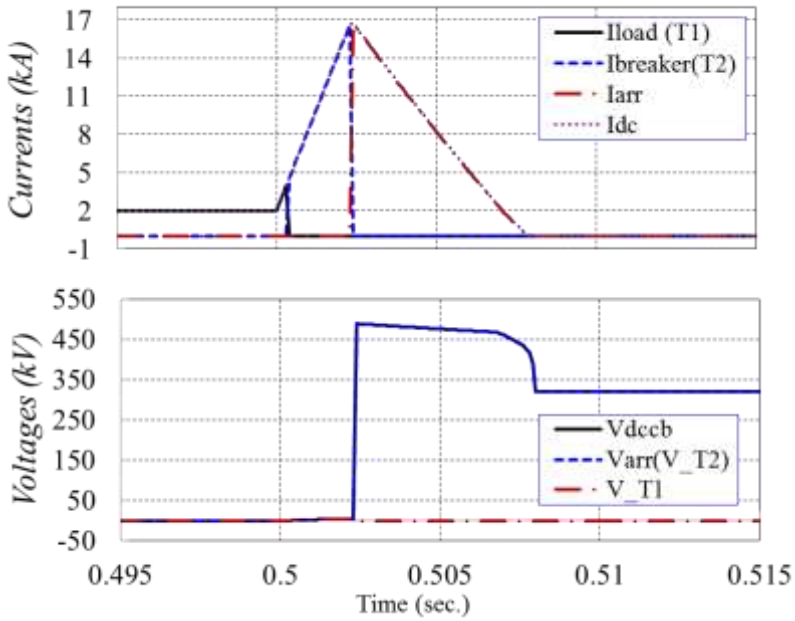

Figure 3.26 Currents and voltages (Opening on self-protection, L_{dc}=0.05 H)

Figure 3.27 shows the junction temperature of each IGBT module of valve T1 and T2 for the same test. It is worth noting that although the fault current is higher (compared to the same test with larger L_{dc}), the fault duration is shorter and therefore the rise of temperature T2 is almost the same (and even lower) of T2 in Figure 3.17.

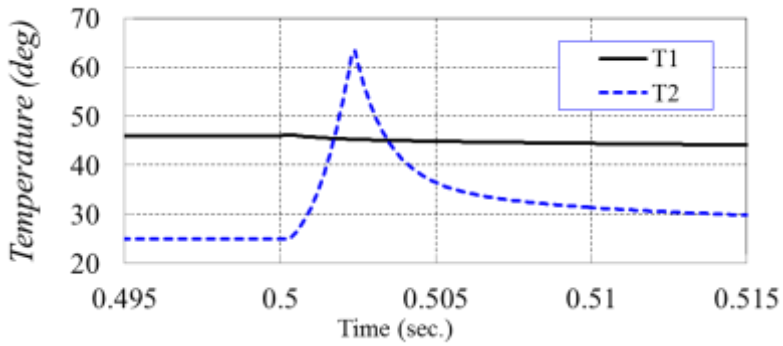

Figure 3.27 Junction temperature of the IGBT modules (T1 and T2) (Opening on self-protection, L_{dc}=0.05 H)

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- **Reclosing in fault with L_{dc}=0.8 H**

The reclosing in fault test case is repeated here with an extremely large inductor L_{dc}=0.8 H. Figure 3.28 shows the switching signals when the DC CB is reclosing in fault with L_{dc}=0.8 H. Figure 3.29 shows that the DC CB operating mode changes from "1" (tripped by grid order) to "0" (back to close-state) and then rises to "2" (trip by self-protection). It is seen that the signals show a similar behaviour of the signals in test case 3.10.2.

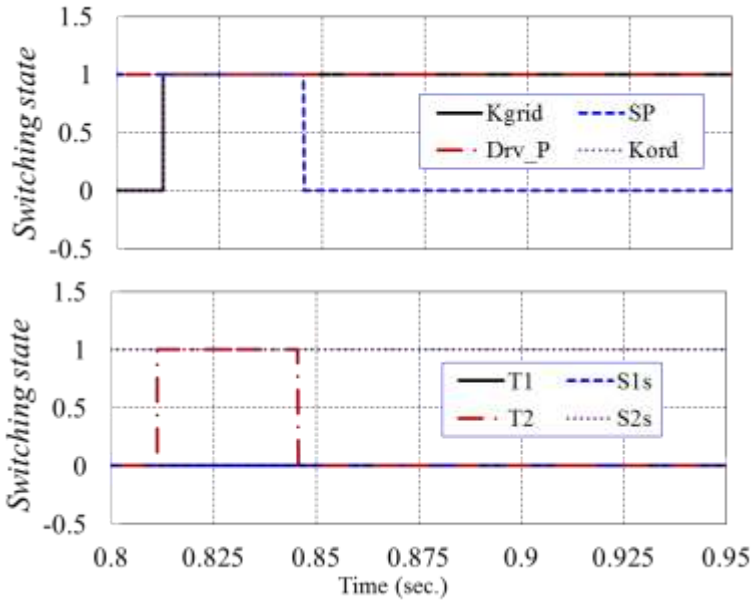

Figure 3.28 Switching signals (Reclosing in fault, L_{dc}=0.8 H)

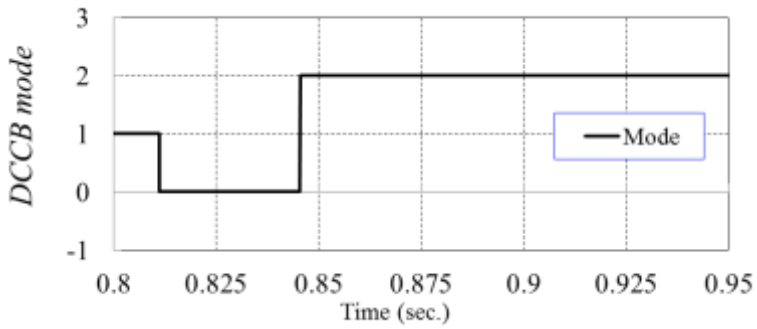

Figure 3.29 Operating mode (Reclosing in fault, L_{dc}=0.8 H)

Figure 3.30 shows the currents and voltages when the DC CB is reclosing in fault with L_{dc}=0.8 H. It is seen that the fault interruption time is much longer (around 35 ms) with this very large L_{dc}. It is seen that the fault current reaches maximum value which is somewhat below the self-protection level I_{trip_sp}=14.4 kA. This implies that the self-protection is activated by temperature limit as can be seen in the next figure.

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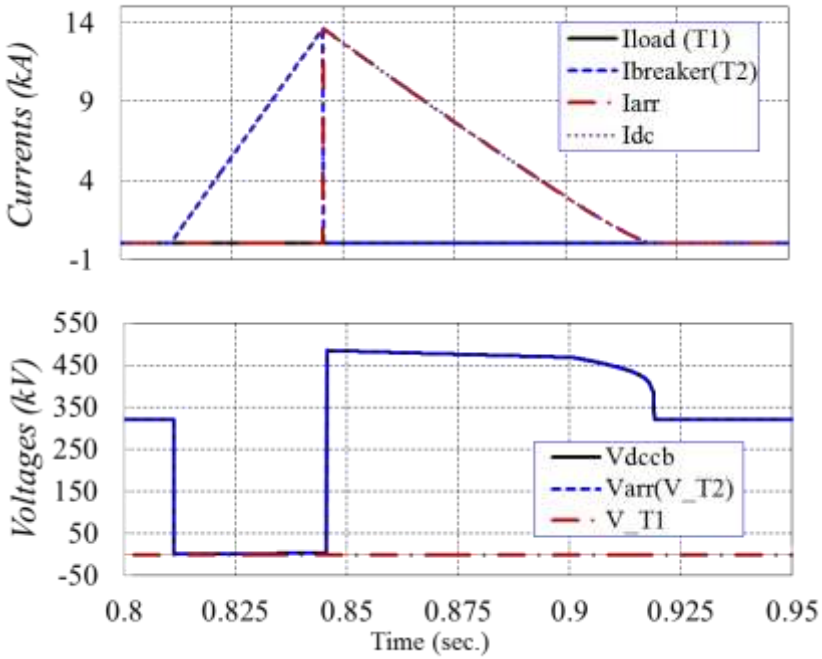

Figure 3.30 Currents and voltages (Reclosing in fault, L_{dc}=0.8 H)

Figure 3.31 shows the junction temperature of each IGBT module of valve T1 and T2 for reclosing in fault. It is seen that the temperature of T_2 hits the limit 120 ºC which in turn trips the DC CB on self-protection. This high temperature is the result of long fault interruption time. Further test shows that maximum inductance value of L_{dc}<0.6H should be used to prevent tripping on high temperature. As inductance is increased further, DC CB would trip on high temeparture while peak current will be lower than 16kA.

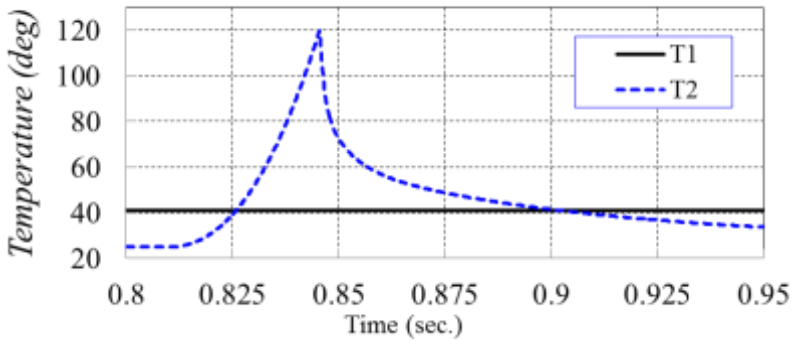

Figure 3.31 Junction temperature of the IGBT modules (T1 and T2) (Reclosing in fault, L_{dc}=0.8 H)

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4 MODELLING THYRISTOR-BASED HYBRID DC CB

4.1 STRUCTURE OF THYRISTOR-BASED HYBRID DC CB

Figure 4.1 shows the structure of thyristor-based HYBRID DC CB. It is composed of the following main components:

- An ultra-fast Disconnector (UFD) S_1
- A residual current breaker (RCB) S_2
- Load commutation switch (LCS) (IGBT valve T_1)
- Main breaker (MB) consisting of Thyristor valves Tr_1, Tr_{11}, Tr_{12} and Tr_2 and surge arrseters SA_{11}, SA_{12} and passive compoenents.
- Energy absorbing element (Main surge arrester as nonlinear resistor with specified I-V table)
- A series inductor L_{dc} to limit the rise of DC fault current

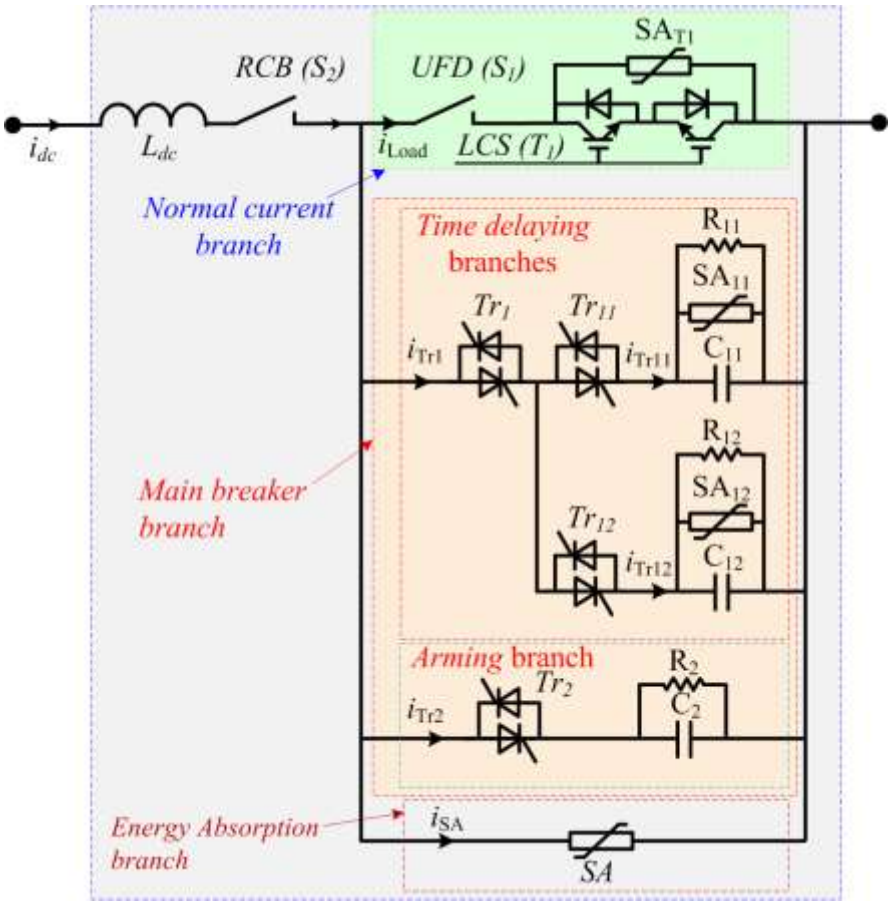

Figure 4.1 Structure of thyristor-based hybrid DC CB

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In normal operation, the UFD S_1 and valve T_1 are closed and all thyristors are off. Therefore the DC current flows through the normal current branch branch; i.e. i_{Load}= i_{dc}.

On receiving trip order, the valve T_1 is turned off and the first time-delaying branch thyristor valves (Tr_1, Tr_{11}) are triggered simultaneously. The fault current is transferred to the first time-delaying branch after the thyristors turn on delay. The surge arrester S_{T1} conducts during this time.The UFD S_1 is opened when its current drops below residual current I_{res}. Once the contacts of UFD S_1 have separated (but not fully opened yet), and the voltage across the capacitor C_{11} in the first time-delaying branch rises to V_{SA11_rated} (0.5*V_{SA11_clamp}) the thyristor valves of the second time-delaying branch (Tr_1, Tr_{12}) are triggered. When the UFD S_1 is fully opened, the arming branch thyristor valve (Tr_2) is triggered and the fault current commutates to this branch. The fault current will then be transferred to the main surge arrester SA and will be extinguished by the counter voltage of the arrester. The RCB S_2 will finally interrupt the arrester leakage current when it drops below I_{res}.

The closing sequence can take place when the capacitors of second time delaying and arming branches are discharged. The sequence is started by closing RCB S_2. When S_2 is fully closed, the valves Tr_1 and Tr_{11} are triggered. When the voltage across C_{11} rises to V_{SA11_rated}, a closing signal is sent to UFD S_1. When S_1 is fully closed, the valve T_1 will be closed.

The function, design requirement and operating limits of each branch are discussed in the following sections.

4.2 BRANCHES DESCRIPTION

4.2.1 NORMAL CURRENT BRANCH

The load branch conducts the DC current in both normal operation and early stage of DC fault. The branch is composed of an ultra-fast mechanical UFD S_1, an IGBT valve T_1 and a surge arrester SA_{T1}.

The UFD S_1 can be opened or closed if its current is less than its rated residual chopping current I_{res}. The mechanical time delay of the switch to reach its full dielectric withstand capability is assumed to be T_{mec}≈2 ms. Note that the UFD S_1 can be opened or closed if its current, i_{load}, is less than I_{res}.

The IGBT valve T_1 conducts the DC current in both normal operation and early stage of DC fault. Therefore the current rating of T_1 should be at least 1.5-2 p.u. There is no specific voltage rating requirement for valve T_1 but typically a configuration 3x3 IGBTs are used to increase voltage and current rating and also to reduce the ON state loss.

The surge arrester SA_{T1} has default PSCAD I-V characteristics shown in Table 3.1. The voltage rating of SA_{T1} must be lower than half of the voltage rating of valve T_1. Note that the voltage across the surge arrester may rise up to 2 p.u. depending on the I-V characteristics and the maximum fault current.

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4.2.2 FIRST TIME DELAYING BRANCH OF MAIN BREAKER BRANCH

The first time-delaying branch conducts the fault current for very short time; i.e. from the time the valve T_1 is opened until the contacts of UFD S_1 have separated (but not necessarily reached their full dielectric withstand capability). The main function of this branch is to start building up the transient interruption voltage (TIV) and to keep the voltage of the surge arrester SA_{T1} (across T_1) below its rated voltage. Without this branch, the voltage across SA_{T1} may exceed its clamping voltage and then its current (and the current in UFD S_1) may increase and prevent the UFD S_1 to be opened. Note that the contacts of UFD S_1 have not separated yet and the SA_{T1} (and T_1) will experience the voltage of C_{11}.

The first branch is turned on by triggering simultaneously the thyristor valves Tr_1 and Tr_{11}, which happens at same time as the valve T_1 is turned off. Thyristors Tr_1 and Tr_{11} will be turned off by triggering the second time-delaying branch.

The main components in this branch are the thyristor valves Tr_1 and Tr_{11}, the capacitor C_{11}, the surge arrester SA_{11} and the resistor R_{11}. The thyristor valves Tr_1 and Tr_{11} should conduct the fault current in the range of 2 p.u. – 5 p.u. depending on the magnitude of the L_{dc} and fault resistance. Although the fault current is high, the conduction time is very short. However, it should be noted that the transient fault current is well within the range of peak non-repetitive surge current (I_{TSM}) of the selected thyrsitors. The voltage rating of Tr_1 and Tr_{11} is determined by the grid DC voltage level.

The maximum size of capacitor bank C_{11} influences the fault interuption time. Larger capacitor increases the capcitor charging time and therefore the interuption time. The minimum size of the capacitance is determined by the maximum rate of voltage rise. It should be ensured that the voltage across the contacts of UFD S_1 is always kept below its dielectric breakdown strength. If the contacts of S_1 separate when the first time-delaying branch is conducting, the UFD S_1 will experience the same voltage V_{C11}. Therefore, the rate dV_{C11}/dt should be lower than the rate of voltage dielectric breakdown strength of S_1, considering the speed of moving contacts.

The resistor R_{11} is required to discharge C_{11} in preparation for the next operating cycle. It is selected as the largest resistance that fully discharge the capacitor before the next reclosing order.

The surge arrester SA_{11} has the same I-V characteristics of Table 3.1 with a voltage rating lower than the rating of valve T_1.

4.2.3 SECOND TIME DELAYING BRANCH OF MAIN BREAKER BRANCH

The second time-delaying branch conducts the fault current from the time when the contacts of the UFD S_1 have separated till the switch is fully opened (reached to its full open course). This branch builds up further the TIV.

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The second branch has the same structure and components as the first branch but with different rating for some of them. The thyristor valves Tr_1 and Tr_{12} are triggered when the contacts of UFD S_1 have separated (but not necessarily reached their full dielectric withstand capability).

The thyristor valve Tr_{11} is turned off by trigerring the thyristor valve Tr_{12}. Considering the extinction time (t_q) for the thyristors, the second branch must keep the thyristor valve Tr_{11} under reverse recovery process for at least t_q. This means that voltage across C_{12} must be lower than voltage across C_{11} for t_q duration. This requirement determines the size of capacitor C_{12}.

The second criterion for sizing the capacitor bank C_{12} is that the voltage across it (and therefore the voltage across S_1) builds up slower than the rate of voltage dielectric breakdown strength of S_1 (as explained earlier).

The surge arrester SA_{12} has the same I-V characteristics of Table 4.1 but with higher voltage rating to allow charging up the capacitor C_{12} to a higher voltage level. The voltage rating of SA_{12} should be lower than the voltage rating of the main surge arrester SA.

The resistor R_{12} is required to discharge C_{12} in preparation for the next operating cycle.

4.2.4 ARMING BRANCH OF MAIN BREAKER BRANCH

The arming branch conducts the fault current when the UFD S_1 is fully opened. The branch consists of thyristor valve Tr_2, capacitor C_2 and resistor R_2. The function of this branch is to build up TIV and transfer the fault current to the main surge arrester SA when the capacitor C_2 charges up to the main SA clamping voltage. The fault current will then be interrupted because of the counter voltage of the main SA in energy absorption branch.

The arming branch is turned on when the UFD S_1 is fully opened. As mentioned earlier, the size of capacitor C_2 determines the time that the second branch is kept under reverse recovery which must be longer than t_q to turn off the valve Tr_{12} completely.

The resistor R_2 is required to discharge the C_2 in preparation for the next operating cycle.

4.2.5 ENERGY ABSORPTION BRANCH

The I-V characteristics of the surge arrester SA is the same of Table 3.1. Its voltage rating is selected to have its clamping voltage around 1.5 times of the nominal DC line voltage.

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4.3 COMPONENT CHARACTERISATION

The test hybrid DC CB will be adopted in accordance with [15][16], leading to rated voltage and current of respectively 120 kV and 1.5 kA. The peak interrupting curent is 10 kA.

4.3.1 NORMAL LOAD BRANCH COMPONENTS (UFD S_1 AND IGBT VALVE T_1)

The current rating of the IGBT valve T_1 should be higher than nominal current (assumed 1.5 kA in the test system). Since the early stage of the fault current passes through this valve for a short time, its junction temperature should be monitored continuously and trip order should be issued if the temperature rises over 120 ºC. There is no specific voltage rating requirement for valve T_1. However, it should be high enough to give more flexibility to the surge arrester SA_{11} in first time-delaying branch.

One suitable IGBT module for valve T_1 could be the IGBT- based StackPak IGBT module 5SNA 2000K450300 (4500V and 2000A). Two IGBT modules should be used in series and opposite direction for bidirectional DC CB. The low ON resistance of this module (less than 1mΩ) generates low conduction loss in normal operation. Usually a matrix configuration 3x3 IGBTs is used in T_1 to reduce the ON resistance (and hence the power loss) and to increase both current and voltage ratings. The voltage rating of T_1 would be therefore 13.5 kV. Each IGBT module has internal driver-level protection which indiscriminately trips IGBT if current is close to destruction level.

The surge arrester SA_{T1} is required to keep the voltage across T_1 well below its rated value. The clamping voltage of SA_{T1} should be less than the voltage rating of valve T_1. Considering that the clamping voltage of SA is around two times of its rated voltage, V_{SAT1_rated}=6 kV (or V_{SAT1_clamp}=12 kV) is selected.

The UFD S_1 is modelled as an ideal swicth with time delay of T_{mec}≈2 ms and with chopping current (maximum interrpting current) of I_{res}=0.01 kA.

4.3.2 FIRST TIME-DELAYING BRANCH (THYRISTOR VALVE TR_1 AND TR_{11}, CAPACITOR C11, SURGE ARRESTER SA11 AND RESISTOR R11)

The voltage across this and all other branches rises up to the voltage of the main surge arrester (which is 1.5*Vdc) when they are not conducting. If the IGBT- based thyristor module 5STP 48Y7200 (7200V and 4800A) is adopted with voltage safety factor over 1.5, the valve voltage rating is 270 kV, and there should be 38 series thyristor modules in the branch. Assuming equal voltage stress across the two valves Tr_1 and Tr_{11}, each valve should be composed of 19 series thyristor modules.

The voltage rating of the surge arrester SA_{11} should be lower than the voltage rating of the surge arrester SA_{T1}, to prevent positive current through S_1 during opening. It should keep the current in S_1 below I_{res} even when the voltage across SA_{11} goes above its clamping voltage and the fault current is too high. Considering the the I-V

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curve of the surge arrester (given in Table 3.1), the rated voltage of SA_{11} should be less than 80% of the rated voltage of SA_{11} to keep the load branch current below I_{res}. Considering the voltages across the thyrsitor valves in the first branch and an appropreate margin, the voltage rating of SA_{11} is selected V_{SA11_rated}=3.5 kV (or V_{SA11_clamp}=7 kV).

Although the first branch start conducting when the contacts of the UFD S_1 are still not separated, it might keep conducting soon after the contacts have begun separation. Therefore, the minimum size for the capacitor C_{11} can be obtained considering the voltage dielectric breakdown strength of UFD S_1.

If the UFD S_1 opens fully in 2 ms and considering a 50% overvoltage, the voltage slope would be (1.5*120 kV)/2 ms. It is concluded that the contacts achieve minimal dielectric distance for 180 kV at 2 ms, although the exact contact separation distance is not known. Therefore the allowed voltage derivative dv_{C11}/dt must be lower than 90 V/μs. The voltage slope across C_{11} can be obtained using the equivalent circuit of the first time delaying branch shown in Figure 4.2. Note that the fault and thyristor resistances and also the surge arrester and resistor across the capacitor are neglected. The simple model of the circuit is:

$$i_{dc}(t) = I_{dc0}\cos(\omega_o t) + \frac{V_{dc} - V_{C110}}{z_o}\sin(\omega_o t) \tag{3.1}$$

$$v_{C11}(t) = V_{dc} - (V_{dc} - V_{C110})\cos(\omega_o t) + z_o I_{dc0}\sin(\omega_o t) \tag{3.2}$$

where $\omega_o = 2\pi f_o = 1/\sqrt{L_{dc}C_{11}}$, $z_o = \sqrt{L_{dc}/C_{11}}$, V_{C110} is the initial value of v_{C11}, and I_{dc0} is the initial value of I_{dc}.

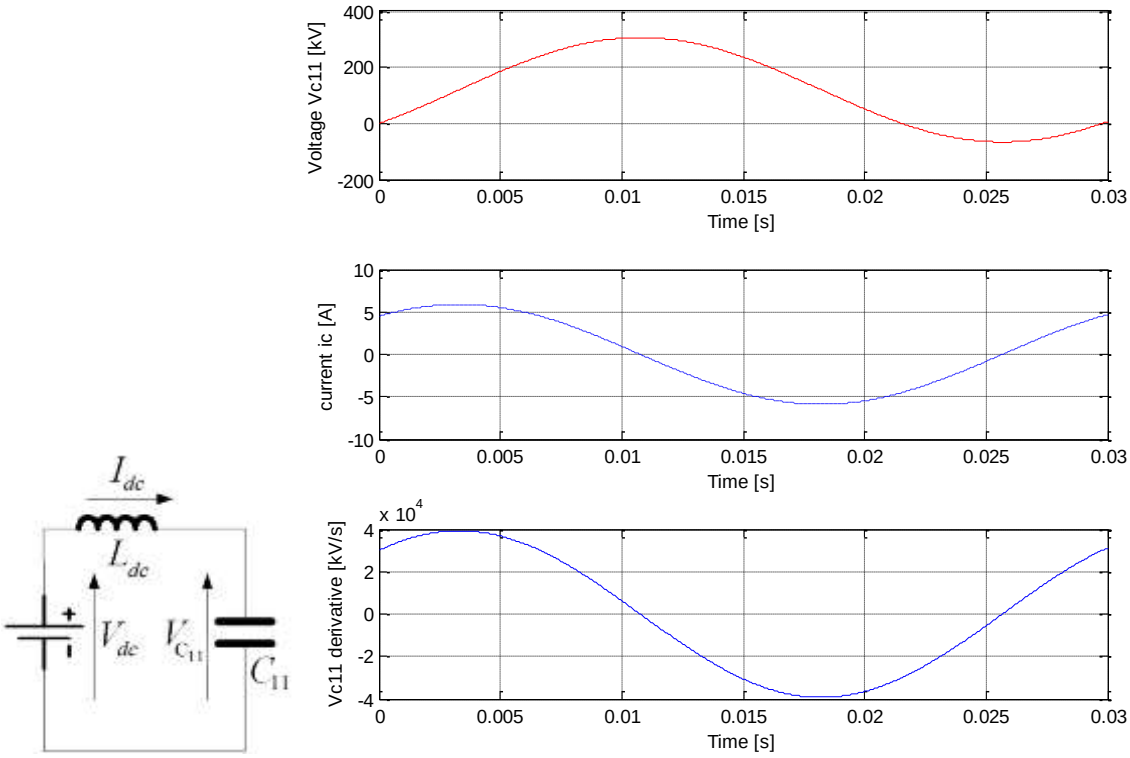

Figure 4.2 Equivalent circuit and unconstrained time response of the first time delaying branch (L_{dc}=0.15 H, C11=150 μF).

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The first derivative of the voltage v_{C11} in (3.2) is given by

$$\frac{dv_{C11}}{dt} = \omega_o (V_{dc} - V_{C11}) \sin(\omega_o t) + \omega_o z_o I_{dc0} \cos(\omega_o t) \tag{3.3}$$

Considering also that there is a resitir R11 accross C11, that reducces intial share of capacitor current, the voltage slope can be assumed to be the largest at the instant t=0:

$$\begin{aligned} &\frac{dv_{C11}}{dt}(t=0) = \omega_o z_o I_{dc0} \\ &\frac{dv_{C11}}{dt}(t=0) = \frac{I_{dc0}}{C} \\ &\frac{I_{dc0}}{C} < 90 \times 10^6 V/s \end{aligned} \tag{3.4}$$

Therefore the size of capacitor is

$$C_{11} > \frac{I_{dc0}}{90 \times 10^6 V/s} \tag{3.5}$$

Assuming that the breaker triping is based on grid order when the current exceeds 2 p.u., the initial value for fault current would be 3 kA. Therefore, C_{11}>33 µF.

Note that the initial fault current can be larger, if as an example the DC CB is tripped on self-protection. Considering (1.1) in section 2.6, the maximum initial fault current with self-protection happens with extremely large series inductor L_{dc}. The initial fault current with L_{dc}=0.8 H and estimated fault interruption time T_{int}=8 ms, is calculated to be around 9 kA. Therefore, the size of C_{11} should be 3 times lager; i.e. C_{11}>99 µF

Considering all possible operating conditions and an adequate margin, a capacitance of 150 µF is selected for C_{11}. The voltage rating of capacitor C_{11} should be larger than the maximum possible voltage over the surge arrester SA_{11} which is almost 2*V_{SA11_rated} (or V_{SA11_clamp}). Therefore, V_{C11_rated}=1.5*V_{SA11_clamp}=15 kV. Figure 4.2 shows unrestricted time domain response, which in practice will be clipped at 15 kV because of SA11.

The resistance R_{11} is selected to discharge C_{11} in required time, which is based on the fastest reclosing time. If the fastest reclosing happens no sooner than 300 ms [35], R_{11} should be selected to discharge the C_{11} in shorter time (for example in around 200 ms).

$$4R_{11}C_{11} \le 0.2s \Rightarrow R_{11} \le \frac{1}{20C_{11}} = \frac{1}{20*150\mu F} = 330\Omega \tag{3.6}$$

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Note that at peak voltage V_{c11}=12 kV, the power dissipation in R_{11} is 436 kW. This power dissipation happens for very short time.

The conduction time of this branch is calculated approximately by solving (3.1) and (3.2) simultaneously. Assuming the DC CB (with V_{dcN}=120 kV and L_{dc}=0.15 H) is tripped on self-protection with initial fault current $I_{dc}(0)$≈4.5 kA and the fault current commutates to the second time-delaying branch when V_{c11}≥0.75*V_{SA11_clamp}=7.5 kV, the conduction time is obtained equal to t_{11}≈0.2 ms and the fault current reaches to around $I_{dc}(t_{11})$≈4.7 kA. The time domain response of first branch is shown in Figure 4.3

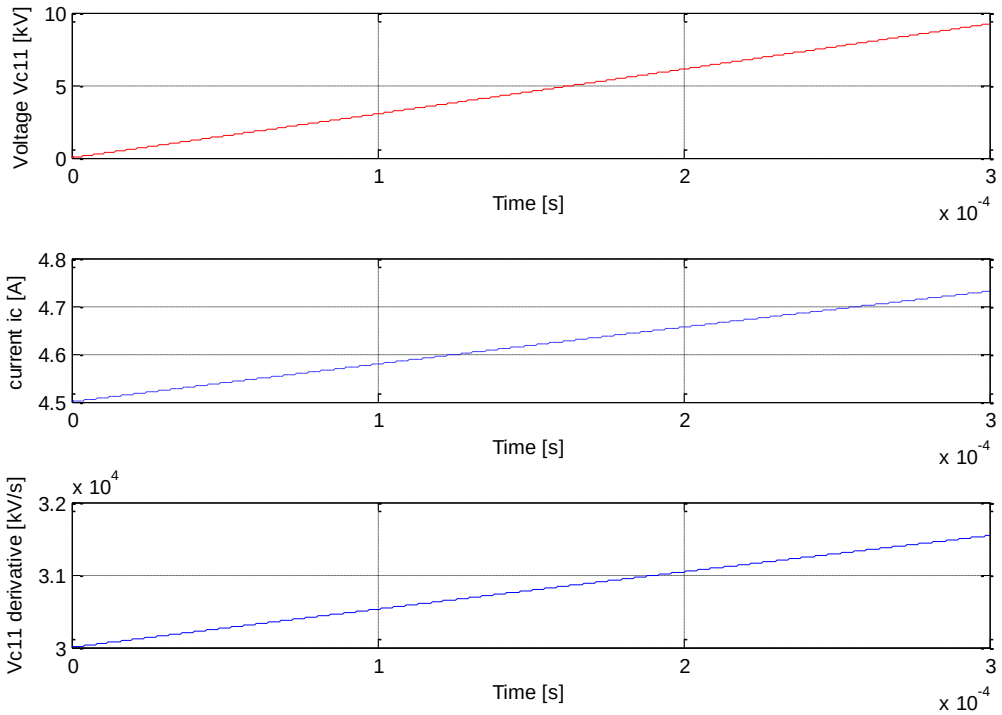

Figure 4.3 Time response of the first time delaying branch in the first 0.3 ms (L_{dc}=0.15 H, C11=150 μF).

4.3.3 SECOND TIME-DELAYING BRANCH (THYRISTOR VALVE TR_{12}, CAPACITOR C12, SURGE ARRESTER SA12 AND RESISTOR R12)

The thyristor valve Tr_{12} is similarly composed of 19 series thyristor modules.

The voltage rating of the surge arrester SA_{12} is selected between the voltage rating of the first branch and the main surge arresters, in this case equal to V_{SA12_rated}=30 kV (or V_{SA12_clamp}=60 kV).

The second time-delaying branch brings the thyristor valve Tr_{11} in the first time-delaying branch under reverse recovery process as long as v_{c12}<v_{c11}. The recovery process should last for the duration of the thyrsitor

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extinction time (for the selected thyristors t_q=700 µs). The voltage equation for the second time-delaying branch in in anlogie to (3.2):

$$v_{C12}(t) = V_{dc} - V_{dc}\cos(\omega_o t) + z_o I_{dc}(t_{11})\sin(\omega_o t) \tag{3.7}$$

Figure 4.4 shows that the capacitor C_{12}=500 µF is adequate to keep voltage v_{C12} below v_{C11}=V_{SA11_clamp}=7 kV for t_q=700µs (V_{dc}=120 kV, v_{C12}(t=700us)=7 kV, I_{dc0}=I_{dc}(t_{11})=4.7 kA, L_{dc}=0.15 H). Assuming adequate margin, a capacitance of 750µF is selected for C_{12}.

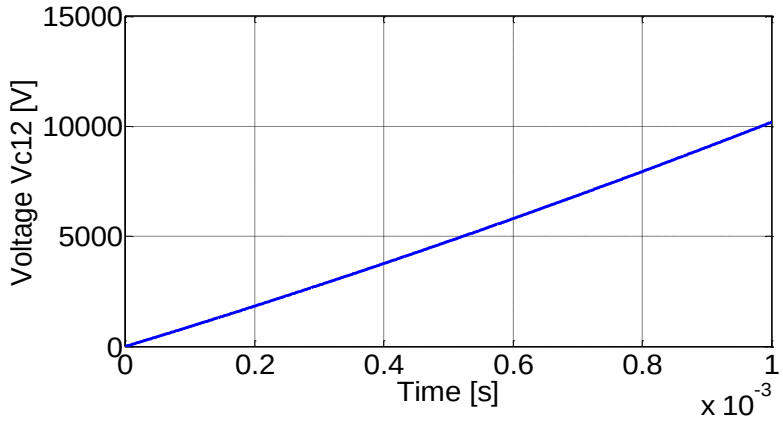

Figure 4.4 voltage v_{C12} vs time, assuming C_{12}=500uF.

Figure 4.5 shows that the voltage derivative is around 12 V/µs for selected components. Note that it is considered that number of series thyristors is (12000*1.5*1.5/7200)=38 and the voltage stress is divided by this number. This is well below 20 V/µs which is the test voltage for selected phase control thyristors (5STP48Y7200). Therefore a smaller reverse recovery time may also be considered.

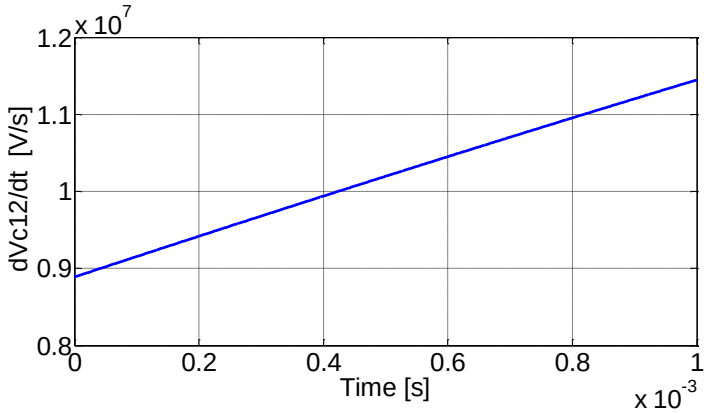

Figure 4.5 voltage dv_{C12}/dt vs time

The resistance R_{12} is calculated similarly as follows

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$$4R_{12}C_{12} \le 0.2s \Rightarrow R_{12} \le \frac{1}{20C_{12}} = \frac{1}{20*750\mu F} = 66\Omega \quad (3.8)$$

The conduction time of the second time-delaying branch is estimated similarly by solving (3.1) and (3.2). Assuming the DC CB (with V_{dcN}=120 kV and L_{dc}=0.15 H) is tripped on self-protection with initial fault current $I_{dc}(0)$≈4.7 kA and that the fault current commutates to the arming branch when v_{c12}≥0.75*V_{SA12_clamp}=45 kV, the conduction time is obtained equal to t_{12}≈5 ms and the fault current reaches to around $I_{dc}(t_{12})$≈8.2 kA.

Note that the overall conduction of the above two branches (first and second time-delaying branches) should be equal or larger than T_{mec}; i.e. t_{12}≥T_{mec}-t_{11}.

4.3.4 ARMING BRANCH (THYRISTOR VALVE TR_2, CAPACITOR C_2 AND RESISTOR R_2) AND MAIN SURGE ARRESTER

The thyristor valve Tr_2 is similarly composed of 38 series thyristor modules. The voltage rating of the main surge arrester SA is selected equal to 120 kV*1.5/2=90 kV (or equivalently V_{SA_clamp}=180 kV).

The arming branch brings the thyristor valves in the second time-delaying branch under reverse recovery process as long as v_{c2}<v_{c12}, which should be sustaned for the thyristor extinction time (t_q=700 μs). The volatge for the arming branch is similar as equation (3.2):

$$v_{C2}(t) = V_{dc} - V_{dc}\cos(\omega_o t) + z_o I_{dc}(t_{12})\sin(\omega_o t) \quad (3.9)$$

Figure 4.6 shows that the capacitor C_2=150 μF is adequate to keep voltage v_{C2} below v_{C12}=0.75*V_{SA12_clamp}=45 kV for t_q=700 μs (V_{dc}=120 kV, v_{C2}(t=700 us)=45 kV, I_{dc0}= $I_{dc}(t_{12})$=8.2 kA, L_{dc}=0.15 H). Assuming adequate margin, a capacitance of 220μF is selected for C_2.

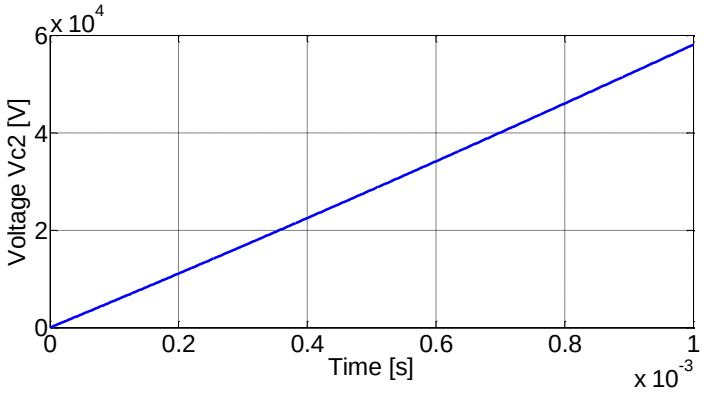

Figure 4.6 voltage v_{C2} vs time with C_2=150μF

Figure 4.7 shows that voltage derivative is around 5.5 V/us for selected components. Note that it is considered that number of series thyristors is (12000*1.5*1.5/7200)=38 and the voltage stress is divided by this number.

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This is well below 20 V/us which is test voltage for selected phase control thyristors (5STP48Y7200). Therefore a smaller reverse recovery time may be considered.

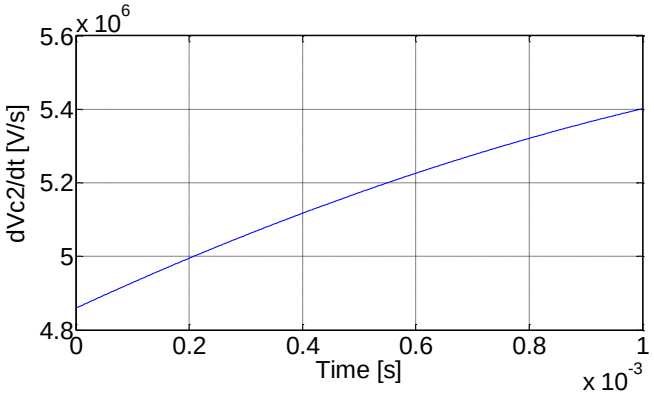

Figure 4.7 voltage dv_{C12}/dt vs time

The discharge resitance R_2 is calculated as follows

$$4R_2C_2 \le 0.2s \Rightarrow R_2 \le \frac{1}{20C_2} = \frac{1}{20*220\mu F} = 230\Omega \qquad (3.10)$$

The conduction time of the arming branch is estimated similarly by solving (3.1) and (3.2). Assuming the fault current commutates to the main surge arrester when $v_{c2} \ge V_{SA2\_clamp}$=180 kV, the conduction time (with V_{dcN}=120 kV and L_{dc}=0.15 H) is obtained equal to $t_2 \approx 0.5$ ms and the fault current would be $I_{dc}(t_2) \approx 7$ kA.

4.3.5 RESIDUAL CURRENT BREAKER S_2

The RCB S_2 is a slow mechanical switch with time delay assumed as T_{res}=30 ms and the same residual chopping current $I_{res.}$=0.01 kA.

4.3.6 SERIES INDUCTOR L_{DC}

The series inductor L_{dc} is used to limit the rate of rise of fault current. Considering the worst case scenario, R_f=0 and ignoring the valves ON resistance, and also assuming that the fault current is allowed to reach 10 kA from the nominal current 1.5 kA during the total fault interruption time (T_{int}>2.5 ms), the value for L_{dc} is

$$V_{dc} = L_{dc}\frac{di_f}{dt} \Rightarrow L_{dc} = \frac{V_{dc}}{\left(\Delta i_f/\Delta t\right)} > \frac{V_{dc}}{\left(\left(i_{fpk} - i_{dcN}\right)/T_{\text{int}}\right)} = \frac{120kV}{8.5kA/5ms} = 71mH \qquad (3.11)$$

This is the minimum L_{dc}. However, L_{dc} is usually selected larger than this minimum value, for example L_{dc}=150 mH.

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4.3.7 THERMAL MODEL FOR VALVES

The thermal model of the IGBT valves T_1 is the same of the IGBT- based hybrid DC CB model described in section 3.2.7. The thermal model of the thyristor valves T_{r1}, T_{r11}, T_{r12} and T_{r2} are also similar to the thermal model of the IGBT valves T_2 (see Figure 3.5) but with the transient thermal impedances Z_{thJC} from thyristor module 5STP 48Y7200 datasheets [36]. Figure 3.4 shows the transient thermal impedances Z_{thJC} for this thyristor [36]. The air temperature is assumed 25 ºC and the coefficient K_1 (in Figure 3.5) is equal to 1.

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i(1-e^{-t/\tau_i})$$

i	1	2	3	4
R_i(K/kW)	2.005	0.602	0.251	0.141
τ_i(s)	0.939	0.146	0.024	0.006

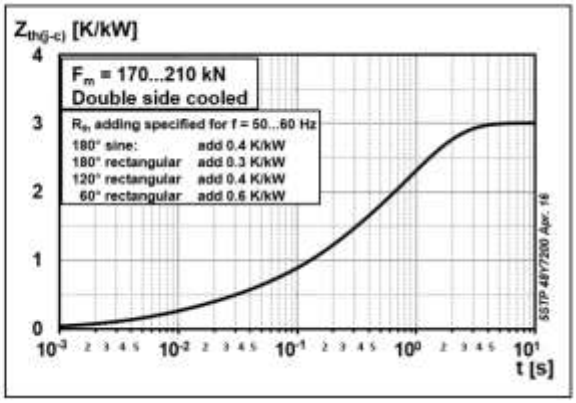

Figure 4.8 Transient thermal impedance Z_{thJC} vs time for thyristor 5STP 48Y7200 [36]

4.4 DESIGN SUMMARY

The design of the thyristor-based hybrid DC CB is summarized as follows:

1) Select the IGBT module for valve T_1 based on the required voltage and current. This valve is usually configured in matrix form to increase the rated current and voltage and also to reduce conduction loss. Usually a 3x3 matrix comination is used for valve T_1.
2) Select the voltage clamping of surge arrester SA_{T1}. It should be lower than the rated voltage of valve T_1.
3) Select the voltage clamping of surge arrester SA_{11}, SA_{12} and main SA; $V_{SA11\_clamp} < V_{SAT1\_clamp}$, $V_{SA11\_clamp} < V_{SA12\_clamp} < V_{SA\_clamp}$ and $V_{SA\_clamp} = 0.75V_{dc}$.
4) Select the number of thyristor modules for each thyristor valve based on the DC line voltage level, main surge arrester voltage rating and appropreate voltage margin.
5) Select the size of capacitor C_{11} based on the maximum allowed voltage slope to keep the voltage across UFD S_1 (when the first branch is conducting) below its voltage dielectric breakdown strength.
6) Select the size of capacitor C_{12} to keep the first branch thyristors under reverse recovery process for at least t_q. The second criterion for sizing the capacitor bank C_{12} is that the voltage across it builds up slower than the rate of voltage dielectric breakdown strength of S_1.
7) Select the size of capacitor C_2 to keep the second branch thyristors under reverse recovery process for at least t_q..

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8) The capacitors voltage rating are: $V_{C11\_rated}=1.5*V_{SA11\_clamp}$, $V_{C12\_rated}=1.5*V_{SA12\_clamp}$, and $V_{C2\_rated}=2*V_{dc}$.
9) The resistors R_{11}, R_{12} and R_2 are required to discharge the corresponding capacitors in 0.2s (less than 0.3s as the time interval for the fastest reclosing).

Table 4.1 and Table 4.2 summarize the main parameters and the design parameters of thyristor-based hybrid DC CB.

Table 4.1 Main parameters of thyristor-based hybrid DCCB (with phase-control thyristor)

Parameters	Value
Voltage rating	120 kV
Current rating	1.5 kA
Peak interrupting current	10 kA
IGBT module	ABB 5SNA 2000K450300 (4500V, 2000A)
Thyristor module	ABB 5STP 48Y7200 (7200V, 4840A, t_q=700μs)

Table 4.2 Design parameters of thyristor-based hybrid DCCB (with phase-control thyristor) of Table 4.1

Load branch	IGBT valve T_1	Voltage rating of SA_{T1} (Clamping voltage)	Ultra-fast disconnector S_1	Residual current breaker S_2
	3x3 IGBT modules	6 kV (12 kV)	T_{mec}=2 ms, I_{res}=0.01 kA	T_{res}=30 ms, I_{res}=0.01 kA
Thyristor branches	Number of thyristor modules in branch (with voltage factor 2.25)	Capacitor C_{11}	Voltage rating of SA_{11} (Clamping voltage)	Resistor R_{11}
First time delaying branch	38 series thyristor modules (19 series thyristor modules for each valve Tr_1 and Tr_{11})	150 μF (15 kV)	3.5 kV (7 kV)	330Ω
Second time delaying branch	19 series thyristor modules in valve Tr_{12}	750 μF (90 kV)	30 kV (60 kV)	55Ω
Arming branch and main surge arrester	38 series thyristor modules in valve Tr_2	220 μF (240 kV)	90 kV (180 kV)	260Ω
Series inductor L_{dc}				
	150mH			

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The values of the capacitors might seem too high and unrealistic. This is because of large extinction time of the phase control thyristors. In the next section, the design will be repeated with fast thyrsitors and it can be seen that the values of the capacitors are significantly smaller.

4.5 DESIGN WITH FAST THYRISTORS

The above design is done with phase control thristors. Althought phase control thyristors are commonly used in HVDC applications, it might not be a good candidate for this application. The main problem with the phase control thyristor is their long extinction time which increases the size of capacitors. These large capacitors increase the fault intruption time significantly. This can be seen later in the simulation results.

In this section the thyristor-based DC CB is designed using fast thyristor 5STF 28H2060 [37]. This thyristor provides suitable rated current (I_{TAV}=2667A) and transient peak current (I_{TSM}=46.5 kA) with very short extinction time (t_q=60µs). The primary dissadvantage is its lower rated voltage (V_{DRM}=2000V) which increases the number of series thyristors in the thyristor valves. The higher ON state loss is not significant issue in DC CB applications.

The design steps are same as explained in Section 4.3 and not repeated here. Table 4.3 Shows the design parameters with the fast thyristors of DC CB from Table 4.1.

It is seen that only the number of thyristor modules in the thyristor valves, the size of capacitors and corresponding resistors are changed compared to the results in Table 4.2. The capacitor size is significantly smaller, and it will be shown in simulation section that the opening time is shorter.
The design with fast thyristors is selected as the final design.

Table 4.3 Design parameters of thyristor-based hybrid DC CB with fast thyristor

Load branch	IGBT valve T_1	Voltage rating of SA_{T1}	UFD S_1		RCB S_2
	3x3 IGBT modules	6 kV	T_{mec}=2 ms, I_{res}=0.01 kA		T_{res}=30 ms, I_{res}=0.01 kA
Thyristor branches	Number of thyristor modules in branch (with voltage factor 2)	Capacitor C_{11}	Voltage rating of SA_{11} (Clamping voltage)		Resistor R_{11}
First time delaying branch	136 series thyristor modules (68 series thyristor modules for each valve Tr_1 and Tr_{11})	250 µF (15 kV)	5 kV (10 kV)		190Ω
Second time delaying branch	68 series thyristor modules in valve Tr_{12}	90 µF (90 kV)	30 kV (60 kV)		540Ω
Arming branch and main surge arrester	136 series thyristor modules in valve Tr_2	16 µF (240 kV)	90 kV (180 kV)		3100Ω
Series inductor L_{dc}					
	150mH				

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4.6 OPENING SEQUENCE

The opening sequence starts when the DC CB is in normal operation (valve T_1 and UFD S_1 are closed and all capacitors are discharged) and a trip order is received. The opening sequence is comprised of 6 main steps as summarized in Table 4.4.

Table 4.4 Opening sequence of thyristor-based hybrid DC CB

	Inputs measurement	Action	Comment
1	(Is trip order received?) & (all capacitors are discharged ?)	Open T_1	The fault current commutates to SA_{T1}. The voltage across T_1 rises very fast to the voltage rating of SA_{T1}.
2	Is v_{T1}>$V_{LimitT1}$?	Trigger Tr_1 & Tr_{11}:	The fault current commutates to the first time delaying branch. The voltage across the capacitor C_{11} rises to the voltage rating of SA_{11}.
3	(Is T_1 opened?) & (i_{load}<I_{res}?)	Open S_1	A mechanical delay T_{mec} is applied in model as it takes T_{mec} seconds to be fully opened.
4	Is v_{C11}>$V_{LimitC11}$?	Trigger Tr_1 & Tr_{12}:	Trigger the second time delaying branch. The thyristor Tr_{11} will be under reverse recovery, (because v_{C12}< v_{C11}) and the fault current commutates to the second branch. The voltage across the capacitor C_{12} rises to the voltage rating of SA_{12}.
5	(Is S_1 fully opened?) & (Is v_{C12}>$V_{LimitC12}$?)	Trigger Tr2	The fault current commutates to the arming branch and shortly after it will be transferred to the main surge arrester SA and will be finally extinguished.
6	(i_{dc}<I_{res}?)	Open S_2	A mechanical delay T_{res} is applied in model as it takes T_{res} second to be fully opened.

Figure 4.9 shows the flowchart of the opening sequence for thyristor-based hybrid DC CB.

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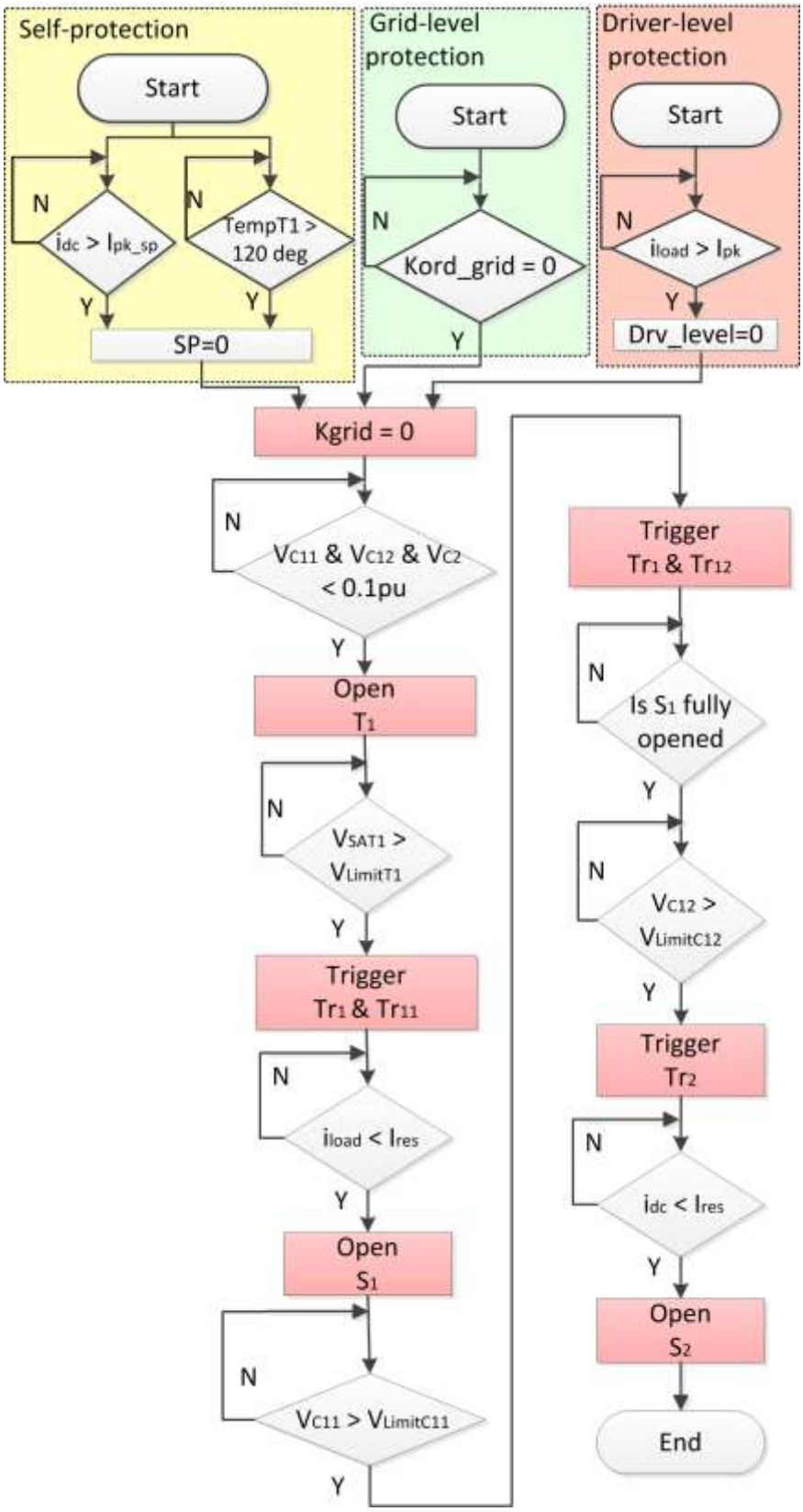

Figure 4.9 Opening sequence flowchart of thyristor-based hybrid DC CB

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4.7 CLOSING SEQUENCE

The closing sequence starts when the DC CB is in fully open state (all switches and valves are open and the capacitors in the second time-delaying and arming branches are discharged) and a closing order from grid-level is received. The closing sequence is summarized in Table 4.5.

Table 4.5 Closing/reclosing sequence of thyristor-based hybrid DC CB

	Inputs measurement	Action	Comment
1	Is closing order (Kord_grid) received? & (i_{dc}<I_{res}?) & (The capacitors C_{12} and C_2 are discharged ?) & (The junction temperature of T_1 is less than T_{limit}?)	Close S_2	A mechanical delay T_{res} is applied in model as S_2 takes T_{res} to be fully opened. The condition (T_{T1} < T_{limit}?) prevents closing if the junction temperature of the valves are still high.
2	Is S_2 fully closed?	Trigger Tr_1 & Tr_{11}:	The first time delaying branch conducts the current and the voltage across the capacitor C_{11} rises.
3	(Is v_{C11} > $V_{LimitC11}$? & No fault is occured)	Close S_1	The check “No fault is occured“ prevents closing S_1 and T_1 if DC CB is reclosing in fault. This speeds up the opening sequence by avoiding mechanical time delay of S_1. A mechanical delay T_{mec} is applied in model as it takes T_{mec} second to be fully opened.
4	(Is S_1 fully closed?)	Close T_1	The current commutates to the load branch.

Figure 4.10 shows the flowchart of the closing sequence for thyristor-based hybrid DC CB. The sequence is triggered if grid order is received and there is neither self-protection nor driver-level protection trip. If the DC CB had been opened on self-protection (SP=0) or driver-level protection (Drv_level=0), the closing will be blocked.

The time delay T_{delay} (which is calculated based on L_{dc}, V_{dcN} and the fault current level) is applied to check whether the closing is under fault or not. If it is under fault, a separate opening sequence is triggered (when the fault current hits the limit) and the fault signal becomes “1” again. This prevents closing S_1 and T_1.

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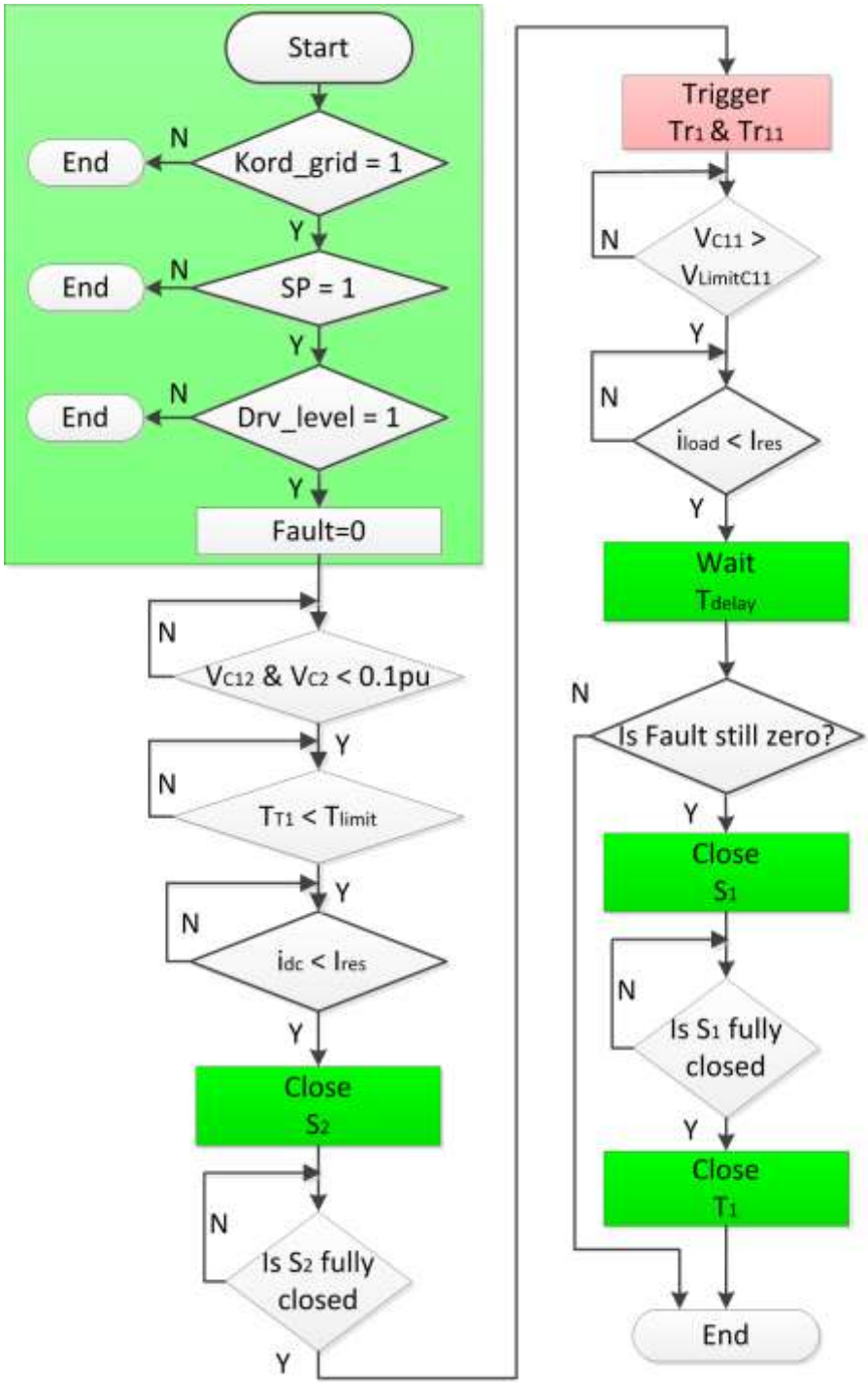

Figure 4.10 Closing/reclosing sequence flowchart of thyristor-based hybrid DC CB

4.8 RECLOSING SEQUENCE

The reclosing sequence happens only if reclosing is enabled. In this case the opening sequence will not open S2. On closing there is no need for closing S_2, which speeds up closing operation.

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4.9 MODEL USER INTERFACE

Table 4.6 summarizes the thyristor-based hybrid DC CB parameters. User is able to change each of these parameters using a user interface panel.

Table 4.6 thyristor-based hybrid DCCB parameters

Variable	DC CB With Phase-control thyristor	DC CB With Fast thyristor
V_{dcN} (Line DC voltage level)	120 kV	120 kV
I_{dcN} (Normal DC current)	1.5 kA	1.5 kA
Number of series IGBT in T_1	3	3
Number of parallel IGBT in T_1	3	3
Thyristor valves ON resistance (Tr_1, Tr_{11}, Tr_{12} and Tr_2)	0.0013 Ω (19 series thyristor)	0.0071 Ω (69 series thyristor)
Thyristor valves OFF resistance (Tr_1, Tr_{11}, Tr_{12} and Tr_2)	19e9 Ω (19 series thyristor)	69e9 Ω (69 series thyristor)
Thyristor valves forward voltage drop (Tr_1, Tr_{11}, Tr_{12} and Tr_2)	0.016 kV (19 series thyristor)	0.083 kV (69 series thyristor)
Thyristor minimum extinction time	700 µs	60 µs
First branch capacitance and resistance	150 µF & 330 Ω	250 µF & 190 Ω
Second branch capacitance and resistance	750 µF & 55 Ω	90 µF & 540 Ω
Arming branch capacitance and resistance	220 µF & 260 Ω	16 µF & 3100 Ω
I_{pk} (Trip level for T1 driver protection)	16 kA	16 kA
I_{pk_sp} (DC CB self protection trip level)	8.5 kA	8.5 kA
I_{res} (residual current for S_1 and S_2)	0.01 kA	0.01 kA
T_{mec} (S_1 mechanical delay)	2 ms	2 ms
T_{res} (S_2 mechanical delay)	30 ms	30 ms
L_{dc} (DC line series inductor)	0.15 H	0.15 H
Voltage rating of surge arrester SA_{T1} (Clamping voltage)	6 kV (12 kV)	6 kV (12 kV)
Voltage rating of surge arrester SA_{11} (Clamping voltage)	3.5 kV (7 kV)	3.5 kV (7 kV)
Voltage rating of surge arrester SA_{12} (Clamping voltage)	30 kV (60 kV)	30 kV (60 kV)
Voltage rating of main surge arrester SA (Clamping voltage)	90 kV (180 kV)	90 kV (180 kV)

4.10 SIMULATION VERIFICATION

Figure 4.11 shows the simple test system for thyristor-based hybrid DC CB. Table 4.6 gives the breaker parameters.

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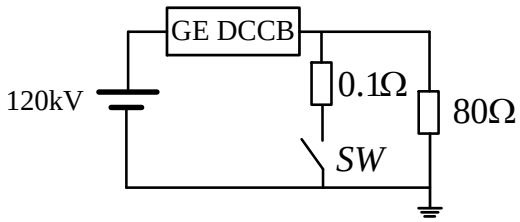

Figure 4.11 thyristor-based hybrid DC CB test system

The performance of the thyristor-based hybrid DC CB model is verified for the following test cases:

- Opening on grid order
- Opening on self-protection order
- Closing on grid order
- Simulation with different parameters
- Simulation with fast thyristors

It can be seen that the thyristor-based hybrid DC CB model is not verified for reclosing in fault. There is uncertainty about reclosing time and further delay for opening after closing. The phase control thyristors are use initially, while design with fast thyristors is tested is last section.

4.10.1 OPENING ON GRID ORDER

Figure 4.12 shows the switching signals of the opening sequence on receiving grid order for a fault at 0.5s. K_{grid} is the grid level signal. It is “1” in normal operation (DC CB closed) and becomes zero “0” if trip order is sent. The signals SP and Drv_P have the same logic but detect the fault from self-protection and driver-level protection. The switching signals T1, S1s and S2s represent the corresponding valve/switches status. The logic “1” represents closed status and logic “0” is for open status. Figure 4.13 shows a zoom view of the switching signals.

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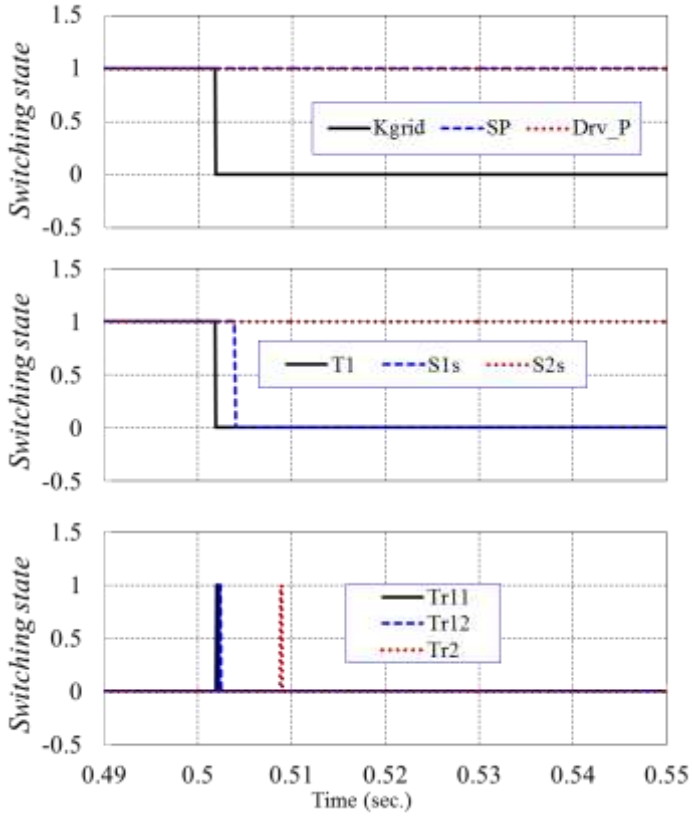

Figure 4.12 Switching signals (Opening on grid order)

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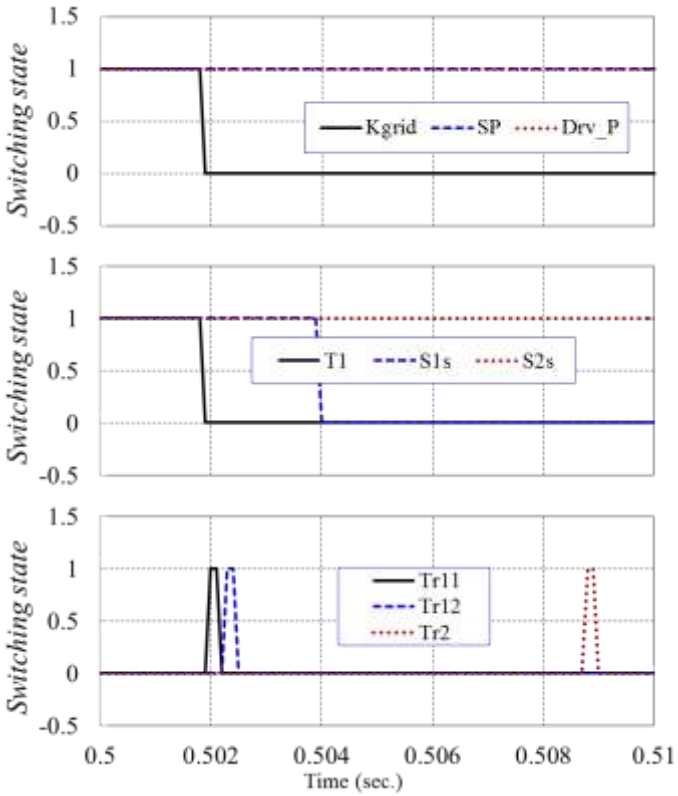

Figure 4.13 Switching signals (Zoom view)

Figure 4.14 shows the currents of the thyristor-based hybrid DC CB for the same fault. When the current reaches 3 kA (2 p.u.), a grid protection issues trip order. The fault current commutates to the first time-delaying branch after tripping valve T1 and triggering thyristor valve Tr11 (and Tr1). The fault current is soon transferred to the second time-delaying branch by triggering valve Tr12 (and Tr1).

The fault current then commutates to the arming branch by triggering valve Tr2 and will be extinguished after transferring to the main surge arrester.

Figure 4.15 shows the current of the surge arresters for the same fault. It is seen that the currents are zero or very small. This implies that the energy loss of the surge arrester is negligible in opening on grid order. The reason that the current of SA_{T1} is zero but the currents of the two other SAs are around 0.008kA is the different threshold voltages that the next branch is triggered. Note that the first time-delaying branch is turned on when the voltage across SA_{T1} rises to $0.5*V_{SAT1\_clamp}$ (or V_{SAT1_rated}), but the second time-delaying and arming branches are turned on when the voltage across C_{11} and C_{12} rises respectively to $0.75*V_{SA11\_clamp}$ and $0.75*V_{SA12\_clamp}$.

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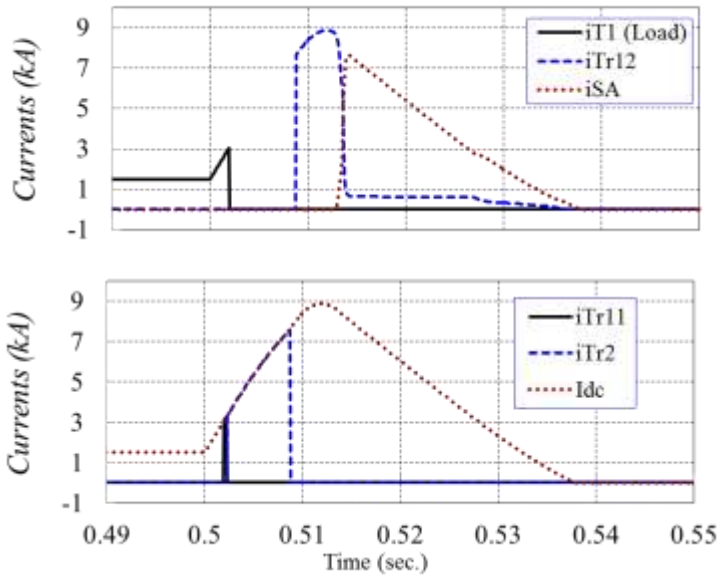

Figure 4.14 Branches currents (Opening on grid order)

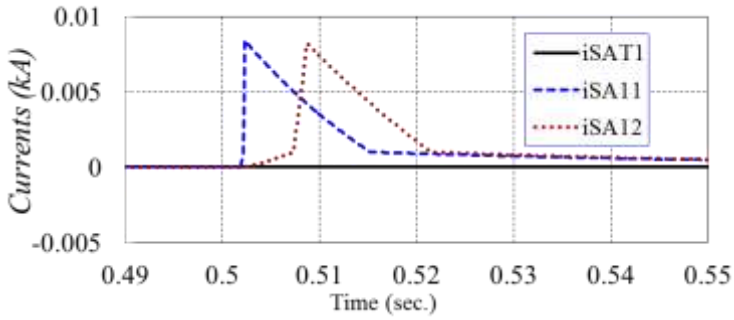

Figure 4.15 Surge arresters current (Opening on grid order)

Figure 4.16 shows the voltages of the thyristor-based hybrid DC CB for the same fault. It is seen that the capacitors voltages (v_{C11} and v_{C12}) rise up to the clamping voltage of the corresponding surge arrester and then discharge into their resistor as the current commutates to the next branch. The capacitor voltage v_{C2} and the breaker voltage v_{DCCB} rise up to V_{SAmain_clamp}. The breaker voltage v_{DCCB} drops to V_{dcN} (120 kV) when the DC CB current becomes zero.

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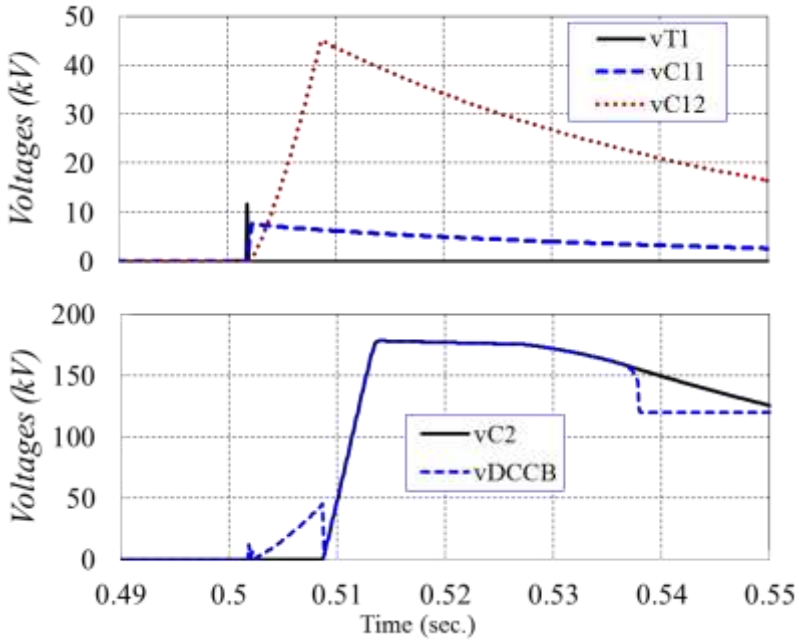

Figure 4.16 Capacitors and DC CB Voltages (Opening on grid order)

Figure 4.17 shows the junction temperature of each IGBT module of valve T1, and each thyristor of valves Tr1 and Tr2. Note that the thyristors of valves Tr11 and Tr12 are not shown as they generate less power loss resulting in lower junction temperature. The junction temperatures are calculated in PSCAD (or EMTP) based on the equations given in sections 3.2.7 and 4.3.7. It is seen that the temperatures are well below the limit of 120 ºC.

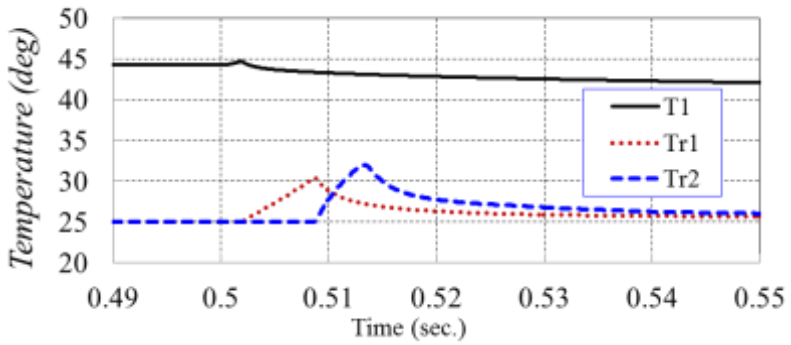

Figure 4.17 Junction temperature of the IGBT modules (T1) and thyristor modules (Tr1 and Tr2) (Opening on grid order)

4.10.2 OPENING ON SELF PROTECTION

The DC fault is applied at 0.5s and the grid protection is disabled to test the self-protection function of the DC CB. Self-protection sends trip signal when fault current exceeds the threshold limit.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

Figure 4.18 shows the switching signals of the opening sequence on receiving self-protection. Figure 4.19 shows a zoom view of the switching signals. It is seen that the signal Kgrid remains “1” and signal SP becomes “0” implying that the DC CB is tripped on self-protection.

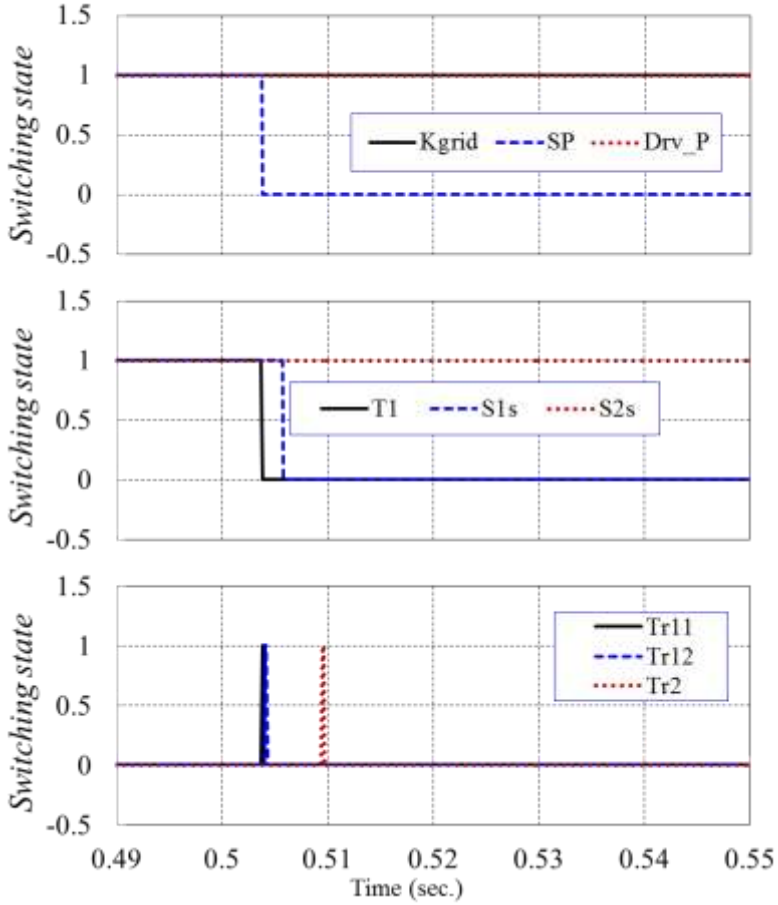

Figure 4.18 Switching signals (Opening on self-protection order)

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

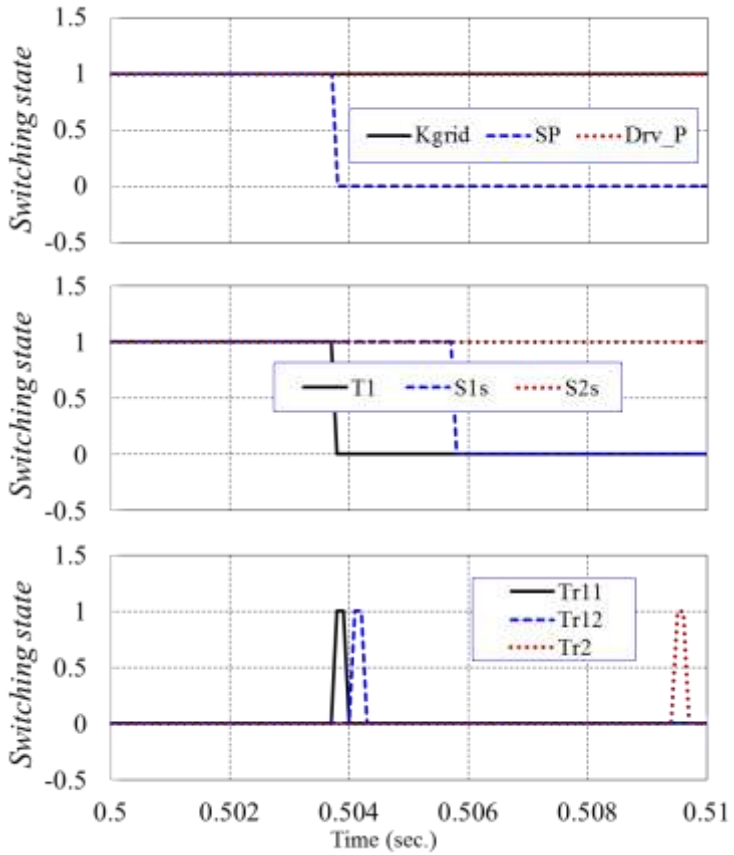

Figure 4.19 Switching signals (Opening on self-protection order, zoom view)

Figure 4.20 shows the currents of the thyristor-based hybrid DC CB in the opening sequence on self-protection. It is seen that the current commutates from the load branch to the commutation branch when it exceeds 4.5 kA. This is trip level for self-protection which is calculated internally based on the nominal DC voltage, L_{dc}, T_{mec} and the maximum current limit I_{trip_sp} (defined by user) as explained in section 2.6. This current limit is higher than typical grid protection trip current (assumed 3 kA) for the given parameters. However it may interfere with grid-protection in some instances (as an example with slow grid protection) and therefore self-protection should be properly modelled.

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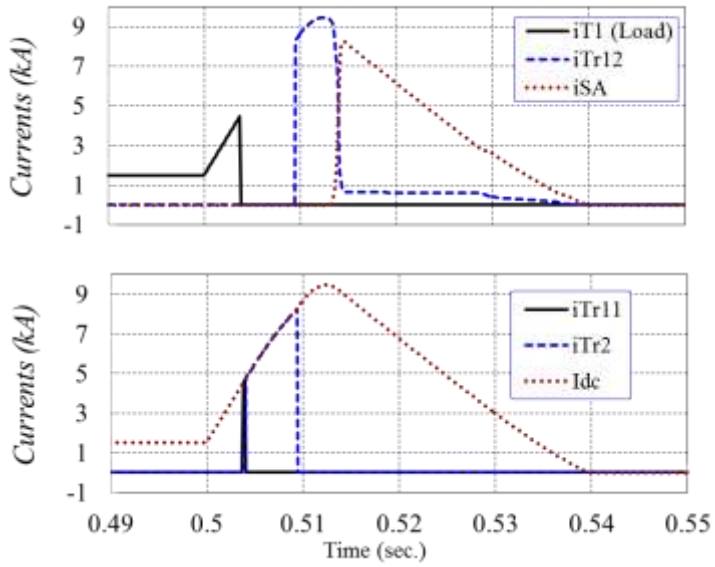

Figure 4.20 Branches currents (Opening on self-protection order)

Figure 4.21 shows the voltages of the thyristor-based hybrid DC CB of the opening sequence on receiving self-protection.

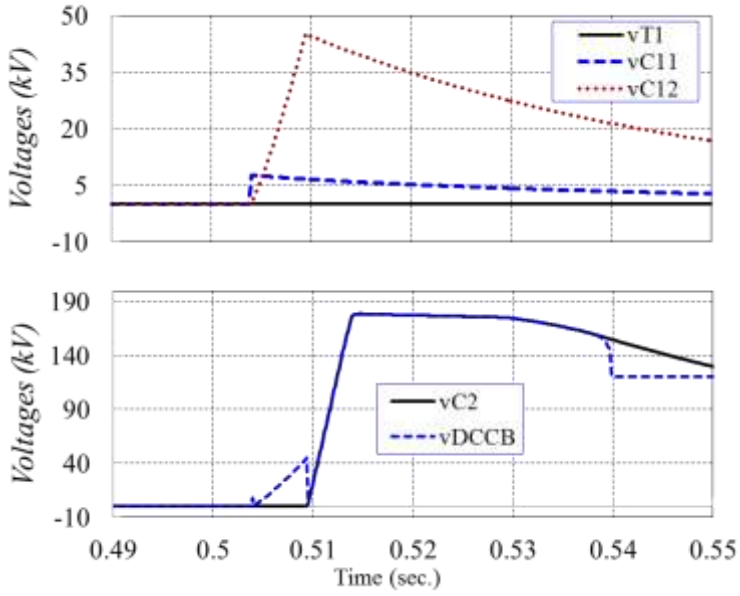

Figure 4.21 Capacitors and DC CB Voltages (Opening on self-protection order)

Figure 4.22 shows the junction temperature of each IGBT module of valve T1, and each thyristor of valves Tr1 and Tr2 in the opening sequence on self-protection.

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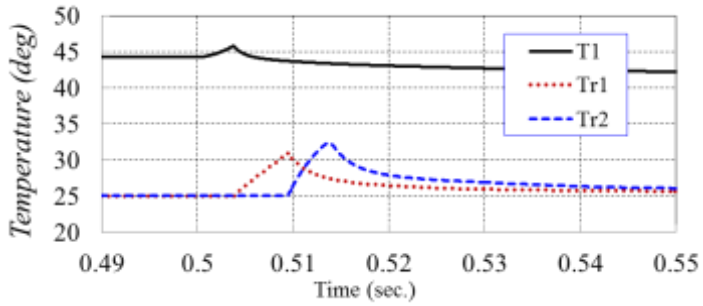

Figure 4.22 Junction temperature of the IGBT modules (T1) and thyristor modules (Tr1 and Tr2) (Opening on self-protection order)

4.10.3 CLOSING ON GRID ORDER

Figure 4.23 shows the switching signals of the closing sequence under normal operation. On receiving grid closing order (Kgrid=1), the RCB S2 is first closed and after T_{res}, the Tr11 is triggered. When the voltage v_{C11} reaches to the V_{SA11_rated}, the UFD S1 is closed first and (after T_{mec}=2 ms) the valve T1 is closed.

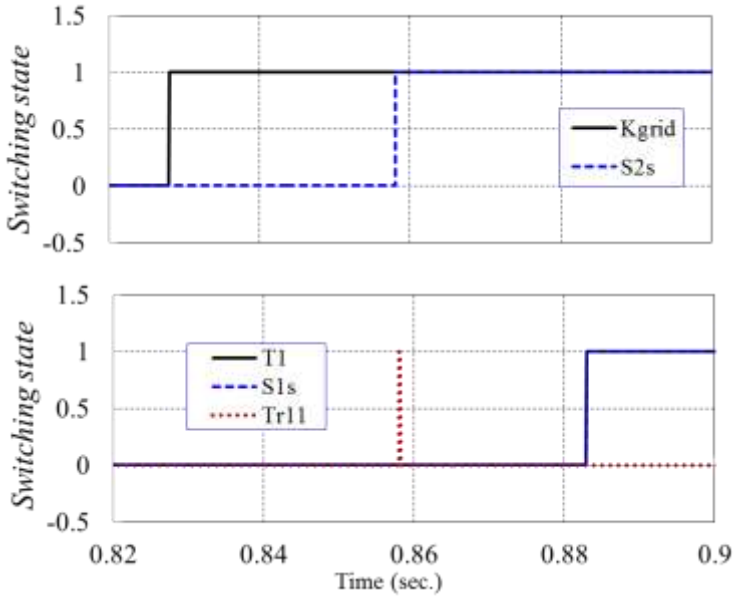

Figure 4.23 Switching signals (Closing on grid order)

Figure 4.24 shows the currents of the thyristor-based hybrid DC CB in the closing sequence under normal condition. It is seen that the current flows first through the first time-delaying branch and then commutates to the load branch.

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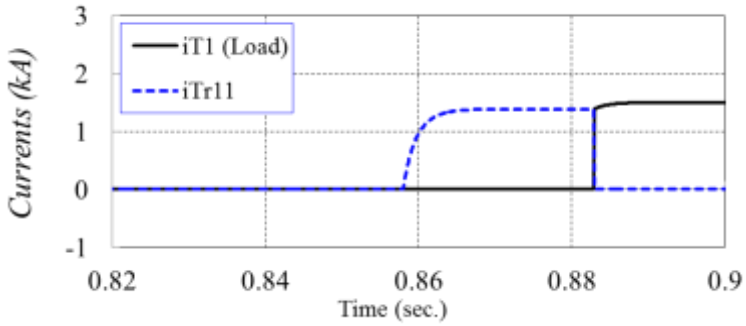

Figure 4.24 Currents (Closing on grid order)

Figure 4.25 shows the voltages of the thyristor-based hybrid DC CB of the closing sequence in normal condition. The breaker voltage v_{DCCB} falls down to zero by triggering the valve Tr1. It tracks the v_{C11} as long as the first time-delaying branch is conducting. Note that UFD S_1 starts closing when $v_{C11} > v_{SATr11}$. At this stage the voltage across UFD S_1 becomes negative (around -5 kV) which is the difference between clamping voltage V_{SA11_clamp}≈7 kV and the clamping voltage V_{SAT1_clamp}≈12 kV and this implies that S1 closes at zero current. Soon afterwards, T1 closes, v_{DCCB} becomes zero again and the current commutates to the load branch.

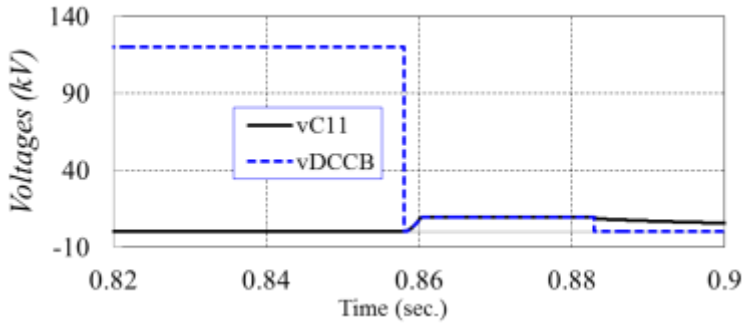

Figure 4.25 Voltages (Closing on grid order)

4.11 SIMULATION VERIFICATION OF MODEL WITH FAST THYRISTORS

As mentioned in section 4.5 and as it can be confirmed with simulation results in section 4.10, the main problem of thyristor-based hybrid DC CB with phase control thyristors is the long fault interuption time (longer than 5 ms). This time can be shorthened by employing fast thyristors and therefore fast thyristors are used in the final design.

4.11.1 OPENING ON GRID ORDER

Figure 4.26 shows the switching signals of the opening sequence on receiving grid order. It is seen that the signals have a pattern similar to those of the same test with phase control thyristors. Figure 4.27 shows the DC CB operating mode indicating that the mode is changed from “0“ (closed mode) to “1“ (tripped by grid order) at t≈0.5s.

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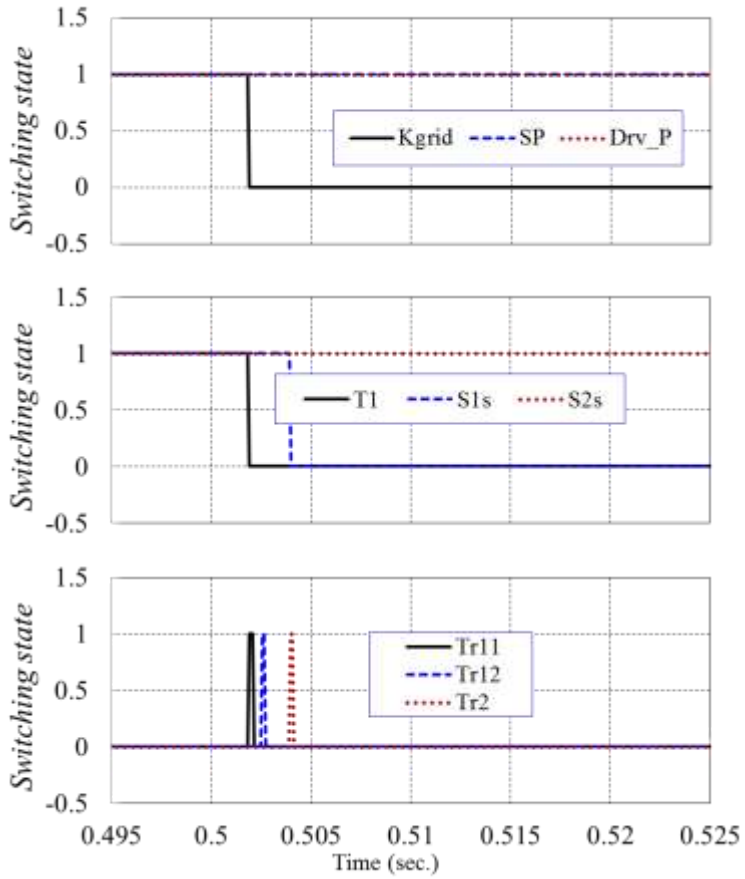

Figure 4.26 Switching signals (Opening on grid order, DC CB with fast thyristors)

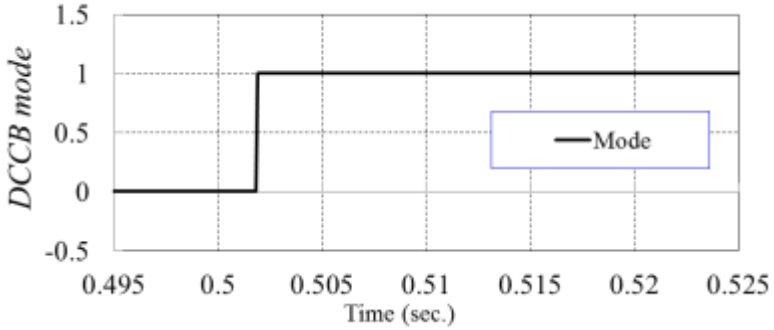

Figure 4.27 Switching signals (Opening on grid order, DC CB with fast thyristors)

Figure 4.28 shows the currents of the thyristor-based hybrid DC CB for the opening sequence on receiving grid order. The currents are also similar to those of the same test with phase control thyristors but with shorter time and smaller peak value. It is seen that the opening times with pase control and fast thyristors are respectively 10.5 ms and 2.5 ms. This is explained by the faster charging time of smaller capacitors and with smaller current. The opening time of 2.5ms is consistent with the experimental prototype reported in [15][16].

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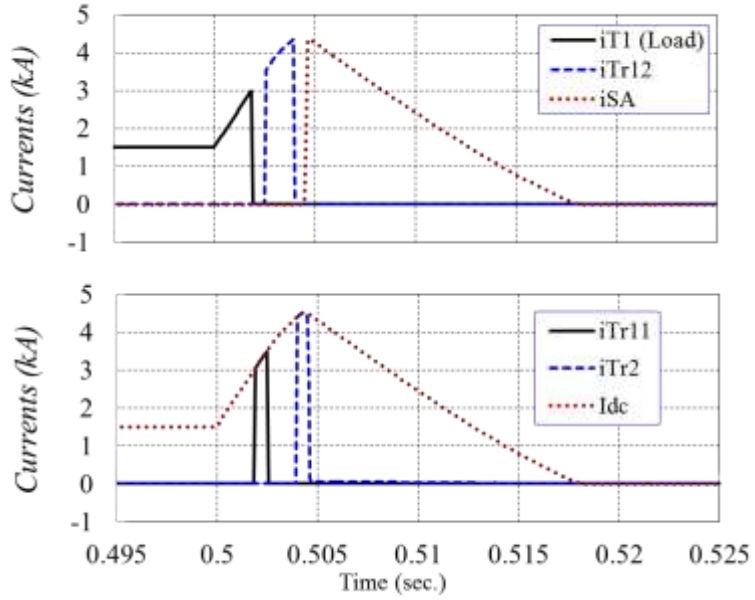

Figure 4.28 Branches currents (Opening on grid order, DC CB with fast thyristors)

Figure 4.29 shows the voltages of the thyristor-based hybrid DC CB for the opening sequence on receiving grid order. It is seen that the voltages are similar to those of the same test with phase control thyristors but with smaller time duration for charging of the capacitors.

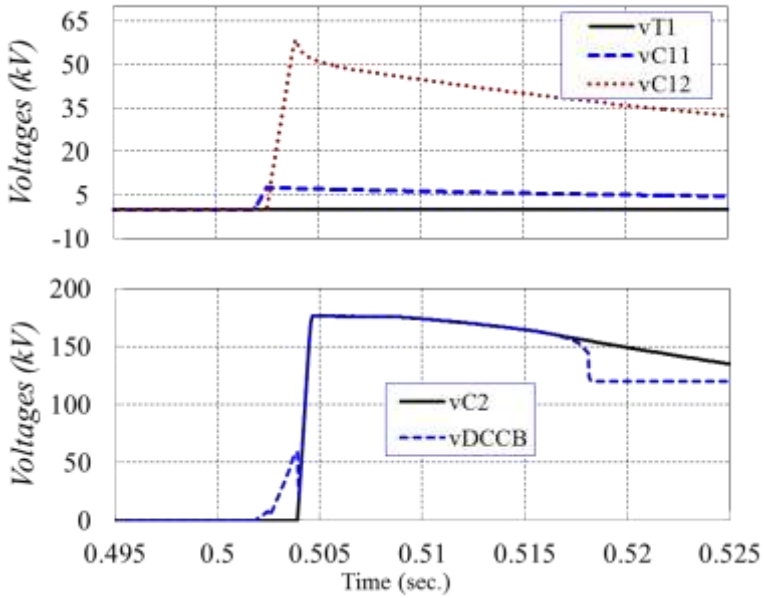

Figure 4.29 Capacitors and DC CB Voltages (Opening on grid order, DC CB with fast thyristors)

Figure 4.30 shows the junction temperature of each IGBT module of valve T1, and each thyristor of valves Tr1 and Tr2. It is seen that the temperatures are much smaller because of smaller and shorter fault current.

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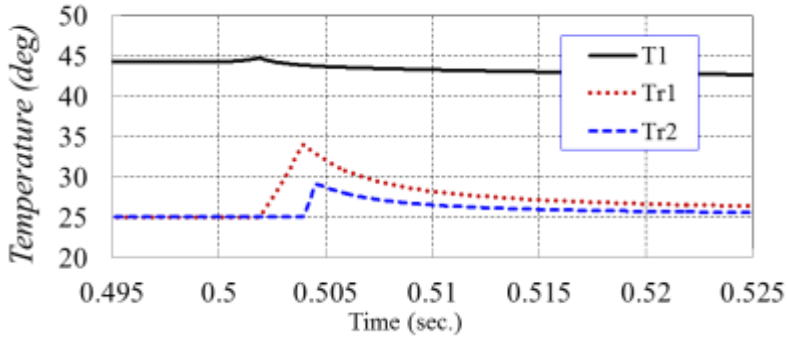

Figure 4.30 Junction temperature of the IGBT modules (T1) and thyristor modules (Tr1 and Tr2) (Opening on grid order, DC CB with fast thyristors)

4.11.2 OPENING ON SELF PROTECTION

Figure 4.31 shows the currents of the thyristor-based hybrid DC CB for opening DC CB on self-protection order. Comparing to the currents of section 4.10.2, it is seen that the currents are smaller with shorter time. It is worth noting that the current trip level for self-protection is much higher for this case (6.5 kA vs 4.5 kA with phase control thyristors) because of much shorter fault interruption time (see section 2.6). It is also seen that even with this larger current limit for triggering self-protection, the fault current remains below 7.5 kA with fast thyristors. Note that the current rises over 9 kA with phase control thyristor.

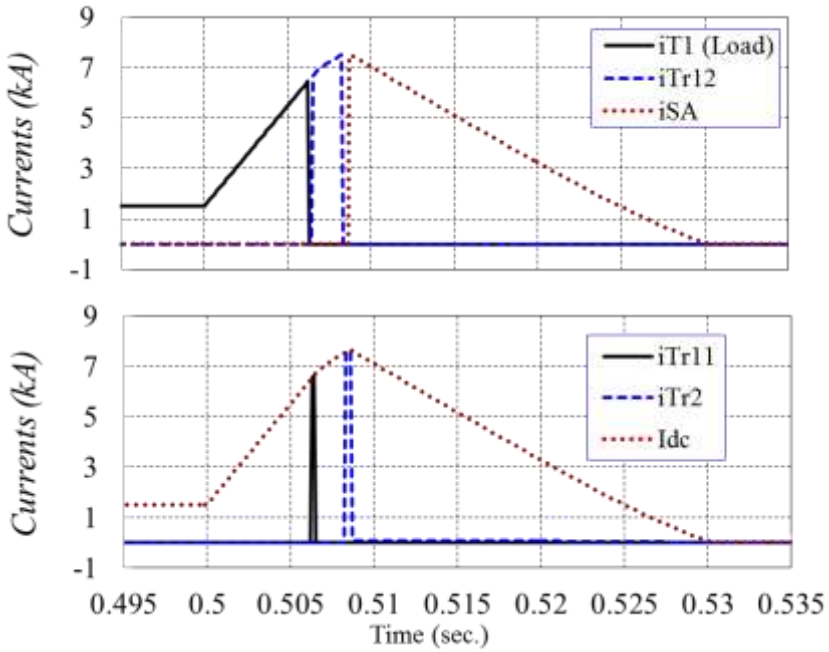

Figure 4.31 Branches currents (Opening on self-protection order, DC CB with fast thyristors)

Figure 4.32 shows the voltages of the thyristor-based hybrid DC CB for opening DC CB on self-protection order. It is seen that the capacitors are charged much faster than the capacitors in test case 4.10.2.

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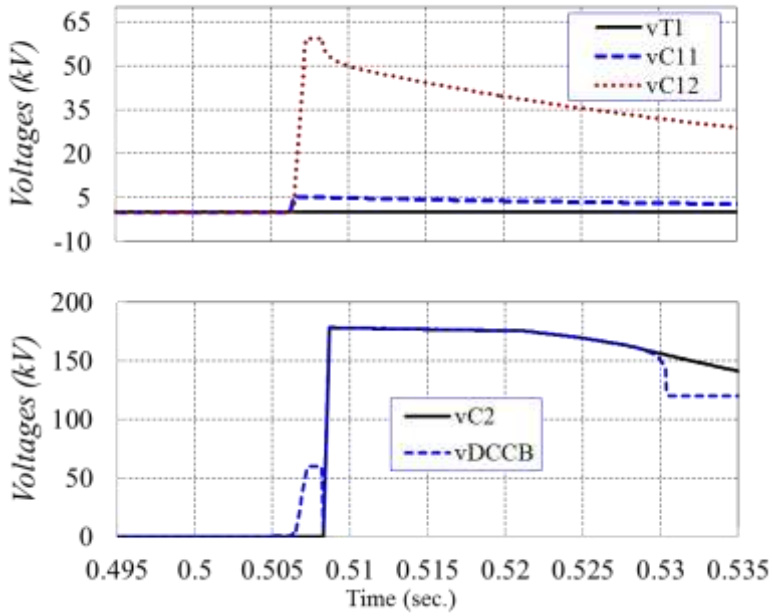

Figure 4.32 Capacitors and DC CB Voltages (Opening on self-protection order, DC CB with fast thyristors)

Figure 4.33 shows the junction temperature of each IGBT module of valve T1, and each thyristor of valves Tr1 and Tr2 for reclosing in fault.

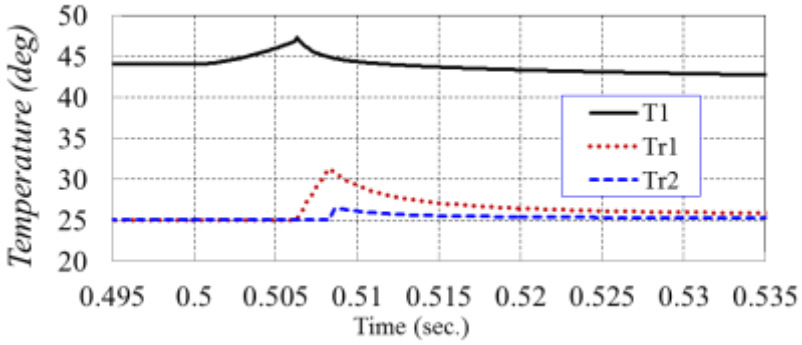

Figure 4.33 Junction temperature of the IGBT modules (T1) and thyristor modules (Tr1 and Tr2) (Opening on self-protection order, DC CB with fast thyristors)

4.11.3 SIMULATION WITH DIFFERENT PARAMETERS

The performance of the thyristor-based DC CB (with fast thyristor) is verified for a wide range of different parameters. Grid operator may want to change L_{dc} inductor to satisfy protection requirements. DC CB should operate well for a range of L_{dc}. Here two of the above tests (opening on self-protection and on grid order with two extreme series inductor L_{dc} are given. The other parameters are same as given in Table 4.6.

- **Opening on self-protection with L_{dc}=0.05 H**

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

The DC fault is applied at 0.5s and the grid protection is disabled. The L_{dc} is selected very small (L_{dc}=0.05 H) to investigate its impact on the breaker operation.

Figure 4.34 shows the operating mode of the DC CB on self-protection order. It is seen that the DC CB is tripped by self-protection at t≈0.5s. The switching states are similar to those in the test case opening on self-protection but with shorter time (because of smaller L_{dc}) and therefore are not shown here.

Figure 4.35 shows the the currents of the thyristor-based hybrid DC CB for the same fault. It is seen that the overal fault interuption time is shorter than the interuption time in Figure 4.31. It is because of smaller L_{dc} that allows larger slope of fault current and faster charging of the capacitors. The calculated trip level for self protection is 2.5 kA (based on V_{dc}, T_{int} and L_{dc}). However, the controller limits the lower value for self protection trip level to 3 kA to avoid interference with normal load current. Therefore trip signal is sent at 3 kA and the fault current rises faster because of small L_{dc}.

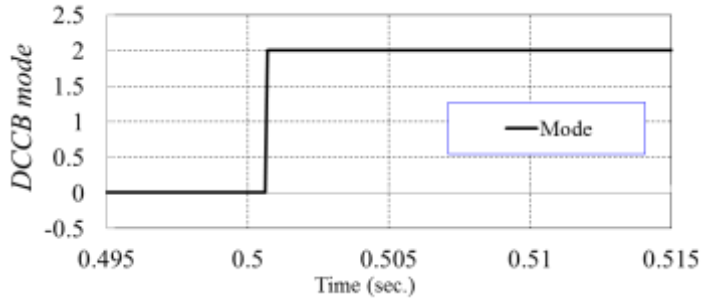

Figure 4.34 Operating mode (Opening on self-protection, DC CB with fast thyristors, L_{dc}=0.05 H)

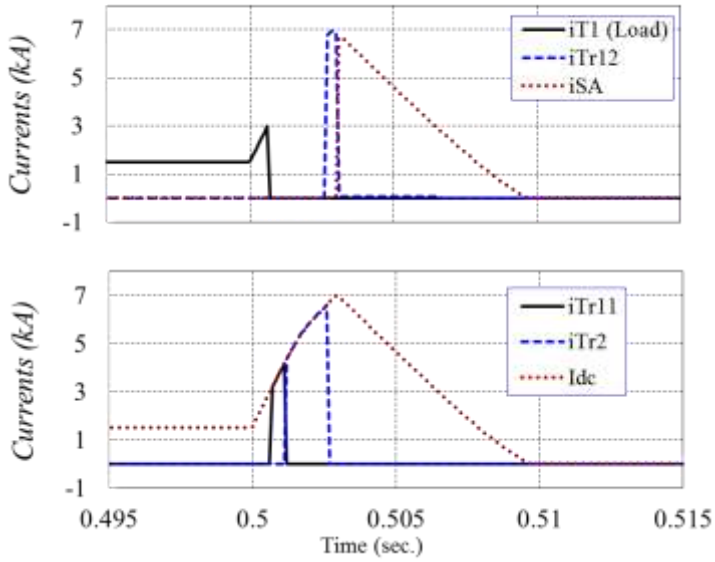

Figure 4.35 Branches currents (Opening on self-protection, DC CB with fast thyristors, L_{dc}=0.05 H)

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

Figure 4.36 shows the voltages of the thyristor-based hybrid DC CB with L_{dc}=0.05 H of the opening sequence on self protection order.

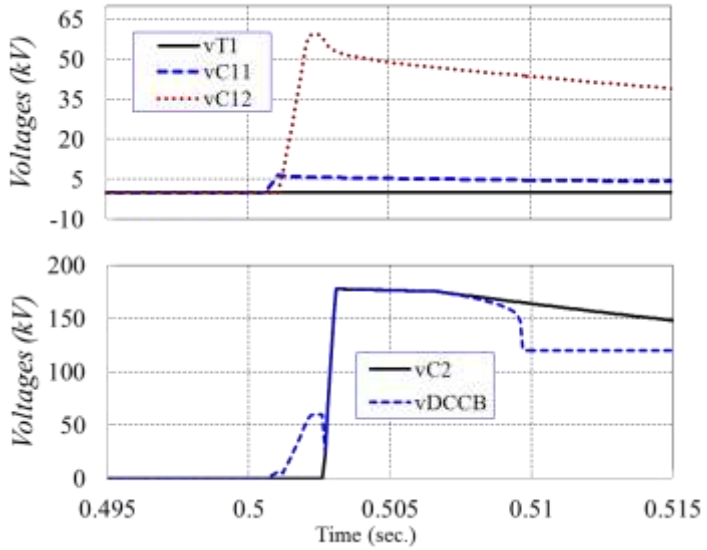

Figure 4.36 Capacitors and DC CB Voltages (Opening on self-protection, DC CB with fast thyristors, L_{dc}=0.05 H)

Figure 4.37 shows the junction temperature of each IGBT module of valve T1, and each thyristor of valves Tr1 and Tr2 of the DC CB with L_{dc}=0.05 H of the opening sequence on self protection order.

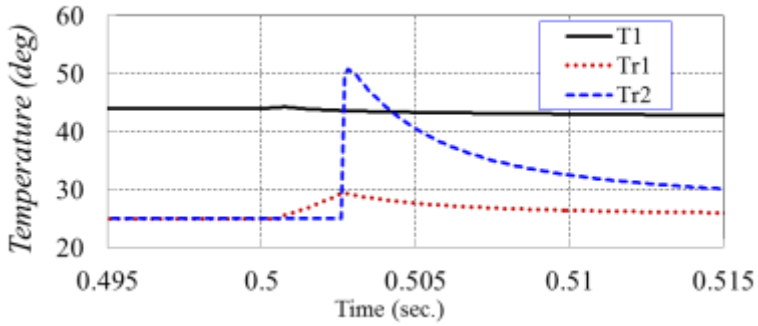

Figure 4.37 Junction temperature of the IGBT modules (T1) and thyristor modules (Tr1 and Tr2) (Opening on self-protection, DC CB with fast thyristors, L_{dc}=0.05 H)

- **Opening on grid order with L_{dc}=0.8 H**

The opening on grid order test case is repeated with extreme large inductor L_{dc}=0.8 H. The switching signals are similar to the test case in section 4.11.1 but with longer time because of larger L_{dc}.

Figure 4.38 shows the the currents of the thyristor-based hybrid DC CB with L_{dc}=0.8 H when opening on grid order. Comparing with current of Figure 4.28, it is seen that the fault interuption time is longer but with smaller peak current, which is expected.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

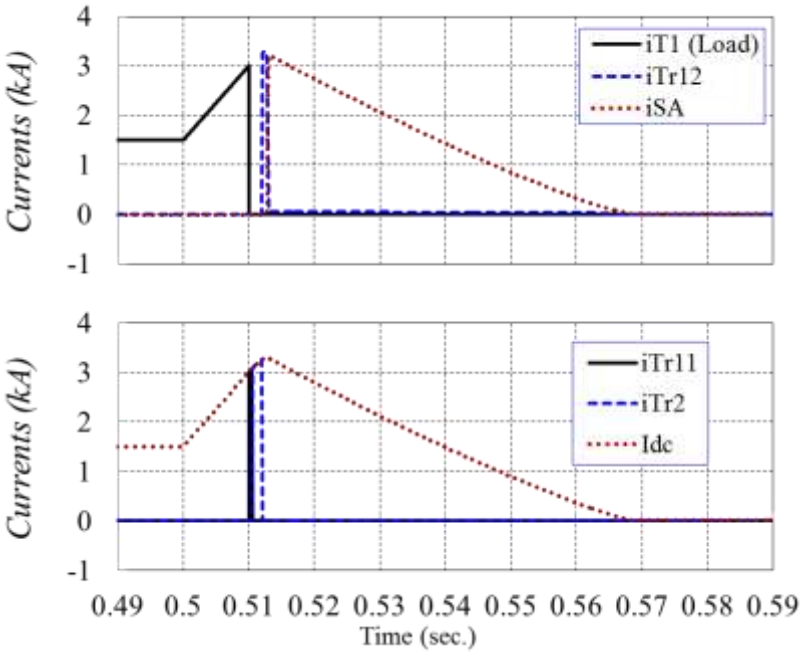

Figure 4.38 Branches currents (Opening on grid order, DC CB with fast thyristors, L_{dc}=0.8 H)

Figure 4.39 shows the voltages of the thyristor-based hybrid DC CB with L_{dc}=0.8 H when the DC CB is opening on grid order.

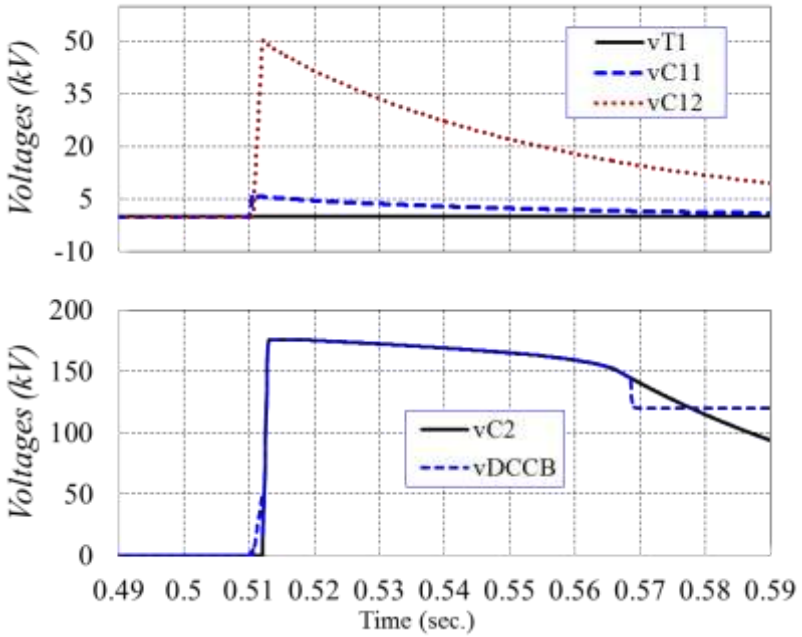

Figure 4.39 Capacitors and DC CB Voltages (Opening on grid order, DC CB with fast thyristors, L_{dc}=0.8 H)

Figure 4.40 shows the junction temperature of each IGBT module of valve T1, and each thyristor of valves Tr1 and Tr2.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

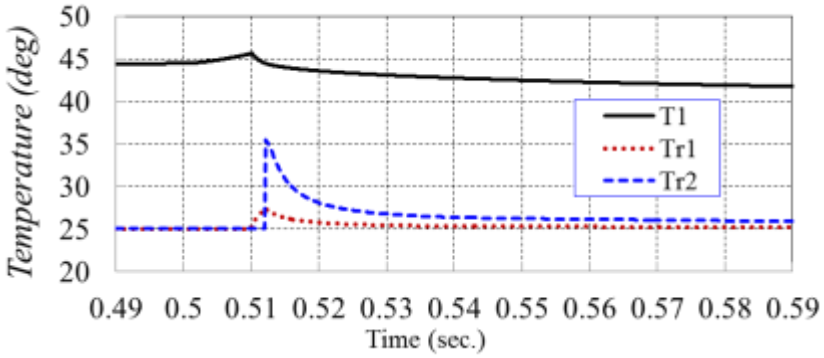

Figure 4.40 Junction temperature of the IGBT modules (T1) and thyristor modules (Tr1 and Tr2) (Opening on grid order, DC CB with fast thyristors, L_{dc}=0.8 H)

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5 CONCLUSION

Hybrid DC CB is an essential DC grid component and two particular designs are selected for study and modelling: IGBT- based and thyristor-based hybrid DC CBs.

The DC CB models in this task are intended for system level off-line studies like DC grid protection development and transient studies involving DC faults. It is therefore recommended that investigation and modelling should include the following:

1. The normal current branch and its main components,
2. The main breaker branch(es) with all main components,
3. Energy absorption branch
4. The residual current breaker,
5. The opening sequence controller,
6. The closing sequence controller,
7. The self-protection which incorporates overcurrent and thermal protection,

Some other functions like proactive breaking and fault current limiting are not included in this model because of complexity, lack of information, and complex interaction with grid-level protection.

After detailed design investigations for thyristor-based DC CB, it was determined that if phase control thyristors are employed the opening time is in the order of 5-9 ms. This is slower than expected and therefore full design with fast control thyristors is also presented, which confirms that opening time can be reduced to 2-3 ms.
The PSCAD simulation results (for both IGBT-based and thyristor-based DC CBs) are presented for the following operating conditions:

1. Opening on grid protection order,
2. Opening on self-protection,
3. Closing on grid order,

The IGBT-based DC CB model is also verified for reclosing into a permanent fault. But the performance of the thyristor-based DC CB is not investigated for this extreme test case.

The simulation results for IGBT- based DC CB and thyristor-based DC CB confirm all design assumptions. Thyristor-based DC CB is simulated with both phase control thyristors and fast thyristors and the assumed opening times are confirmed.

Both DCCBs are tested for a wide range of different series inductors, and it is found that the designs are adequately robust.

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6 REFERENCES

[1] Bucher, M., Frank, C.: 'Analytical approximation of fault current contributions from capacitive components in HVDC cable networks', IEEE Trans. Power Del., 2015, **30**, (1), pp. 74-81.

[2] Jovcic, D., Taherbaneh, M., Taisne, J., *et al.*:'Topology assessment for 3+3 terminal offshore DC grid considering DC fault management', IET Gener. Transm. Distrib., 2015, **9**, (3), pp. 221-230.

[3] Gowaid, I., Elserougi, A., Abdel-Khalik, A., *et al.*: 'A series flywheel architecture for power levelling and mitigation of DC voltage transients in multi-terminal HVDC grids', IET Gener. Transm. Distrib., 2014, **8**, (12), pp. 1951-1959.

[4] Park, K., Chen, Z.: 'Control and dynamic analysis of a parallel-connected single active bridge DC-DC converter for DC –grid wind farm application', IET Power Electron., 2015, **8**, (5), pp. 665-671.

[5] Francos, P., Verdugo, S., Alvarez, H, *et al.*: 'INELFE Europe's first integrated onshore HVDC interconnection'. Proc. IEEE PES General Meeting, San Diego, USA, Jul 2012, pp. 1-8.

[6] Shukla, A., Demetriades, G.: 'A survey on hybrid circuit-breaker topologies', IEEE Trans. Power Del., 2015, **30**, (2), pp. 627-641.

[7] Häfner, J., Jacobson, B.: 'Proactive Hybrid HVDC Breakers - A key innovation for reliable HVDC grids'. Proc. CIGRE 2011 Bologna Symp., Bologna, Italy, Sep 2012, pp. 1-7.

[8] Dijkhuizen, F., Berggren, B., 'Zoning in high voltage DC (HVDC) grids using hybrid DC breaker'. Proc. EPRI HVDC and FACTS conference, Palo Alto, USA, AUG. 2013, pp. 1-8.

[9] Derakhshanfar, R., Jonsson, T., Steiger, U., *et al.*: 'Hybrid HVDC breaker-A solution for future HVDC system'. Proc. CIGRÉ Session, Paris, France, Aug 2014, pp. 1-12.

[10] Sano, K., Takasaki, M.: 'A surge-less solid-state dc circuit breaker for voltage source converter based HVDC transmission systems'. IEEE Trans. Ind. Appl., 2014, **50**, (4), pp. 2690-2699.

[11] Eriksson, T., Backman, M., Halen, S., *et al.*: 'A low loss mechanical HVDC breaker for HVDC grid applications'. Proc. CIGRÉ Session, Paris, France, Aug 2014, pp. 1-18.

[12] Tahata, K., Oukaili, S., Kamei, K., *et al.*: 'HVDC circuit breakers for HVDC grid applications', Proc. IET ACDC 2015 conference, Birmingham, UK, Feb 2015, pp. 1-9.

[13] Shi, Z., Zhang, Y., Jia, S., et al., 'Design and numerical investigation of a HVDC vacuum swich based on artificial current zero', IEEE Trans. Dielectr. Electr. Insul., 2015, **22**, (1), pp. 135-141.

[14] Hassanpoor, A., Häfner, J., Jacobson, B.: 'Technical assessment of load commutation switch in hybrid HVDC breaker', IEEE Trans. Power Electron., 2015, **30**, (1), pp. 5393-5400.

[15] Davidson, C., Whitehouse, R., Barker, C., *et al.*:'A new ultra-fast HVDC circuit breaker for meshed DC networks', Proc. IET ACDC 2015 conference, Birmingham, UK, Feb 2015, pp. 1-7.

[16] Grieshaber,W., Dupraz, J., Penache, D., *et al.*: 'Development and Test of a 120 kV direct current circuit breaker'. Proc. CIGRÉ Session, Paris, France, Aug 2014, pp. 1-11.

[17] Wang, Y., Marquardt, R., 'Future HVDC-grids employing modular multilevel converters and hybrid DC-breakers'. Proc. EPE, Lille, France, Sep 2013, pp. 1-8.

[18] Wang, Y., Marquardt, R.: 'A fast switching, scalable DC-breaker for meshed HVDC-Supergrids'. Proc. PCIM Europe, Nuremberg, Germany, May 2014, pp. 1-7.

[19] Kontos, E., Pinto, R., Rodrigues, S., *et al.*:'Impact of HVDC transmission system topology on multiterminal DC network faults', IEEE Trans. Power Del., 2015, **30**, (2), pp. 844-852.

[20] Sneath, J., Rajapakse, A.: 'Fault detection and interruption in an earthed HVDC grid using ROCOV and hybrid DC breakers', IEEE Trans. Power Del., DOI: 10.1109/TPWRD.2014.2364547

[21] Ahmed, N., Angquist, L., Mahmood, S., *et al.*: 'Efficient modelling of an MMC-based multiterminal DC system employing hybrid HVDC breakers', IEEE Trans. Power Del., DOI: 10.1109/TPWRD.2015.2398825.

[22] Jovcic, D., Taherbaneh, M., Taisne, J., *et al.*: 'Offshore DC grids as an interconnection of radical systems: protection and control aspects', IEEE Trans. Smart Grid, 2015, **6**, (2), pp. 903-910.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

[23] Yu, F., Lin, W., Wang, X., et al.: 'Fast voltage-balancing control and fast numerical simulation model for modular multilevel converter', IEEE Trans. Power Del., 2015, **30**, (1), pp. 220-228.

[24] Mahseredjian, J., Dennetière, S., Dubé, L., *et al.*: 'On a New Approach for the Simulation of Transients in Power Systems'. Electric Power Systems Research, 2007, **77**, (1), pp. 1514-1520.

[25] Peralta, J., Saad, H., Dennetière, S., *et al.*: 'Detailed and average models for a 401-level MMC-HVDC system'. IEEE Trans. Power Del., 2012, 27, (3), pp. 1501-1508.

[26] D. Jovcic and K Ahmed, "High Voltage Direct Current Transmission: Converters Systems and DC grids", Wiley 2015.

[27] M. Pinaki ; C. Wikström, N. Johanesson; T. Larsson , "First real-time implementation of DC grid protection strategy",AC and DC Power Transmission, 11th IET International Conference on, Feb. 2015

[28] J. Hafner, B. Jacobson, "Proactive Hybrid HVDC Breakers-A key innovation for reliable HVDC grids", Cigre meeting, Bolognal, 2011.

[29] W. Grieshaber, J. P. Dupraz, D. L. Penache, L. Violleau, "Development and test of a 120 kV direct current circuit breaker", Cigre meeting, Paris, 2014.

[30] P. Skarby, U. Steiger, "An Ultra-fast Disconneting Switch for a Hybrid HVDC breaker-a technical breakthrough", Cigre meeting, Canada, 2013.

[31] M. RAHIMO at all. "The Bimode Insulated Gate Transistor (BIGT), an ideal power semiconductor for power electronics based DC Breaker applications" CIGRE Parsis session 2014, paper B4-302.

[32] Liutauras Storasta at all "Optimized Power Semiconductors for the Power Electronics Based HVDC Breaker Application" PCIM Europe, Nuremberg, May 2015.

[33] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, Losses, and Semiconductor Requirements of Modular Multilevel Converters", IEEE Trans. INDUSTRIAL ELECTRONICS, 2010, 57 (8), pp. 2633-2642.

[34] [online],https://library.e.abb.com/public/871a1c55cd6a4d96a3abe408f7fa123b/5SNA%202000K450300%205SYA%201431-00%2005-2015.pdf, [Accessed: 02-Dec-2016]

[35] PC27.104™/D9, "Draft Guide for Automatic Reclosing of Circuit Breakers for AC Distribution and Transmission Lines", Power System Relaying Committee, IEEE Power and Energy Society, April 2012

[36] [online],https://library.e.abb.com/public/2b46fe067bbb45fe87ba1b3d735356ce/5STP%2048Y7200_5SYA1076-02%20Oct%2016.pdf, [Accessed: 02-Dec-2016]

[37] [online], https://library.e.abb.com/public/c822c598abbd44a2bd4a3bef65641b43/5STF_28H2060.pdf , [Accessed: 02-Dec-2016]

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.