PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

D6.2 Develop system level model for mechanical DCCB

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List of Contributors

Work Package 6 and deliverable 6.2 involve a large number of partners and contributors. The names of the partners, who contributed to the present deliverable, are presented in the following table.

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1 EXECUTIVE SUMMARY

This report presents the results of Task 6.2 of WP6 “HVDC circuit breaker performance characterization”. The objective of Task 6.2 is the development of a PSCAD system-level model of the mechanical DC circuit breaker with active current injection. This will then be used for DC grid protection studies in WP4 and WP9.

The circuit breaker topology consists of a mechanical interrupter with parallel circuit used to inject a counter-current, creating a current zero. Typically, the natural frequency of this current injection is high – in the order of several kHz - and internal transients within the circuit breaker during operation are very fast. For system level studies, it is challenging to replicate these whilst also maintaining reasonable simulation times.

The report presents two system level models, of different complexity. Model 1 includes the current injection circuit; Model 2 does not. By neglecting the current injection circuit the highest frequency transients are removed, which allows a longer time-step to be used.

The two model types are implemented in PSCAD and demonstrated 320kV, using a simple validation circuit. Simulation results indicate that Model 1 requires a very small time-step (less than 1µs) to accurately capture the fast transients within the breaker. Model 2 does not replicate the initial transient interruption voltage (TIV) across the main interrupter, which results in a small difference in peak current and energy dissipation requirements. Both models are then demonstrated for robustness, to ensure that they perform as expected. Validation simulations show clearing of faults from a synthesised relay trip order and failed interruption, when current is over circuit breaker rating.

It is shown that the error introduced by Model 2 are acceptable (within approximately 2%), and have little to no effect on the HVDC system. When conducting simulation studies of large, multi-terminal HVDC network, this model may be more suitable. Moreover, the time-step is limited by hardware capability in the real time studies performed in WP9. As such, a model that can operate with a longer time-step is required.

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2 NOMENCLATURE

S_1	Vacuum interrupter (VI)
S_2	Residual current circuit breaker
S_3	High speed switch used to inject counter-current
I_{s1}	Chopping current of switch S_1
I_{s2}	Chopping current of switch S_2
I_{s3}	Chopping current of switch S_3
I_{VI}	Current flowing through the main interrupter (S_1)
I_{cb}	Current flowing through the dc breaker (S_2)
I_p	Current flowing through the parallel circuit (S_3)
I_{sa}	Current flowing through surge arrester
V_{vi}	Voltage across main interrupter (S_1)
V_{sa}	Voltage across surge arrester
V_c	Voltage across capacitor
V_{dcn}	Rated pole-to-ground DC voltage
V_{SAn}	Nominal voltage of the arrester (1pu)
E_{sa}	Surge arrester energy dissipation
T_{s1}	Operation time of switch S_1
T_{s2}	Operation time of switch S_2
T_{s3}	Operation time of switch S_3
L_p	Inductance of the parallel circuit
C_p	Capacitance of the parallel circuit
SA	Surge arrester
DCR	Additional dc inductance
DCCB	DC circuit breaker
TIV	Transient interruption voltage

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3 INTRODUCTION

3.1 DC GRIDS

In the near future, the existing transmission systems are expected to undergo several modifications to accommodate the growth of renewable energy sources (RES) into the market. The development of Voltage Source Converter (VSC) based HVDC gives full control over active and reactive power, allowing connection to offshore wind or weak networks. The fixed voltage polarity also allows converters to be readily connected in parallel, making multi-terminal networks feasible. This facilitates the development of a meshed network, rather than a number of point-to-point links, to be established [1]. In such case, the number of converter stations required may be reduced and transmission efficiency increased.

Small scale DC networks are likely to be below the maximum loss of infeed specified by Transmission System Operators (TSO), therefore the stability of the connected AC system is not expected to be jeopardized after DC faults. However, larger DC networks will have a significant impact on the AC network during DC disturbances [2]. These should not lead to damage of HVDC equipment or unacceptably influences on the ac network – instability through loss of power throughput, for example. Therefore, an adequate protection scheme is necessary. One of the key components of a DC protection scheme is the HVDC circuit breaker, which would allow isolation of faulted segments of the network and permit the healthy areas to continue to operate.

In Work Package 6, a number of dc breaker models are being constructed. These will then be used in other work packages to assess protection strategies. Task 6.1 and Task 6.2 deal with different types of CB models based on technologies from different manufacturers. In this document, the system level model of the mechanical circuit breaker with active current injection is described.

3.2 SCOPE OF MECHANICAL DC BREAKER SYSTEM LEVEL MODELLING

The aim of Work Package 6 is to deliver HVDC circuit breaker models for system level and component level studies. These will then be used for assessing dc protection strategies (WP 4, WP 9) and evaluation of circuit breaker performance (WP 5, WP10). In WP 6, two HVDC circuit breaker topologies will be investigated: the hybrid circuit breaker and the mechanical circuit breaker with active current injection. Table 3.1 gives an overview of the interactions between the outputs of WP 6 tasks and other work packages.

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Table 3.1: Selected tasks in Work Package 6

MODEL	TASK 6.1	TASK 6.2	TASK 6.3	TASK 6.4
Breaker Type	Hybrid Breaker	Mechanical breaker (current injection)	Hybrid breaker	Mechanical breaker (current injection)
Model Type	System level	System level	Component level	Component Level
Output/ coordination with	WP4/WP5/ WP9	WP2/WP4/WP5/ WP9	WP10	WP10

In WP2 a simulative analysis of two or three meshed offshore grid topologies is performed to define recommendations for minimum requirements on future meshed DC power systems in order to adapt and extend existing grid codes. As WP 2 is expected to provide meshed DC grid benchmark networks, intensive exchange with WP3, WP4 and WP6 is required to enable the inclusion of all the aspects relevant to DC grids operation (i.e. converter models, DC protection schemes and DCCB models respectively).

WP 4 will investigate the relative performance of a number of fault clearing strategies and components (dc circuit breakers, disconnectors, ac breakers, blocking converters, etc.) in meshed offshore HVDC networks. The dc fault clearing strategies are expected to protect the dc system components and ensure that the ac system continues to function adequately. The goal of WP 4 is to highlight the protection schemes which have the best performance, for the lowest cost.

In WP 9 the protection schemes selected in WP4 will be evaluated with a real time digital simulator. This will be used to test the performance of protection practical protection relays using hardware in the loop.

WP 5 will define the test circuit requirements to be used in WP 10 (circuit breaker testing). A system level model will be used to evaluate the requirements of the test circuit, through multi-terminal HVDC network simulations. This will allow equivalent test circuits, that replicate circuit breaker stresses, to be realised using currently available equipment (e.g. power frequency ac short circuit generators).

The system level model, developed in Task 6.2, shall be used in WP2, WP 4, WP 5 and WP 9. This model must provide adequate representation of the circuit breaker for system analysis, as it will be then implemented in larger, multi-terminal grids. The key circuit breaker characteristics for these studies are maximum interruption current and operating time, etc. The internal stresses and performances will be investigated in depth by the component level models developed in Task 6.3 and Task 6.4 in collaboration with WP 10 (practical breaker testing). Therefore, mechanical delays and maximum capabilities (such

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as peak current breaking capability) should be included but the level of detail should be minimal to avoid unnecessary complexity.

3.2.1 DEFINITION OF SYSTEM LEVEL MODEL

System level models are applied to studies using multi-terminal HVDC networks. Their aim is to evaluate system performance when dc breakers are included, and the requirements of the breakers (imposed by the system). As such, the internal characteristics of the circuit breaker (i.e. interaction between sub-components) are not considered. For example, in ac system studies the arc generated between contacts is not considered.

The simplest representation of a dc circuit breaker system level model is an ideal switch in parallel with a surge arrester (SA). An artificial delay between the trip signal and the switch opening should be included to emulate mechanical and electrical delays that occur in the practical breaker. Maximum capabilities (such as interrupting current) may also be incorporated. These features vary on topology of the circuit breaker used.

3.2.2 DEFINITION OF COMPONENT LEVEL MODEL

Component level models include internal components, such as mechanical interrupters, power electronic devices, surge arresters thermal characteristics, etc. This allows the interaction between, and performance of, sub-components to be assessed. In the case of the mechanical breaker, the electrical stresses on the mechanical interrupter will be modelled in detail, to assess its performance and capability to withstand the high di/dt and dv/dt imposed by the resonant circuit around current zero. For hybrid dc circuit breakers, component level models are used to assess semiconductor stresses.

Mayer and Cassie thermal arc equations may be used when modelling passive resonant mechanical breakers, where Gas Circuit Breakers (GCB) are typically applied [3]. However, mechanical breakers with current injection typically use vacuum interrupter because of their superior di/dt and dv/dt capabilities, which allows higher frequency operation.

There have been several attempts to develop arc models of a vacuum interrupter by considering the plasma (metal ions and electrons) behaviour between the electrodes [3]. Despite these efforts, there are currently no convenient arc models for a vacuum interrupter applicable to thermal interruption process. It may be possible to use empirical data to determine critical interrupting thresholds for VCB (e.g. the critical slope of current). However, there are many interdependent factors which influence interruption success, which may be difficult to quantify individually.

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3.3 BACKGROUND ON MECHANICAL DC CIRCUIT BREAKER MODELLING

Several mechanical DC circuit breaker models have been presented in the literature. The level of complexity of such models changes according to their applications. More simplistic models, like the one presented in [3], [5] and [6], are conceived to be applied in system-level studies. More accurate models (i.e. in [7]) are used to understand the physical performance as well as the interactions and stresses between internal components. A brief overview of the mechanical DCCB models available from the literature is presented hereafter.

The DC circuit breaker model presented in [5] consists of a series of modularized vacuum switches to achieve the required system voltage level. The layout of a single module consists of three parallel branches: the vacuum interrupter, the metal oxide arrester and a RC snubber. To achieve high voltage DC interruption the modules are placed in parallel with a commutation branch. In this model, a triggered sphere gap is adopted as commutation switch to obtain bidirectional DC interruption. After the commutation process, an oscillating residual current can appear due to the low arc extinguishing capability of the triggered sphere gap. The residual current is usually interrupted by the back-up switches. The model is quite detailed, which takes into account most of the significant system-level features of the breaker. Nevertheless, a number of relevant aspects for system-level studies, such as the influence of simulation time-step, control system and reclosing logic, are not included in the model.

In [6], an EMTP (electromagnetic transient program) model of the mechanical DCCB for transmission applications is presented. The model includes the main hardware components (ideal switches with delay, resonant circuit, surge arrester), the control logic and interlocks between sub-components, and self-protection feature in case of failure of the DC protection scheme. The model proved to be robust to a large range of operating conditions (DC fault clearing, reclosing operation, self-protection, reclosing into a DC fault). Despite being a valuable starting point for developing a system level model of the mechanical DCCB with active current injection, the model results too detailed for system-level studies (as intended in WP4) and it is not compatible for RTDS applications as it would require a very fast time sample.

In [7] a vacuum circuit breaker was modelled in detail using electromagnetic transient simulation program (PSCAD). It including: (i) the nature of arcing time, (ii) current chopping ability, (iii) characteristic recovery dielectric strength between contacts during opening and (iv) quenching capability of high frequency current at zero crossing.

The core of this deliverable is to provide a model of the mechanical DCCB with active current injection, suitable for system-level studies. To allow a broad range of studies to be performed (on RTDS, for example) the level of detail of the vacuum interrupter modelling and other components should be intentionally reduced. At the same time, the model should be as realistic as possible, so that reasonable conclusions can be drawn when it is used in

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other studies - dc system protection studies, for example. In WP6.4 a more detailed, component–level, DCCB model will be included investigated.

3.4 REPORT OVERVIEW

The remainder of the report is organized in further five chapters. In Chapter 4, an overview of the fundaments of DC circuit breaker performance is presented. The main types of mechanical DC circuit breakers are described, including arc voltage mechanical circuit breaker, mechanical circuit breaker with passive oscillation and mechanical circuit breaker with active current injection. The operation sequence and the key components of the mechanical DC circuit breaker with active current injection are presented in Chapter 5. These include: vacuum interrupter, parallel oscillation circuit, surge arrester and residual current circuit breaker. In Chapter 6 two modelling options for mechanical DCCB system-level model are introduced: Model 1 includes all components presented in Chapter 5, whereas Model 2 is a reduced complexity representation, more suitable for large system and real time simulation studies. In Chapter 7, the performance of the mechanical DCCB system level model is compared using Model 1 and Model 2 considering 320 kV in a number of case studies to prove its robustness. Finally, conclusions are drawn in Chapter 8.

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4 MECHANICAL DC BREAKERS

4.1 FUNDAMENTALS OF DC BREAKERS

Faults within dc systems result in high currents that propagate rapidly. DC breakers used in multi-terminal networks must force an artificial current zero, whilst also dissipating significant amounts of energy. A number of dc breaker topologies have been developed for this purpose, which have different operating principles. Common principles are described below.

4.1.1 ARTIFICIAL CURRENT ZERO CREATION

In dc systems, current zeros do not occur naturally. To generate a current zero a dc breaker must generate a counter-voltage, to force current down. Eq. (1) gives a simplistic relationship between the source (HVDC system/converter) voltage V_s, counter-voltage generated by the breaker V_{CB}, system inductance L and the current through the circuit breaker V_{CB}. The greater the difference between the source voltage and the counter-voltage the larger resulting di/dt will be, bringing current to zero faster and reducing energy dissipation. . To achieve a negative di/dt (and, thus, a current zero) condition Eq. (2) must be met. This shows the counter-voltage (V_{cb}) generated by the circuit breaker must exceed that of the source. A higher circuit breaker voltage results in a higher di/dt; decreasing current decay time (see Figure 4.1).

$$\frac{d}{dt}i(t) = \frac{V_s - V_{\text{cb}}}{L} \quad (1)$$

$$V_{\text{cb}} \geq V_s \quad (2)$$

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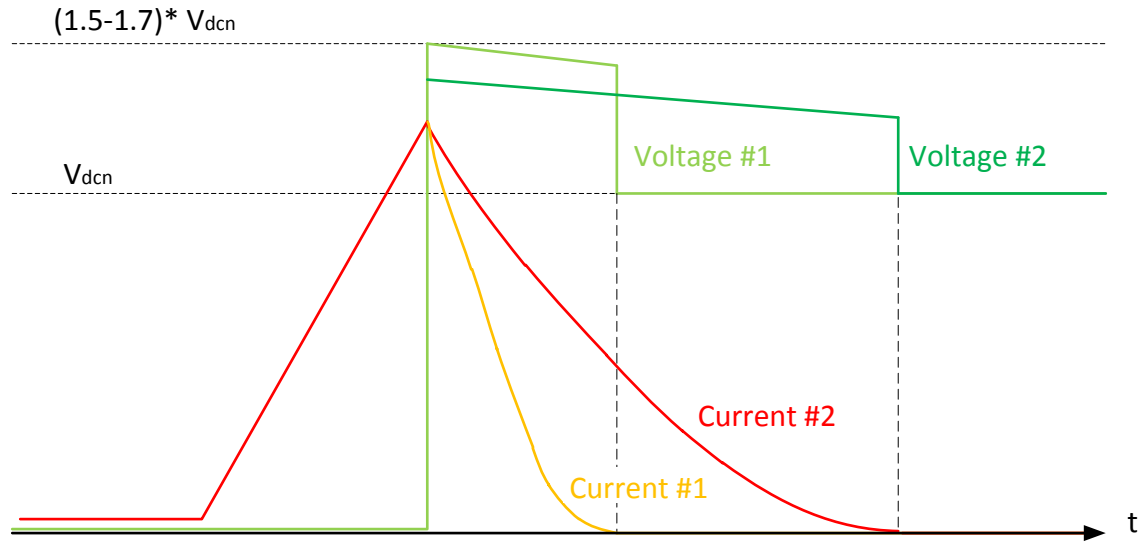

Figure 4.1: Influences for MOSA clamping level on circuit breaker current decay. In the figure, two voltage and current waveforms are shown, to demonstrate the impact higher circuit breaker voltage has on current decay time.

4.1.2 DC REACTOR

Faults in HVDC systems cause a higher rate of rise of current and steady-state value, than those seen in HVAC systems. As such, breaking the current at its steady-state value is a significant challenge. Breaking time is also critical within HVDC systems, and breakers are expected to operate in the first 5-10ms from a fault transient taking place. Breakers are typically designed to operate during the transient stage of the fault, as shown in Figure 4.2. To reduce the peak current the breaker must clear, it is common that additional dc reactance (DCR) is applied. This can then be used to profile the current to an acceptable level, for a given circuit breaker operation time. In a practical system the size of DCR is found through system analysis to ensure it satisfies a range of requirements, such as reducing circuit breaker breaking current, ensuring system controllability, etc.

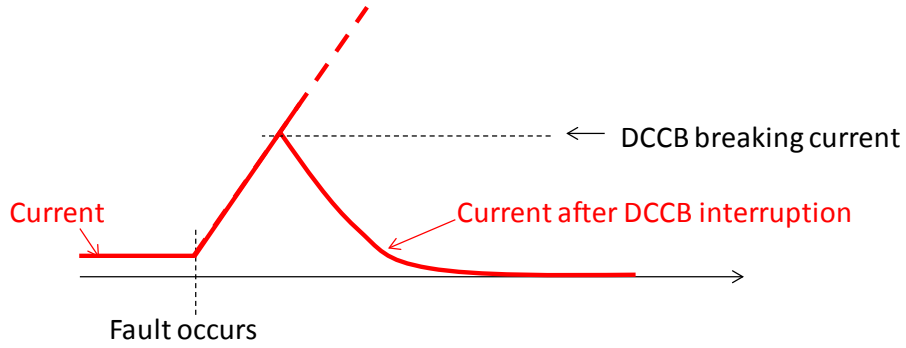

Figure 4.2: HVDC Circuit breaker current during breaker operation

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4.2 MECHANICAL DC BREAKER TOPOLOGIES

Several circuit breaker topologies are currently under investigation. Each of these must perform two functions: primarily, they must generate a counter-voltage large enough to reduce current to zero; secondly, they must absorb a significant amount of energy (in the order of several MJ) during breaking.

4.2.1 ARC VOLTAGE MECHANICAL CIRCUIT BREAKER

In Figure 4.3, the circuit topology of an arc voltage mechanical circuit breaker is shown. In this scheme, when a fault occurs the interrupter is opened and an arc is generated between the contacts. To force a current zero, the arc voltage must be sufficiently high – larger than the system voltage. Arc chutes are typically used to stretch the arc length, increasing its voltage. This scheme is often applied to low voltage class DC No-Fuse Breaker (NFB). For example, 1.5kV high-speed switches are used for railway power systems [8]. However, HVDC applications require very high breaker counter-voltages. In practice voltage and energy requirements are too severe for this topology to be used: arc chutes become very large, heavy and bulky and dissipating the stored energy of the system becomes challenging.

Figure 4.3: Arc voltage mechanical dc breaker

4.2.2 MECHANICAL CIRCUIT BREAKER WITH PASSIVE RESONANCE

In the mechanical circuit breaker with passive resonance, the interrupter and parallel inductor-capacitor branch form a resonant circuit, as shown Figure 4.4 . When the interrupter is opened, an arc is generated between the contacts. Air or SF6 circuit breakers are often used for the interrupter. The voltage generated forces a resonant current in the parallel branch. The negative di/dv characteristic of the arc results in a resonant current with growing amplitude [9]. When its magnitude reaches that of the current into the circuit breaker a zero current instant is created in the interrupter and the arc extinguishes. Current then only flows through the parallel branch, charging the capacitor. Its voltage rise is limited by the MOSA, which dissipates the majority of the energy.

Resonant frequency of the parallel branch is typically in the range of 1-3 kHz. This scheme is often applied to Metallic Return Transfer Breaker (MRTB) which can clears the neutral current flowing through a neutral line of a HVDC transmission system, with current interrupting capability of up to 8 kA at present [9]. However, it is typical that 20-40

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milliseconds are required for the resonant circuit current magnitude to build up sufficiently, making the breaker too slow circuit breaker applications where fast disconnection is required.

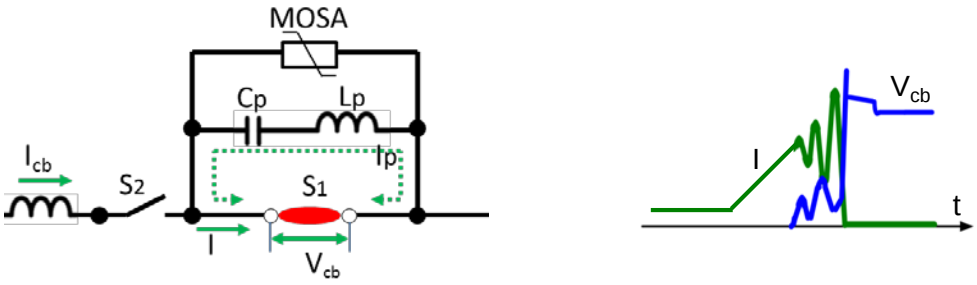

Figure 4.4: Mechanical dc breaker with passive resonant circuit

4.2.3 MECHANICAL CIRCUIT BREAKER WITH ACTIVE CURRENT INJECTION

The circuit topology is similar to that of the passive resonant scheme, except that the capacitor in the parallel branch is pre-charged (typically to dc line voltage, although this is not required). Upon triggering the circuit breaker, the interrupter is actuated and the switch in the resonant branch (high-speed mechanical switch) is closed. The superposition of the current into the dc breaker and the resonant current from the parallel branch results in a current zero through the interrupter, and the arc extinguishes.

Resonant frequency is typically much higher than the passive scheme (several kHz) and a current zero is created in a 1/4 or 3/4 of a cycle (depending on current direction). After a current zero is reached, all current is commutated to the resonant branch, charging the capacitor. Capacitor voltage is clamped by the MOSA, which dissipates the energy. In [11] a prototype breaker was shown to interrupt nominal and fault current (up to 16kA) within approximately 8-10 milliseconds, making it a viable HVDC circuit breaker. Vacuum interrupters, which have good high frequency interruption performance, are typically used as the main interruption device.

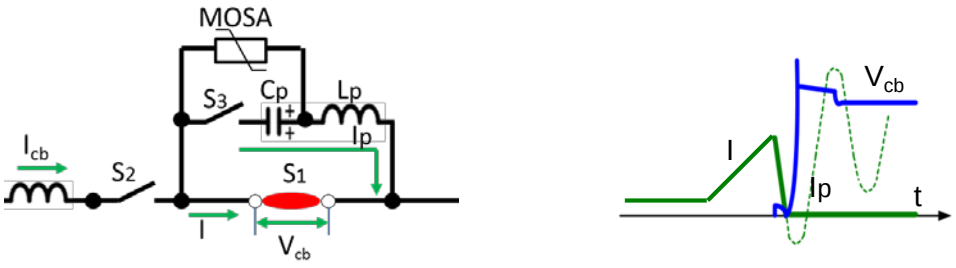

Figure 4.5: Mechanical circuit breaker with current injection

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5 MECHANICAL CIRCUIT BREAKER WITH ACTIVE CURRENT INJECTION

In this section, modelling of the mechanical circuit breaker with active current injection is described. The brief overview given in Section 4.2.3 is expanded to give a detailed description of the mechanisms by which the circuit breaker operates.

5.1 TOPOLOGY

The general structure of the mechanical HVDC circuit breaker with active current injection is given in Figure 5.1. The breaker consists of a high speed mechanical interrupter (S_1), a switched parallel resonant branch (L_p, C_p, S_3) with surge arrester and a Residual current circuit breaker (S_2). Resistor R_{ch} is used to maintain capacitor pre-charge voltage. Key components are listed in Table 5.1.

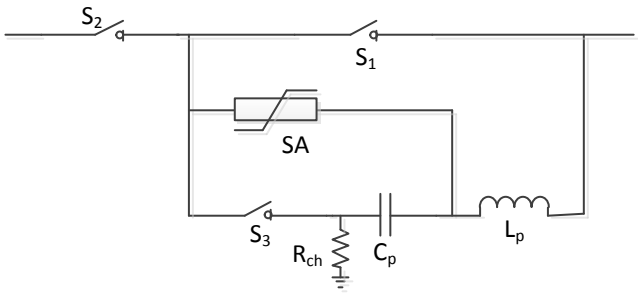

Figure 5.1: General topology of the mechanical dc breaker with current injection.

Table 5.1: Main components of the mechanical breaker with current injection

COMPONENT	NOTES
C_p	Parallel circuit capacitance
L_p	Parallel circuit inductance
R_{ch}	Charing resistor
SA	Surge arrester
S_1	High speed mechanical interrupter (vacuum interrupter)
S_2	Residual current circuit breaker
S_3	High speed switch

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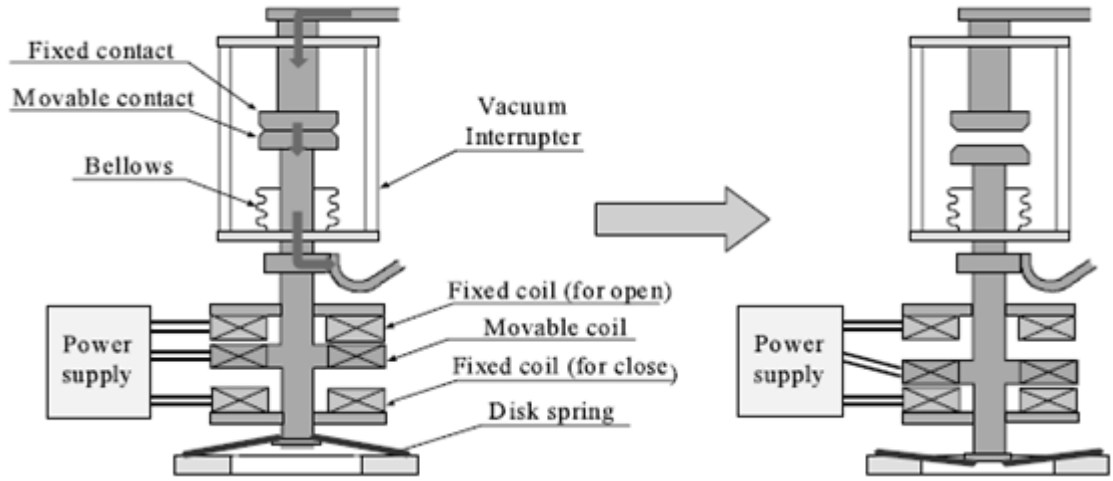
5.2 MECHANICAL CIRCUIT BREAKER COMPONENTS

In this section an overview of the key components of the mechanical dc breaker with active current injection are given.

5.2.1 HIGH SPEED INTERRUPTER WITH ELECTRO-MECHANICAL OPERATING MECHANISM

The main interrupter contacts (S_1) must separate a sufficient distance before voltage can be applied (to ensure adequate dielectric strength). Typically, standard ac interrupter units use a mechanical latch to hold them closed, and are driven apart by a coil spring when opened. This results in a relatively long operating time (in the order of 30ms). For dc breaker applications this results in a breaker operation speed which is, typically, unacceptable.

For mechanical dc breakers, a high-speed electro-mechanical actuator can be used to reduce the actuation time, as shown in Figure 5.2. This actuator topology does not have a mechanical latch, which reduces time delay. High speed operation of the interrupter contacts allows the resonant circuit to be operated faster, and the dc breaker to generate a counter-voltage in a shorter space of time. This configuration can allow the mechanical dc breaker to produce a counter voltage within approximately 8ms from the trip order being given.



(a) Closed position (b) Open position

Figure 5.2: High speed interrupter with electro-mechanical operating mechanism (Switch S_1)

5.2.2 CURRENT INJECTION CIRCUIT

The resonant circuit, when triggered by closing S_3, generates an oscillating current through the main interrupter (S_1). With sufficient magnitude, this causes a current zero to be generated in the interrupter.

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The circuit topology is shown again in Figure 5.3 for reference. The current in the interrupter (I_{VI}) is given by (3). The prospective current in the resonant circuit after S_3 is closed (that is, the current if the interrupter were to remain closed) is given by (4). The resonant circuit must generate a current pulse equal to the dc breaker current, as given by (5).

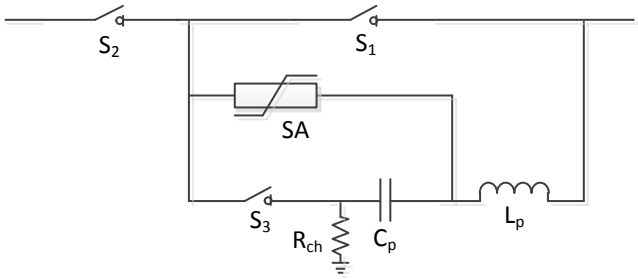

Figure 5.3: General topology of the mechanical dc breaker with current injection

$$I_{VI} = I_{CB} - I_p \quad (3)$$

$$I_p = V_{c(0)}\sqrt{\frac{C_p}{L_p}}\sin(\omega t) \quad (4)$$

$$V_{c(0)}\sqrt{\frac{C_p}{L_p}} \geq I_{CB} \quad (5)$$

$$\omega = \frac{1}{\sqrt{C_p L_p}} \quad (6)$$

The balance of frequency, current magnitude and component sizes must be traded-off against one another to optimise the circuit breaker functionally and cost. A higher frequency is desirable as it reduces the cost and volume of the components in the resonant circuit. However, it also places additional stress on the vacuum interrupter (VI) in the form of a higher di/dt. This can make it challenging for the VI to interrupt successfully upon a current zero.

Capacitance and inductance in the resonant circuit and pre-charge voltage affect the profile of the discharge current, in both magnitude and frequency. The capacitor voltage is maintained at line voltage by the charging resistor R_{ch}. In the model considered, the capacitor is pre-charged to the nominal line voltage, so the breaker is ready to operate immediately. As the charging voltage is fixed, the values of L_p and C_p must be adjusted to achieve the required current injection.

5.2.3 SURGE ARRESTER

The voltage generated across the DCCB is governed by the characteristic of the SA placed in parallel with capacitor C_p. When the circuit breaker commutates current from the resonant circuit into the SA, the voltage rapidly rises to a level determined by the SA characteristic. Typically, many SA elements are added in parallel to absorb the required energy, which influences the clamping voltage of the DCCB. Sample SA current-voltage

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characteristics are given in Table 10.1 of the appendix. These represent the aggregated I-V curve for a number of parallel columns used with a clamping voltage of approximately 1.5pu nominal dc voltage at 16kA, as shown in Figure 5.4.

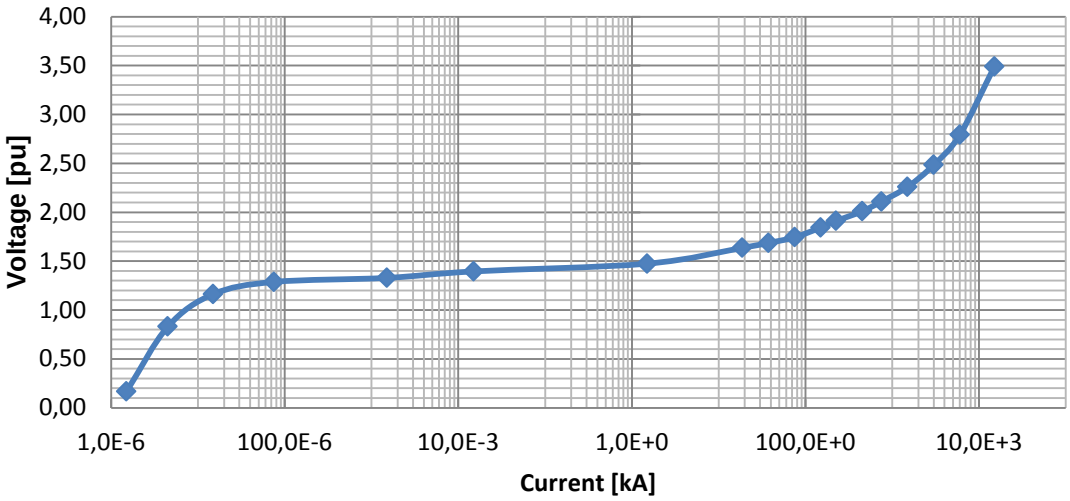

Figure 5.4: Aggregated SA current-voltage characteristics

5.2.4 RESIDUAL CURRENT CIRCUIT BREAKER

When current through the breaker falls below a lower threshold the surge arrester conducts only leakage current. This results in an oscillation between the system inductance and circuit breaker capacitance. The residual current circuit breaker (S_2) clears this when a current zero is created. For the purpose of modelling, a standard ac breaker with low chopping current can be used.

5.3 PRINCIPLES OF OPERATION AND TIME SEQUENCE

Representative time-domain current and voltage waveforms are given in Figure 5.5. The operation sequence of the breaker is given in Table 5.2. The opening sequence starts when the DCCB is in normal operation (interrupter S_1 and Residual current circuit breaker S_2 are closed, S_3 is open).

The circuit breaker is triggered by the protection relay. As the detection scheme is still under evaluation in WP4, a 2ms relay time has been assumed here. After the trip signal has been received,s switch S_1 begins to actuate. When it has reached a sufficient distance (to withstand the transient voltage applied during interruption) the resonant circuit injects a counter-current, by closing switch S_3. This generates a current zero within the interrupter (S_1) and all current now flows through the resonant branch, causing capacitor voltage to rise. When the clamping voltage of the SA is reached current through the circuit breaker

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begins to rapidly decrease. The total time from the trip signal being received to counter-voltage generation is approximately 8ms, which takes into account mechanical actuation and current commutation, etc.

Energy stored in the system is then dissipated in the SA. The time this takes is dependent on system conditions. When the dc breaker current passes through zero, the residual current circuit breaker S_2 becomes open circuit, providing galvanic isolation of the circuit breaker from the rest of the network.

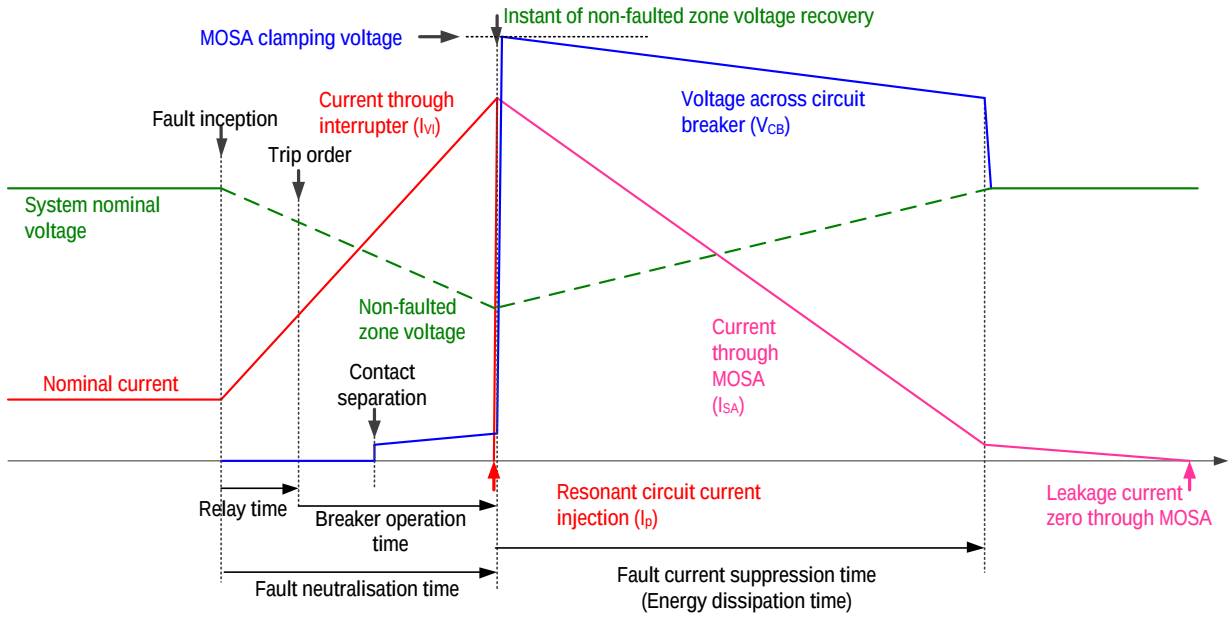

Figure 5.5: Current and voltage waveforms for the mechanical dc breaker with current injection

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Table 5.2: Interruption sequence of mechanical circuit breaker with current injection

Time	Definition and Operation	Default Value
Fault inception	Current and voltage wave fronts arrive at the circuit breaker location: • DC side voltage starts to decay and current increase.	0ms
Relay time	Time required for fault detection and discrimination: • Breaker receives trip signal sent from relay	2ms
Breaker operation time	Delays associated with physical movement of circuit breaker components. At the end of the period: • Switch S_1 has opened; • Switch S_3 has closed; • A current zero is generated in S_1 from the resonant circuit; • Capacitor voltage rises until the MOSA clamping voltage is reached. Current is then commutated into the MOSA; • Circuit breaker voltage (V_{CB}) is equal to clamping voltage	8ms
Fault neutralisation time	Combination of relay time and breaker operation time: • Breaker has been tripped; • Current zero and counter voltage generated.	10ms
Fault current suppression time	Time for stored magnetic energy to be dissipated in the MOSA: • The time is determined by the system configuration. For example, cable length, MOSA characteristic	-
Residual current circuit breaker open	Residual current circuit breaker (S2) opens • Current has reached leakage level (several mA), determined by the MOSA V-I characteristic; • Residual current is removed by S2	-

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6 SYSTEM LEVEL MODELLING

System level models must provide adequate representation of the circuit breakers for system analysis. They should produce external current-voltage characteristics of the circuit breaker that are representative of those seen from the practical devices. As such, internal characteristics and operation of the breakers is not required. Therefore, mechanical delays and maximum capabilities (such as peak current breaking capability) should be included but the level of detail should be minimal to avoid unnecessary complexity.

Detailed modelling of individual components requires more processing power – reducing simulation speed. This is particularly critical for simulation of the mechanical circuit breaker with active current injection. In this topology, the natural frequency of the resonant branch is high (in the order of several kHz). To accurately model the current in the resonant branch a very small time-step is required (in the order of several microseconds or less). This places a significant burden on the simulation platform and should be avoided, where possible.

In the following sub-sections, two options for mechanical dc breaker system level models are proposed and compared. The appropriate model can then be chosen based on the study requirements.

A prototype of the mechanical DC circuit breaker rated at 72kV will be used in WP5 and WP10 for testing in the high voltage laboratory. In protection system simulations (such as WP4, 5 and 9) system-level models rated at 320kV will be considered. As such, the models provided may be used for both applications. Table 10.2 in the appendix gives values of L_p, C_p and capacitor pre-charge for the two voltage levels considered.

6.1 MODEL DESCRIPTIONS

WP4 will assess a large number of protection cases – various system topologies, power flows, protection options, etc. To increase the number of cases investigated, simulation time of the breaker models should be reduced as much as possible. It is, therefore, desirable that the circuit breaker model does not reduce the performance of the larger system – i.e. the simulation time-step requirements of the breaker model should not be a constraint on the overall system performance, if possible.

To give flexibility, two levels of model complexity have been developed, as shown in Figure 6.1. Model 1 includes the resonant circuit; Model 2 does not. For reasons that will be explained in the following sections, this allows longer time-steps to be used, with marginal reduction in simulation accuracy.

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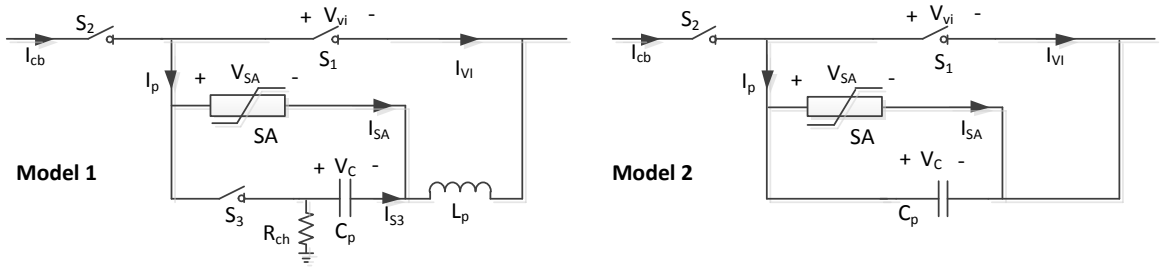

Figure 6.1: Methods of modelling mechanical circuit breaker for system level applications

6.1.1 MODEL IMPLEMENTATION

Each interrupter is modelled as an ideal switch, with a mechanical delay and chopping current. The main interrupter (S_1) begins in the closed state (①, as shown in Figure 6.2). After a trip signal is given, a mechanical delay is modelled and the switch interrupter transitions to state ②.The chopping current represents the minimum current through the interrupter for an arc to be sustained. Above this current, the interrupter switch model remains in the closed (low impedance) state ②. When current goes below the chopping current value, it transitions into a (high impedance) open state ③. Figure 6.2 demonstrates the state transitions involved in interrupter modelling.

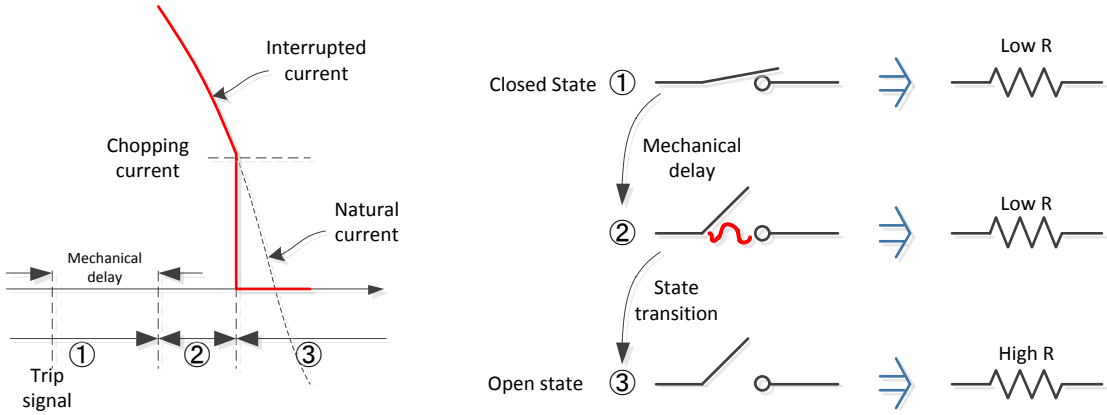

Figure 6.2: Interrupter state transitions (low impedance to high impedance), based on chopping current threshold

The key differences between the two circuit breaker models are given in Table 6.1. In a practical circuit breaker, switch S_1 becomes open circuit when the chopping current level, I_{S1_chp}, is reached (typically, this is in the order of several amps). In Model 1, a current zero is generated by the counter-current injection from the parallel circuit, at which point S_1 transitions from the conducting state to open circuit state. Model 2 does not include all elements to generate a current injection, and thus it does not naturally generate a current zero in S_1. To allow it to interrupt the current, the *chopping current level is set to the rated circuit breaker interruption capability*. In this way, provided the current through the breaker

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is at or below its rated capability, S_1 will transition from state ② to ③ immediately after the mechanical delay (following a trip order being given).

Table 6.1: Summary of key differences between Model 1 and 2 model implementation

	Model 1	Model 2
Chopping current of S_1	Several amps	Circuit breaker interruption capability
Initial charge of C_p	System voltage (320kV)	0kV
Parallel circuit inductance (L_p)	Included	Not included
Parallel circuit switch (S_3)	Included	Not included

6.1.2 CONTROL LOGIC

The models are designed to replicate the circuit breakers action after a trip signal has been sent. There are three main delays between a trip order being given and the circuit breaker producing a counter-voltage, which originate from the operation of mechanical switches S_1, S_2 and S_3. The control logic inside the circuit breaker model, shown in Figure 6.3, is used to replicate these delays. Default values for the delays are given in Table 6.2. As the model presented is for single open operation only, an S-R latch is used to ensure a fluctuating trip signal does not inadvertently cause multiple operations.

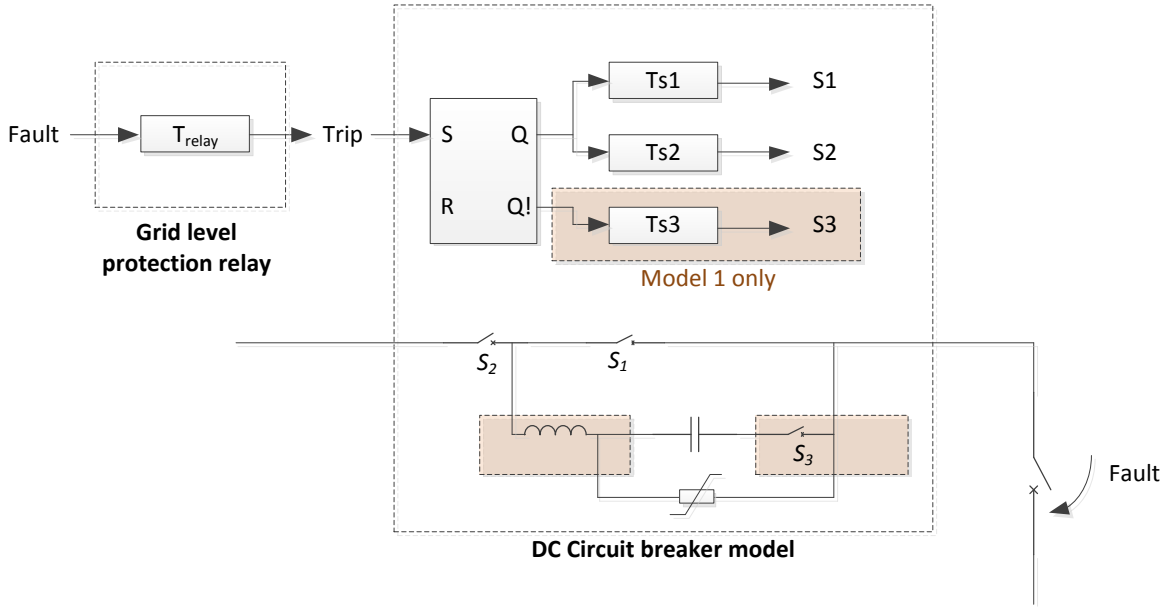

Figure 6.3: Circuit breaker model control logic block diagram

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Table 6.2: Values of the time parameters of mechanical circuit breaker with current injection

Time parameter	Definition	Default value
T_{relay}	Delay for receiving trip signal from protection relay	2ms
T_{S1}	Mechanical delay for switch S_1	8ms
T_{S2}	Mechanical delay for switch S_2	8ms
T_{S3}	Mechanical delay for switch S_3	8ms

6.1.3 APPLICATIONS OF MODELS

Model 1 is suitable to study the interrupter requirements – initial TIV, etc. Model 2 is suitable for system requirements simulations, as the key characteristics (clamping voltage, etc.) are represented. Using Model 1 requires a sampling time smaller than several microseconds (as in Section 7.3.1), due to the presence of the high frequency resonant circuit. This increases the simulation time for the overall system. However, Model 2 allows a significantly longer time-step to be used, allowing a greater number of protection studies to be performed. Accordingly, the DCCB model used should be chosen based on the goal of the studies performed.

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7 VALIDATION SIMULATIONS

The performance of the previously presented DCCB system-level models is discussed here. Model 2 is compared against Model 1 to calculate the error related to the reduced complexity of this model. The limitation of the two models as well as their robustness for different operation is then evaluated.

7.1 VALIDATION CIRCUIT

To demonstrate the dc breaker model operation, it is convenient to use a simplified validation circuit, such as that shown in Figure 7.1. Circuit parameters are given in Table 9 of the appendix.

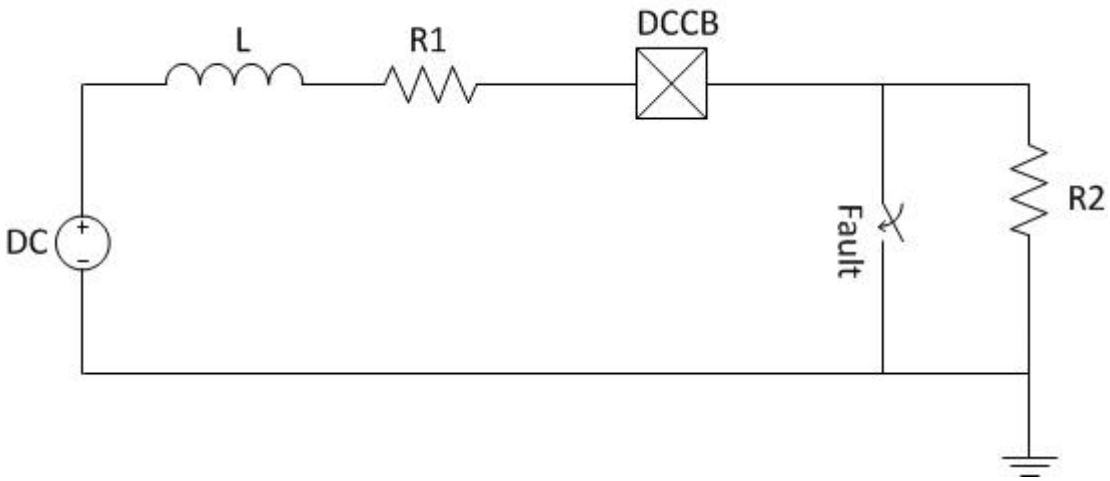

Figure 7.1: Circuit breaker model validation circuit

7.2 MODEL 1 AND MODEL 2 COMPARISON

Simulation results comparing Model 1 and Model 2 are shown in Figure 7.2. After the mechanical delay (T_{S1}) has passed, switch S_1 opens, as long as current is below I_{S1_chp}. In Model 1 I_{S1_chp} is set to a relatively small value (several amps) and S_1 only becomes open circuit after counter-current injection. In Model 2 I_{S1_chp} is equal to the circuit breaker interruption capability, and therefore opens immediately (providing current is smaller than the threshold). This results in S_1 transitioning to an open circuit state earlier in Model 2 than in Model 1. Due to this delay, current through the circuit breaker (I_{cb}) continues to increase in Model 1, resulting in a higher peak current through the surge arrester.

Peak voltage across the interrupter matches closely between the two models. When current is fully commutated from the main interrupter (S_1) into the parallel branch, S_1 becomes open circuit. At this point the residual voltage on the capacitor is applied across the S_1. The

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remaining capacitor voltage is related to the current magnitude interrupted (and circuit design). Model 2 does not replicate this initial TIV as the capacitor is not pre-charged. However, the duration of this error is short, as demonstrated in Section 7.3.2, and has a negligible impact on the system. In Table 7.1 the error introduced by Model 2 is given, for key measurements. As Model 2 does not replicate the initial TIV, error is not shown.

Table 7.1: Error introduced by Model 2 of key measurements

Quantity		Error
I_{cb}		0%
I_{vi}		0%
I_{sa}		<1%
TIV	Peak	<1%
	Initial	-
E_{sa}		1.5%

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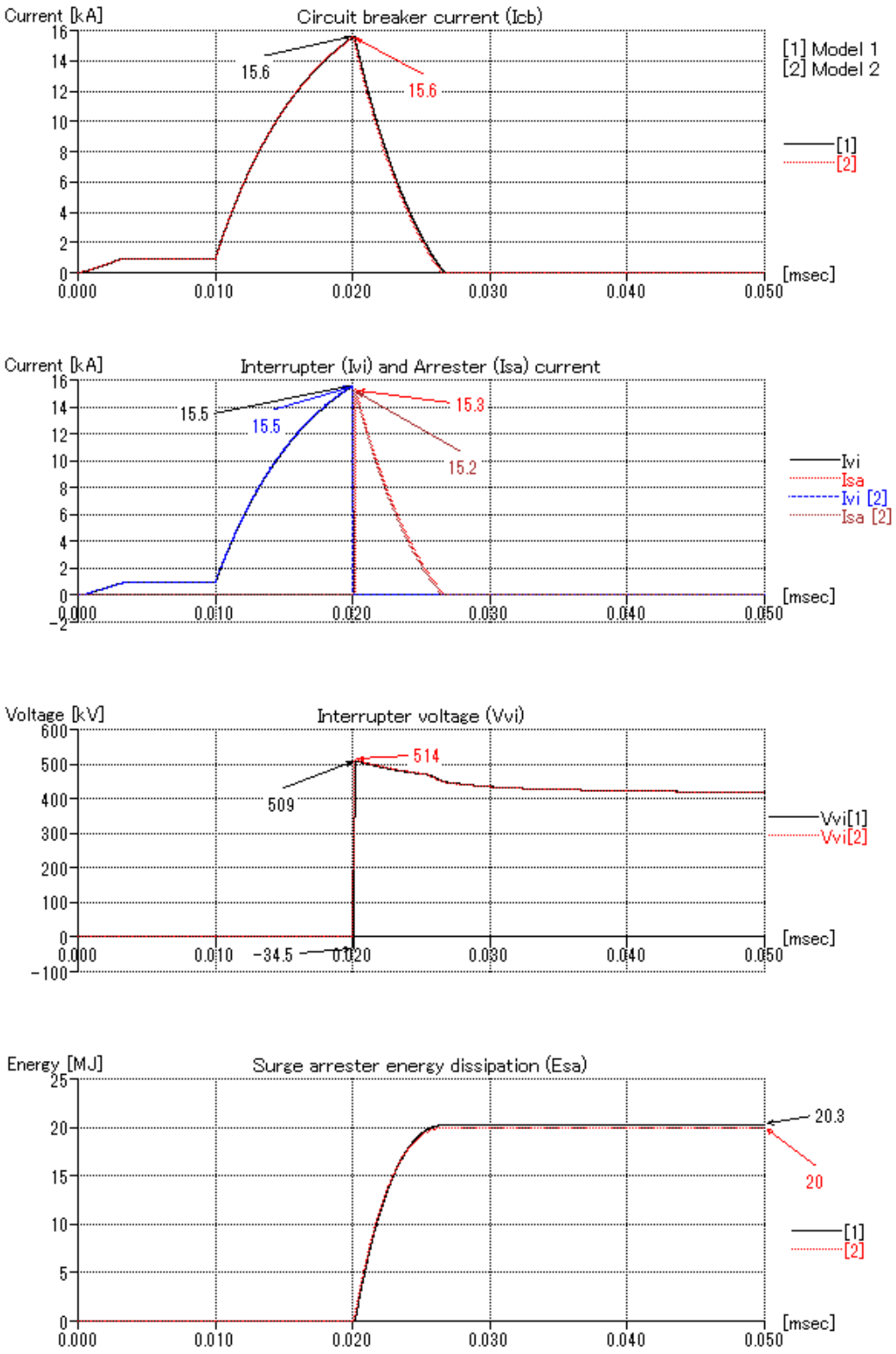

Figure 7.2: Comparison of Model 1 and Model 2 ; rated voltage - 320kV; parallel circuit resonant frequency - 3kHz; simulation times-step, 1us

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7.3 MODEL LIMITATIONS

Due to the fast transients within the circuit, Model 1 requires a very small time-step to be used, which can be challenging for large system studies. Model 2 does not replicate the initial TIV, which results in a small change in peak current and energy dissipation. The intrinsic limitations of each model, in particular the influence of time-step on simulation accuracy, are discussed in the following sections.

7.3.1 MODEL 1

Model 1 includes the oscillation circuit and is thus able to simulate current injection. However, the natural frequency of the parallel circuit is relatively high (in the order of several kilohertz, typically), which results in fast transients inside the circuit breaker. To accurately capture these, a small time-step must be used. Figure 7.3 shows the interrupter voltage (V_{vi}), for a range of simulation time-step values. The plot shown is a detailed view of the moment when current is fully commutated into the parallel branch, and S_1 becomes open circuit. At this point the residual capacitor voltage is applied to S_1. In the case simulated, with a time-step of 0.05µs (black trace) the initial TIV is accurately shown. Extending the time-step to 1µs (representing a 20 times increase in simulation speed) results in a loss of accuracy of approximately 10% loss. With a time-step of 10µs there is single data point during the initial transient, indicating that it's captured poorly. At 10 µs, 20µs and 40µs the solver is unable to represent the time instant the initial TIV occurs or its magnitude.

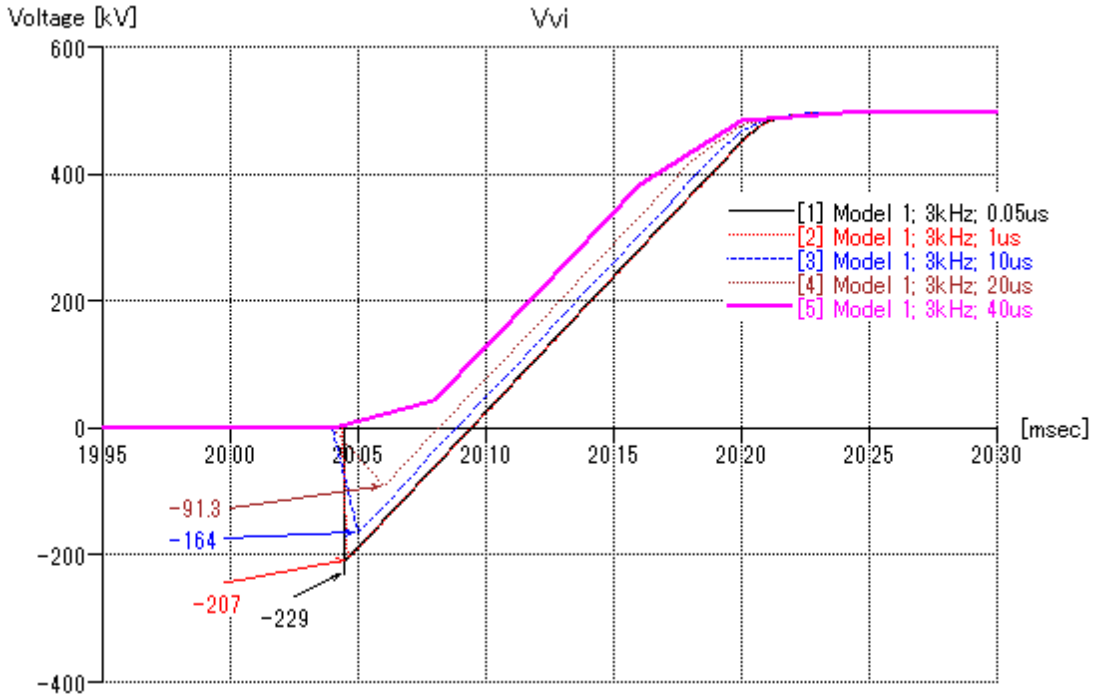

Figure 7.3: Influence of time-step on simulation accuracy of Model 1. Rated voltage: 320kV; parallel circuit resonant frequency: 3 kHz; simulation times-step: 0.05us → 40us.

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Accurately representing the initial TIV becomes more challenging if the natural frequency of the parallel circuit is higher. Figure 7.4 shows simulation results of the initial TIV across S_1, with a parallel circuit natural frequency of 8 kHz. With a time-step larger than 15µs the solver was unable to represent the current zero, and the circuit breaker did not operate successfully.

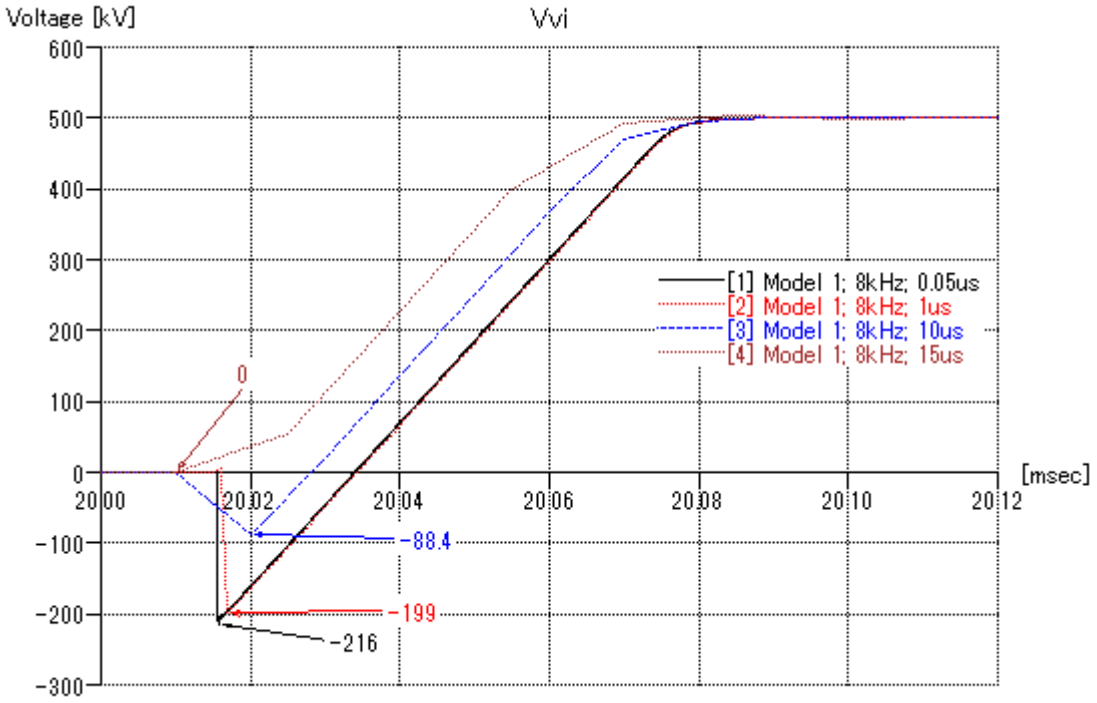

Figure 7.4: Influence of time-step on simulation accuracy of Model 1. Rated voltage: 320kV; parallel circuit resonant frequency: 8 kHz; simulation times-step: 0.05us → 15us.

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7.3.2 MODEL 2

In a practical circuit breaker, when the current zero is generated in the interrupter (S_1) the parallel capacitor is still partially charged, causing an initial TIV across (S_1). The magnitude of this voltage depends on the residual voltage on the capacitor at this instant. In Model 2, the capacitor is permanently in parallel with the surge arrester (switch S_3 is not modelled) and is not pre-charged. This causes two forms of error to be introduced, which are demonstrated in the simulation results given below.

Figure 7.5 shows measurements of interrupter current and voltage across the capacitor and main interrupter (S_1). The detailed view, shown on the right, highlights the difference between the two models. The first error is the lack of initial TIV produced by Model 2: as the capacitor is not pre-charged, negative voltage is not applied to S_1 at current zero. The second error is the capacitor voltage reaches the SA clamping level prematurely, when compared to Model 1.

In Model 2, the capacitor begins to charge from zero. However, in Model 1 the capacitor voltage must first increase from -320kV. This results in the capacitor reaching the clamping voltage earlier in Model 2 than Model 1. Subsequently there is a variation in peak current through the breaker and energy dissipated in the arrester (current through the circuit breaker continues to increase during this time in Model 1). However, as simulation results show the error introduced is small (in the order of 100µs).

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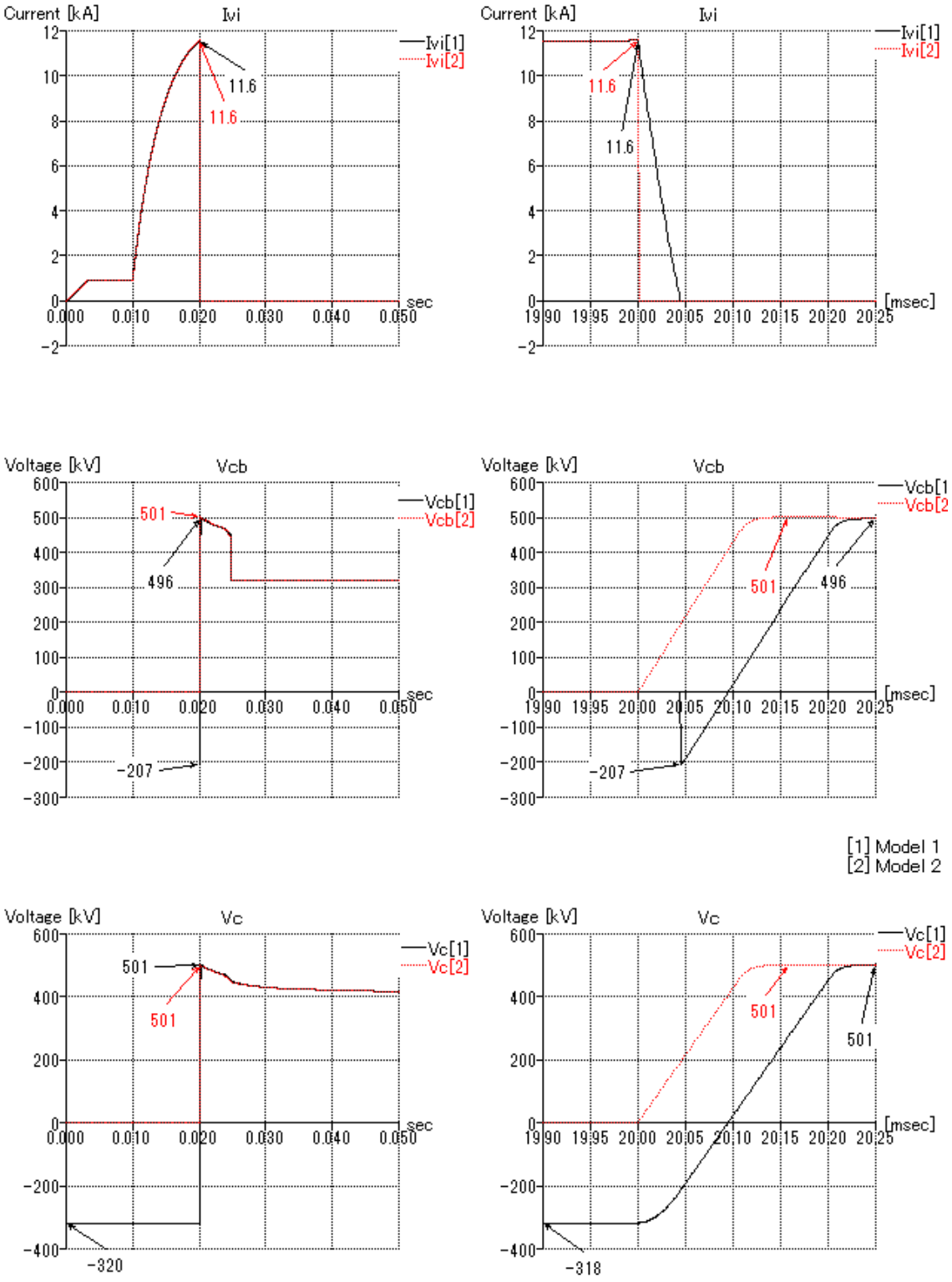

Figure 7.5: Comparison of initial TRV with Model 1 and Model 2. Rated voltage: 320kV; parallel circuit resonant frequency: 3 kHz; simulation times-step: 1us.

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7.4 SUMMARY OF MODEL TYPES

The impulse generated by the initial TIV is very short, when compared to the total TIV of the circuit breaker (in the order of several hundred microseconds, compared to several tens of milliseconds). Although this is a significant burden for the interrupter requirements, it has negligible impact on the HVDC system dynamics. As the system level model is designed for system studies, the reduction in accuracy should be acceptable for most cases. A summary comparing the two models is given in Table 7.2. It shows that, for the purposes of protection simulations, Model 2 can be used.

Table 7.2: Comparison of system level model capabilities

			MODEL 1	MODEL 2
DC Breaker Requirements	Peak current		✓	✓
	TIV	Peak	✓	✓
		Initial	✓	X
HVDC System Analysis	Peak current		✓	✓
	Peak voltage		✓	✓

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7.5 MODEL ROBUSTNESS

The models should replicate the real capability of the circuit breaker in a physical system. They should interrupt up to rated current, but no more. In this section both models are assessed in their interruption performance for rated current, as well as excessive currents.

7.5.1 SUCCESSFUL AND FAILED INTERRUPTION

The circuit shown in Figure **7.1** is used to validate the DCCB models. Resistance R1 is varied (as given in Table 10.4) to adjust the interrupting current and validate the possible range of operation of the circuit breaker. Figure 7.6 shows simulation results of Model 1 for successful and failed interruption. Figure 7.7 shows similar results for Model 2.

In the results given, Case 1 demonstrates a successful interruption, by setting interruption current to approximately 15.5kA (500A less than breaker capability). Case 2 breaker current is set to approximately 19.5kA (3500A greater than interruption capability, which results in failed interruption. The results are summarised in Table 7.3. It is demonstrated that during overcurrent (Case 2), Model 1 does not generate a current zero in the main interrupter and Model 2 does not transition into a high impedance state. As expected, both models do not interrupt current in Case 2, demonstrating that realistic performance is achieved.

Table 7.3: Description of validation results from succesful and unsucessful interruption with Model 1 and Model 2

Plot		16kA interruption (successful)	19kA interruption (unsuccessful)
Model 1	**(a)**	dc breaker current is forced to zero, 10ms after the fault is initiated	current continues to increase – circuit breaker does not interrupt
	(b)	upon current zero creation, voltage across the circuit breaker rapidly increases, forcing current to zero, and returns to nominal system voltage (determined by the supply) after interruption is complete	Circuit breaker does not produce counter-voltage - S1 stays in the low impedance state, as current zero is not generated (see (d)).
	(c)	Current injection is able to match I_{cb}. After current zero is created in S_1, current is clamped while capacitor is charged.	16kA current injected. This is not large enough to match I_{cb} and no current zero is created in S_1. Current resonances between L_p, C_p and S_1.
	(d)	a current zero is generated in the main interrupter (S_1)	Current through S_1 does not reach zero. Interrupter stays in low impedance state

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	Plot	16kA Interruption (successful)	19kA interruption (unsuccessful)
Model 2	**(a)**	Current interrupted 10ms after fault inception	Current continues to rise – dc breaker does not interrupt
	(b)	Current through S_1 (I_{vi}) is less than chopping current (rated breaking capability - 16kA). Thus, interrupter transitions from low impedance to high impedance state, and force commutates current out into the parallel branch.	Current through S_1 (I_{vi}) is greater than chopping current at when interrupter is in the open position. As such, it stays in a low impedance state and continues to conduct all current.
	(c)	Upon current zero creation in S_1 voltage rapidly rises across the dc circuit breaker, forcing current to zero successfully	No current zero is created in S_1. As current is not commutated into the arrester, no voltage is generated.

Case 2 demonstrated that for interruption current larger than the circuit breaker rating, the dc breaker fails to interrupt (for both models). For Model 1, this results in a resonant current, superimposed on the fault current, that circulates between the parallel path and main interrupter. This is not replicated in Model 2, since current injection is not included (for modelling simplification purposes). However, this current is contained within the circuit breaker itself, and has no effect on the external system. Therefore, it has no consequence for system level simulations and may be neglected.

In the case of failed interruption, back-up protection must be used – the next dc breaker further back in the HVDC network or breakers on the ac side, for example. When closed into a discharged line or fault, the mechanical breaker can withstand the large transient current this causes, due to its lack of semiconductor devices, and does not require self-protection.

7.5.2 RECLOSING

It is possible for the mechanical circuit breaker to perform multiple operations, for example using additional parallel current injection circuits. This allows reclosing operations to be performed in systems where reclosing operation is required. This feature will be investigated further in Deliverable 6.4.

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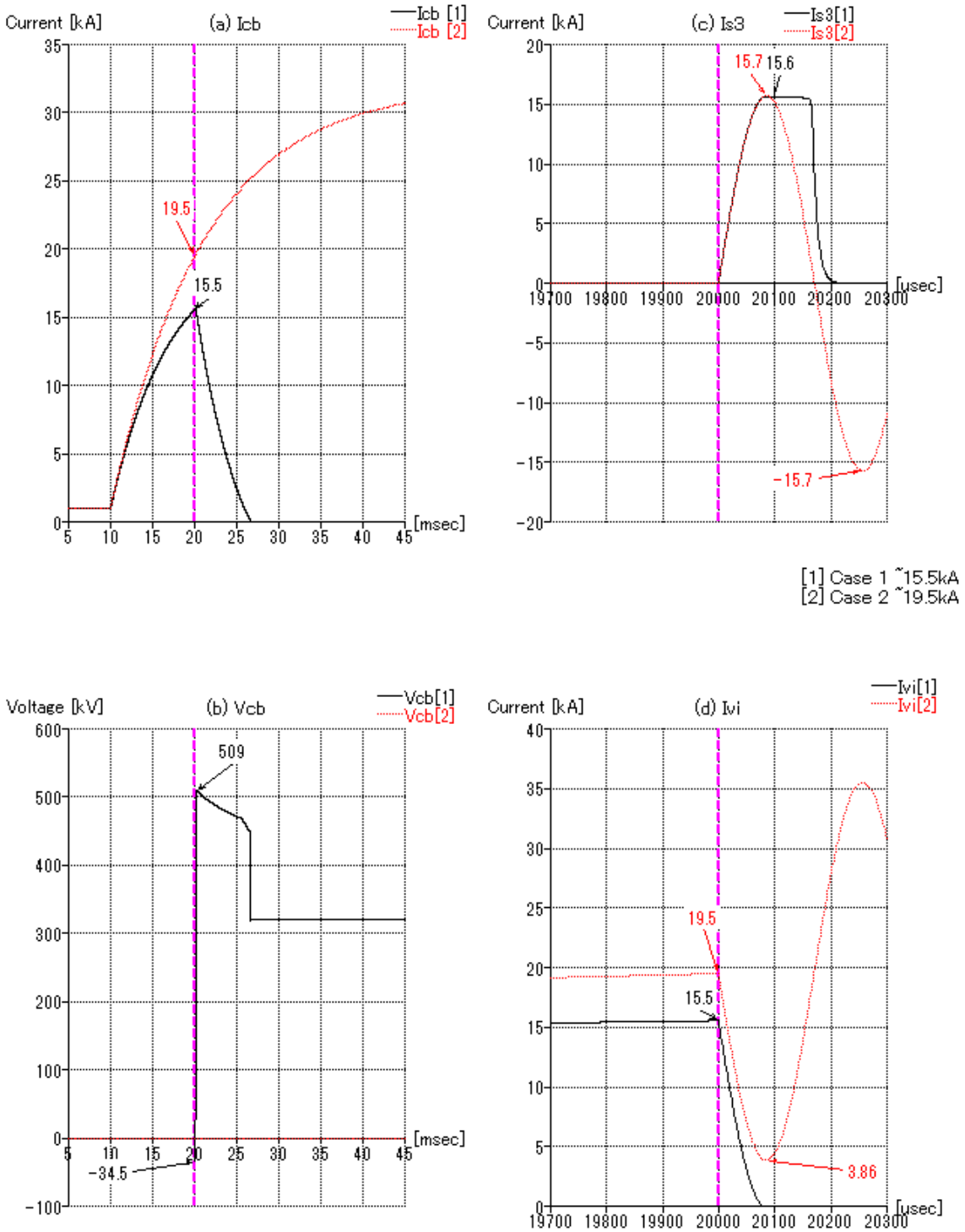

Figure 7.6: Model 1 validation. (a) dc breaker current; (b) dc breaker voltage; (c) current injection; (d) interrupter (S1) current. Case 1 = 15.5kA; Case 2 = 19.5kA

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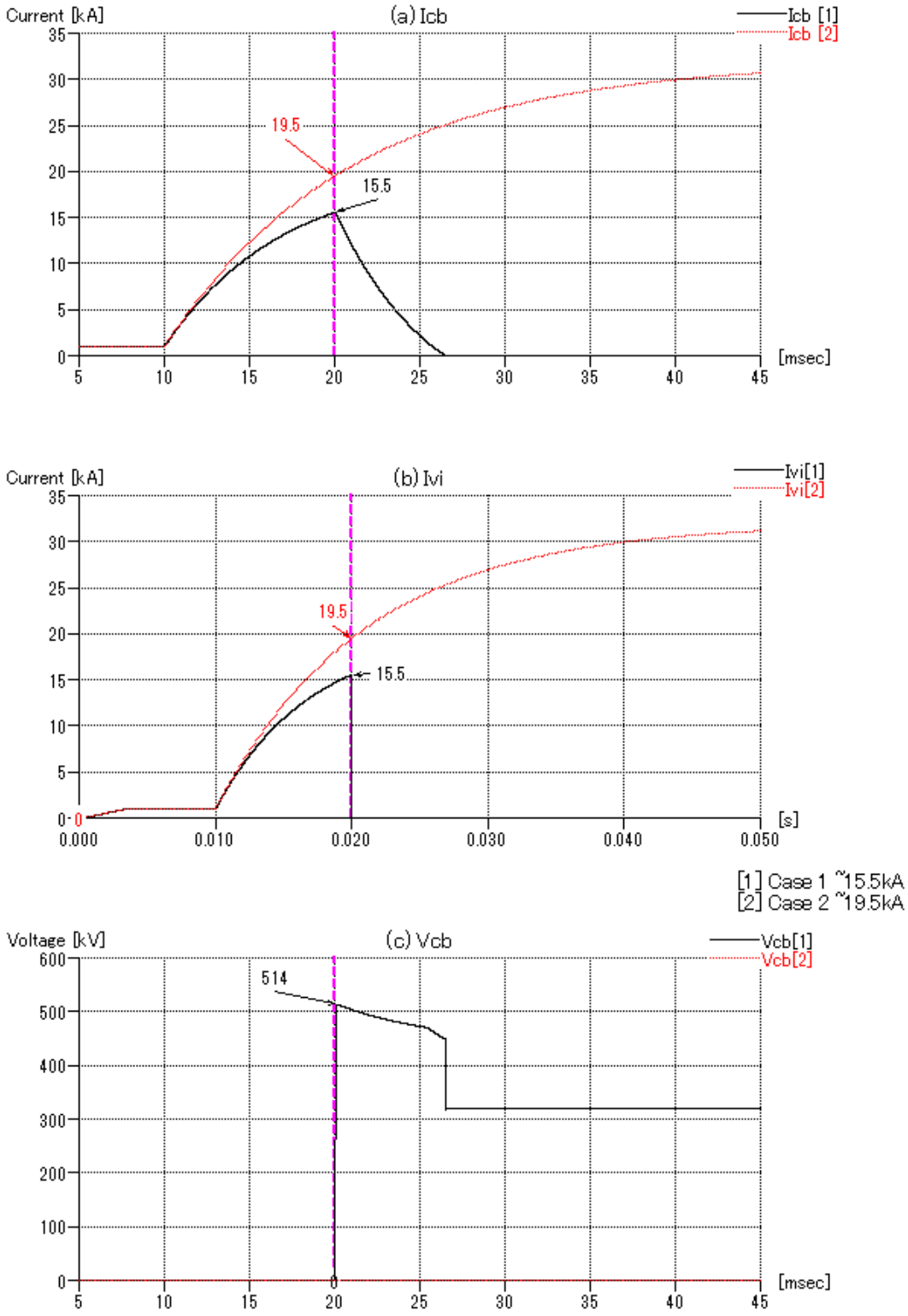

Figure 7.7: Model 2 Validation. (a) dc breaker current; (b) interrupter (S1) current (c) dc breaker voltage Case 1 = 15.5kA; Case 2 = 19.5kA.

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8 CONCLUSION

Two approaches have been proposed to model the mechanical circuit breaker with current injection, for system level studies. In Model 1 the characteristics of the parallel current injection circuit were considered and in Model 2 they were not. Both models were implemented in PSCAD and test simulations performed to investigate applicability for system level studies.

Results showed that to accurately replicate fast transients, Model 1 requires a very small time-step (less than 1 µs). This may be challenging to implement on RTDS hardware, which will be used in WP 9, where the smallest time-step available is in the range of 3-5µs, due to hardware constrains. Although feasible with off-line simulation tools, such as PSCAD, the small time-step represents a barrier to studies of large systems (multi-terminal HVDC networks, for example). It was shown that Model 2 resulted in a marginal loss in accuracy, from a system perspective. The proposed DCCB models have been shown to be robust in a number of case studies (opening from relay trip signal, failed interruption through overcurrent, etc). The choice of model used (Model 1 or Model 2) can be selected based on the study undertaken.

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10 APPENDIX

10.1 APPENDIX A: CIRCUIT BREAKER PARAMETERS

Table 10.1: Surge arrester data

Current [kA]	Voltage [pu]	Current [kA]	Voltage [pu]
1.5E-6	0.17	75.0E+0	1.74
4.5E-6	0.83	150.0E+0	1.84
15.0E-6	1.16	225.0E+0	1.91
75.0E-6	1.29	450.0E+0	2.01
1.5E-3	1.33	750.0E+0	2.11
15.0E-3	1.40	1.5E+3	2.26
1.5E+0	1.47	3.0E+3	2.48
18.8E+0	1.64	6.0E+3	2.79
37.5E+0	1.69	15.0E+3	3.49

Table 10.2: Circuit breaker parameters

Parameter		**Module**	**Full Breaker**
Nominal Voltage	[kV]	72	320
Rated Breaking Current	[kA]	16	16
Pre-charge Voltage	[kA]	72	320
Resonant frequency (f_0)	[kHz]	3	3
Capacitor (C_p)	[uF]	11	2.7
Inductance (L_p)	[uH]	238	1.1

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

10.2 APPENDIX B: VALIDATION CIRCUIT PARAMETERS

10.2.1 TEST CIRCUIT: REQUIREMENTS FROM HVDC NETWORK

Circuit breaker requirements can be assessed by simulation. Figure 10.1 shows a radial multi-terminal network that has been used to evaluate the current and voltage stress that a mechanical dc breaker must withstand. Sample simulation results are shown in Figure 10.2. System parameters used in the test system are given Table 10.3. The simulation model used included detailed modelling of converter stations to ensure accurate representation of the fault current stress imposed on the circuit breaker. In the simulation results, a peak current of approximately 16kA is reached 10ms after the fault occurs, at which point the breaker is opened in the simulation.

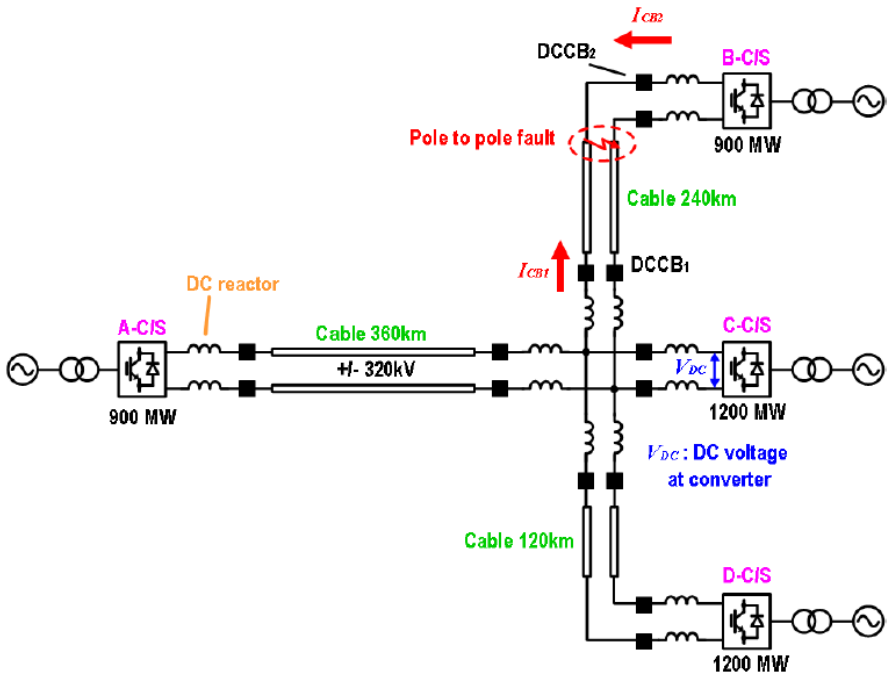

Figure 10.1: Radial multi-terminal network used to assess circuit breaker stresses

Table 10.3: Radial multi-terminal simulation model parameters

Parameter	A-C/S	B-C/S	C-C/S	D-C/S
DC voltage	+/-320 kV	+/-320 kV	+/-320 kV	+/-320 kV
Converter capacity	900 MVA	900 MVA	1200 MVA	1200 MVA
AC network voltage	400 kV	400 kV	400 kV	400 kV
AC network capacity	20000 MVA	8000 MVA	15000 MVA	15000 MVA
Transformer primary voltage	400 kV	400 kV	400 kV	400 kV
Transformer secondary voltage	320 kV	320 kV	320 kV	320 kV
Transformer leakage reactance	20%	20%	20%	20%
MMC arm inductance	10%	10%	10%	10%

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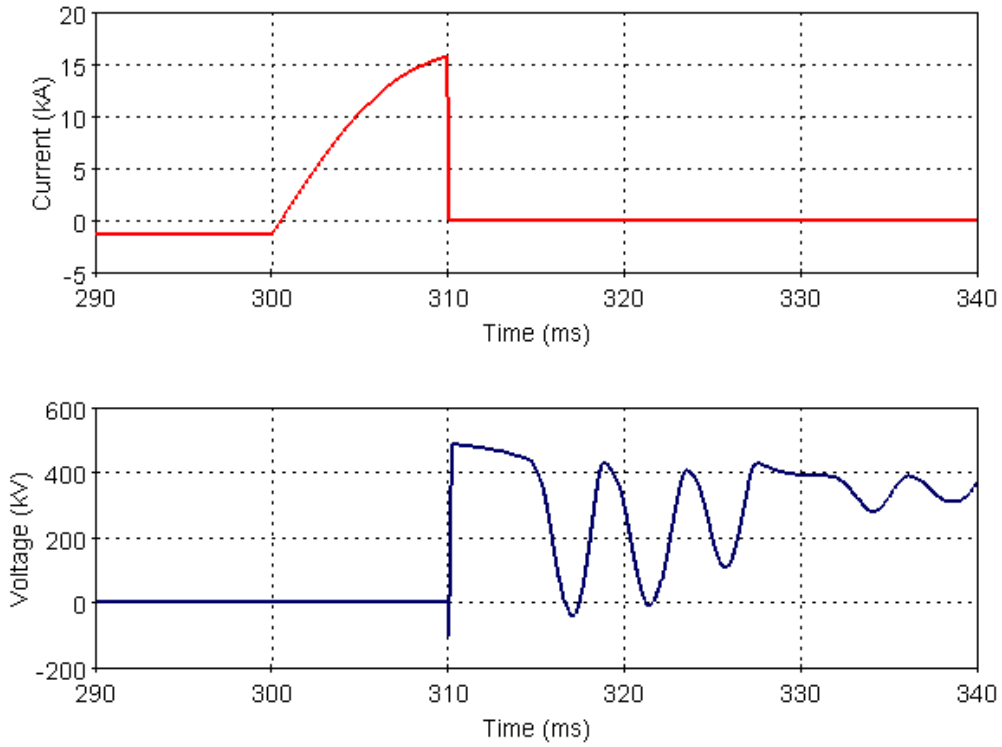

Figure 10.2: Simulation results of mechanical circuit breaker with current injection system in a multi-terminal HVDC network [1]

10.2.2 VALIDATION CIRCUIT PARAMETERS

Table 10.4 Test circuit parameters

Parameter		Full Breaker	Notes
Source voltage	[kV]	320	
R1	[Ω]	10	Interruption current ≈ 19.5kA
		16	Interruption current ≈ 15.5kA
		25	Interruption current ≈ 11.5kA
R2	[Ω]	320	
L	[mH]	110	

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