PROJECT REPORT

PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

Deliverable 6.5 – Low Voltage Hardware Demonstrators of DC CBs

PROMOTioN – Progress on Meshed HVDC Offshore Transmission Networks

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LIST OF CONTRIBUTORS

Work Package and deliverable involve a large number of partners and contributors. The names of the partners, who contributed to the present deliverable, are presented in the following table.

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CONTENT

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SUMMARY

This report presents the results of task 6.5 of the work package WP6 “Develop kW-size hardware models for hybrid and mechanical DC CB”. The main objective of this task is developing DCCB test circuit and kW size (900V and 500A) IGBT hybrid and mechanical DC CB.

A test circuit suitable for testing the DC CB’s is designed and built in the laboratory. The test circuit uses a large capacitor bank to store energy and release this energy during the fault. This results in the limitation of the grid current during the fault so that the local grid is not disturbed by large fault currents. The test circuit is capable of supplying 1000V and a peak fault current 1000A.

A 900V, 500A unidirectional IGBT based hybrid DC CB topology is designed and fabricated in the laboratory. This will imply the peak transient voltage of around 1500V which is the current limit in the laboratory. An ultra-fast disconnector (UFD) is designed and fabricated in house and placed in the DC CB. The main breaker branch consists of eight IGBT’s with suitably rated arresters across each. Experimental results show that the fabricated hybrid DC CB is capable of breaking a fault current of 500A.

A 900V, 500A mechanical DC CB is designed and built. The main breaker in the mechanical DC CB consists of three series connected (900V, 500A) contactors with grading resistors. The resonance circuit design is presented and components selected for required performance. It is decided to use a set of back to back thyristors (switch S3) for closing the resonant circuit. A contactor is used as the residual switch. The mechanical DC CB is tested and the results show that the DC CB is able to open under a fault current of 500A in positive or negative direction as well as low fault current of around 30A.

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ABBREVIATIONS

Abbreviation	Explanation
AC	Alternating Current
ADC	Analog to Digital Converter
CB	Circuit Breaker
DC	Direct Current
DC CB	Direct Current Circuit Breaker
DCL / DCR	DC Current Limiting Reactor
DSP	Digital Signal Processor
EMB	Electromagnetic Braking
FO	Fibre Optic
HDC CB	Hybrid Direct Current Circuit Breaker
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
PCB	Printed Circuit Board
PI	Proportional Integrator
PWM	Pulse Width Modulation
RCB	Residual Current Breaker
RTDS	Real Time Digital Simulator
UFD	Ultrafast disconnector
VSC	Voltage Sourced Converter
WP	Work Package

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1 INTRODUCTION

1.1 BACKGROUND

The use of high-voltage direct current (HVDC) transmission has been increasing because of many changes in power industry like the use of remote renewable sources, increasing the need for interconnections and increasing use of cable systems. There have been significant advances in HVDC technologies which have increased performance but reduced losses, costs and harmonics [1]-[3].

The DC grid is a very promising concept where multiple HVDC are required, however, many challenges need to be addressed before a complete DC grid can be realized. Until recently, one of the most important challenges was the protection of the DC grid [2]-[4]. In the last 5 years, several manufacturers have announced high-voltage DC Circuit Breaker prototypes and some are commercially available [5]-[8]. These devices have very fast operating time and minimal on-state losses, at the expense of high complexity and use of a combination of technologies (mechanical switchgear, high voltage electronic valves and surge arresters).

This task 6.5 runs in parallel with DC CB modelling tasks in PROMOTioN project where hybrid [9] and mechanical DCCB models are developed [10] [11], and they will be utilised in this task.

Task 6.3 substantially utilises results from this task and many new concepts studied in task 6.3 are verified on hardware. As an example, the new UFD voltage control which substantially improves operating speed of hybrid DC CBs [12], has been tested on hybrid DCCB demonstrator presented further in this report.

The forthcoming task 6.6 will utilise these hardware components from task 6.5 to perform further DC CB studies.

Work package 10 of the PROMOTioN project performs the testing of full scale DC Circuit Breakers, which will provide most accurate testing results. However, such testing is very restrictive in terms of scope and depth of studies, because of IP issues with vendors' DC CBs, because of the complexity of testing full-scale units, and costs associated with each test in particular with destructive tests.

1.2 MOTIVATION

The purpose of task 6.5 is to develop small-scale hardware prototypes for mechanical and hybrid DC CBs which will be used later in Task 6.6 for testing and analysis. The benefit of small scale hardware is in flexibility and costs. Many tests can be performed in short time and destructive tests will be possible, as it will be analysed later in Task 6.6.

The main research questions that will be addressed with small-scale prototypes are:

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1. Demonstration of technical feasibility of implementing complete DC circuit breakers, including all auxiliaries and control systems. The design, assembly and testing will reveal the level of challenge/complexity of each subsystem and it will reveal if new/advanced technologies/processes will be required to manufacture DC CBs. This aspect can not be addressed with simulation models.

2. The impact and importance of parasitic parameters in electrical circuits and friction components in mechanical systems. This is particularly important aspect since simulation models are always idealised to some degree.

3. Understanding of interdependence between subsystems in multiple engineering domains and magnitude of interaction variables. Since DC CBs involve electrical, mechanical and thermal processes it is very difficult to model such system on a single simulation model.

4. Understanding interactions in multiple time domains. The operation of power electronics will crucially depend on phenomena in *ns* range, many electrical systems in DC CBs operate in µs range, the mechanical systems dynamics will have time constants in ms range, while thermal processes may respond in seconds or longer. Such a wide range of dynamics is difficult for study and impossible on a single simulation model.

5. Understanding failure modes at component and system level. The modelling of component failure is particularly difficult and hardware experiments will offer particularly useful conclusions on model developments and impact between components.

It is understood that laboratory hardware demonstrators will not behave the same way as full scale DC Circuit Breakers. The ratings of demonstrators in this task will be limited by the University laboratory capabilities and the cost effectiveness of demonstrators. However, during the design, building and testing, all the effort will be placed in developing demonstrator that represents the actual system as accurately as possible. Various limitations of the scaled hardware will be indicated at a specific design and testing sections.

Most of the above research questions 1-5 can be addressed to some degree with the DC CB hardware demonstrators in the range of 1kV and 500A, assuming that topologies resemble full scale topologies. This range of ratings is suitable for University laboratory and costs will be reasonable. The key components will have properties which do not significantly differ from those in full scale DCCBs. As an example, 1.8 kV, 600A IGBT will be used in the demonstrator, which has ratings not far from those in hybrid DC CBs which are commonly 3.3kV-4.5kV, 2kA. Some other components (like vacuum interrupters) will be crucially different and this will be discussed.

A low power DC CB demonstrator is not able to accurately represent all the phenomena occurring in high-power DC CBs. The key differences and limitations of low power demonstrator will be explained in various places in this report when the particular subunit is introduced and responses analysed.

This Task 6.5 consists of three subtasks as:

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1. Test circuit design and implementation.
2. Hybrid DC CB prototype design and implementation.
3. Mechanical DC CB prototype design and implementation.

The test circuit is used for testing the fabricated DC CB's. Each subtask has to fulfil some requirements which are presented in next subsections.

1.3 TEST CIRCUIT DESIGN AND IMPLEMENTATION

The design considers capabilities of the power supply at University of Aberdeen laboratory (around 50 kW at 415 V). The test circuit facilitates testing of all important aspects of DC CB similarly as in WP5, but at lower power levels. The design aims are:

- Current interruption in the range of 500A,
- Voltage control to the level of 900V-1000V to facilitate dielectric tests.
- Energy absorption of around 300-2000J should be facilitated.
- Testing thermal stability of energy absorbers assembled using surge arresters.
- The design must be fail safe, considering that DC CB may fail to open.

The design will be coordinated with WP5 in order to complement studies in WP5 and WP10.

1.4 HYBRID DC CB PROTOTYPE DESIGN AND IMPLEMENTATION

The testing of full scale high-voltage DC CBs in WP10 is restricted since CB cannot be exposed to destructive testing or to internal failure mode demonstration. These tests are also costly, the number of tests and flexibility is very limited. The ability to probe into subcomponent level is also restricted because of IP issues.

A low power prototype of hybrid DC CB is developed in the laboratory in order to complement full scale testing. Some of the important considerations include:

- The topology should closely represent high power hybrid DC CB.
- Current interruption is in the range of 500A,
- Rated voltage of the order of 900V-1000V.
- Energy absorption of around 300-1000J.
- The main valve should have series connection of multiple semiconductors.

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- The ultra-fast disconnector should be developed to closely resemble actual topology and made to operate within 2ms.

1.5 MECHANICAL DC CB PROTOTYPE DESIGN AND IMPLEMENTATION

A low power prototype of mechanical DC CB will be developed in the laboratory to facilitate a range of tests.

Some of the important considerations include:

- The topology should closely represent high power mechanical DC CB.
- Current interruption in the range of 500A.
- Rated voltage of the order of 900V-1000V.
- Energy absorption of around 1000-2000J (because of longer operating time).
- Standard commercial circuit breaker units will be adopted for the main switches.
- The operation of the main switch should be made within 5-10ms, considering commercially available units. Vacuum interrupters are not available in the voltage range of 1kV and their cost is prohibitive for the project. Therefore air switches will be considered

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2 TEST CIRCUIT DESIGN AND IMPLEMENTATION

2.1 INTRODUCTION

As DC Circuit Breakers become acceptable technology, an important challenge is hardware testing the DC CB in order to confirm the working in real conditions. Different DC CB testing configurations have been proposed in literature. In [5] charged capacitors, which have enough energy to inject the required peak current, are used. In [6] two different frequencies are used to generate the nominal voltage and the peak current. A current source is used in [7] for testing DC CB. The authors of [8] propose a method which uses a 50Hz sinewave and the authors in [14] use 16.7Hz sine wave to stress the DC CB.

The test circuit should contain significant energy storage with fast discharge capability, since high energy pulses cannot be drawn directly from the grid without dangerously approaching safety margins for tripping thresholds. The nature and shape of peak current stress and dielectric stress on DC CB should correspond to the conditions in the actual DC grid. A challenge with capacitive energy storage is that voltage reduces as the energy is released and this implies incorrect (lower) dielectric stress on the DC CB. Because of requirements for DC CB re-closure and repeated operations within 200-500ms cycle, the test circuit should be capable of fast recharging.

2.2 CIRCUIT TOPOLOGY

This section presents design of a 900V-500A test circuit for testing DCCBs. It details all the design of converter, energy storage, component parts and controller used in the test circuit. The initial DC CB test circuit topology is presented in [13], but further improvements have been made subsequently.

The test circuit topology is shown in Figure 2.1. This is an AC-DC power converter with a charge controllable capacitor bank. This means, it is possible to control the charging of the capacitor bank. The advantage of this circuit is, once the fault current is reduced to zero by DC CB, the dc voltage can be quickly increased to the nominal value, assuming interruption within 2-10ms. This is possible because we can turn OFF the capacitor bank switch T_2 so that the capacitor bank is not charged (this would take long time because of size of C_s). This is important if the test needs to replicate the stresses of the DC CB in future DC grids.

The DC input voltage V_d is around 1174V. This voltage is obtained by series connection of two rectifies on the secondary windings of the transformer XFMR. The secondary windings are star/delta hence the series connection will block flow of any fifth and seventh harmonics and its multiples. Third harmonic is naturally eliminated in a symmetrical and balanced 3-phase system. A capacitor Cd is connected across the DBR for smoothing out ripples and reduces the effect of stray inductances.

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The chopper (T_1) regulates the output voltage V_{dc} to 900V in normal condition. For testing the CB, the chopper charges the capacitor to a higher level of 10% (990V) in order to reduce size of storage capacitance. For the duration of the fault and while DC CB is in the process of opening, DC voltage will drop. As soon as the fault is cleared, the chopper reference changes to keep the V_{dc} voltage at 900V. During this period the T_2 is turned OFF so that the dc voltage reaches 900V very fast in order to provide adequate voltage stress across test object. Capacitor C_{dc} and resistor R_{dc} help to keep DC terminal voltage stable. The charging of storage capacitor Cs is delayed by a short period until fault is cleared.

The fault is generated by closing the fault switch T_f. The fault switch is a thyristor and only needs to make the short circuit and need not break fault current. It is controlled by giving a pulse to the thyristor gate driver.

All the parts of the test circuit are explained in the next sub sections. The chopper operates at switching frequency of 10kHz. The filter inductor is selected such that the ripple current is not excessive. An inductor of 3mH results in worst case peak ripple current of about 20A.

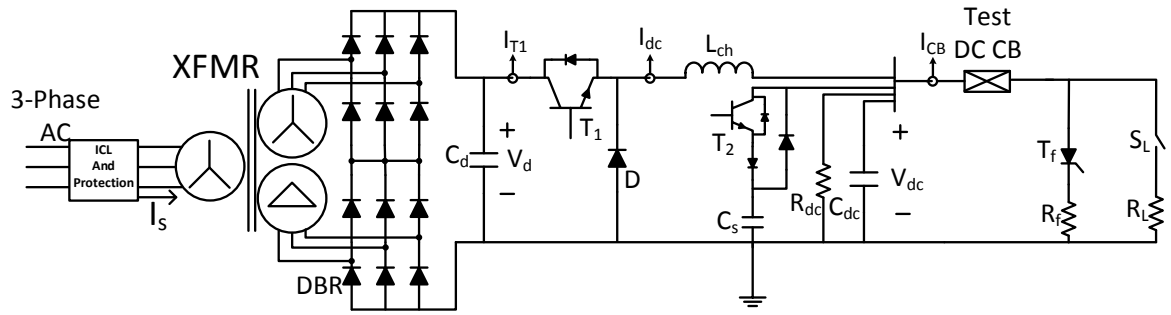

Figure 2.1 The circuit configuration of the DC CB test circuit.

2.3 CAPACITOR BANK CALCULATION:

When a fault is applied to the circuit the capacitor bank C_s voltage drops from V_{cs1} to V_{cs2}. During the discharge of the capacitor bank C_s, the energy released is:

$$E_s = C_s \frac{V_{cs1}^2 - V_{cs2}^2}{2} \qquad (0)$$

There is clearly a trade-off between voltage deviation and the capacitor size. To avoid very low final DC voltage and large capacitor, it is proposed to increase the initial test voltage. Assuming that the nominal voltage is V_{dcn}, the initial and final DC voltages can be expressed as:

$$V_{cs1} = V_{dcn} + \Delta V_{dc}; \quad V_{cs2} = V_{dcn} - \Delta V_{dc}; \qquad (0)$$

where ΔVdc is the allowed voltage deviation. Substituting (0) into (0) results in:

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$$E_s = 2\, C_s V_{dcn}\, \Delta V_{dc} \tag{0}$$

The required energy release (E_s) can be determined from simulation tests with an infinite DC bus which represents ideal test circuit. Then, knowing E_s, (0) can be used to evaluate required storage size for assumed allowed DC voltage deviation (ΔV_{dc}) during the discharge test. For the test system Es=600J, and with V_{dcn}=900V, ΔV_{dc}=50V the capacitor bank is calculated to be 6.66mF. A capacitor bank of 7mF is selected for the test circuit.

2.4 LOAD BANK CALCULATION:

The rating current of the test circuit is 30A. If the output voltage of 1000V is considered for the test circuit the required load is:

$$R_L = \frac{V_{dc}}{I_{dc}} = \frac{1000}{30} = 33.33\Omega \tag{0}$$

Twelve 47Ω, 2kW resistors (3 in series x 4 in parallel) are used to make a load bank of 35Ω.

2.5 TEST CIRCUIT OPERATION AND REFERENCE VOLTAGE SELECTION

The initial photograph of fabricated test circuit is shown in Figure 2.2. The arrangement of components may change before the destructive tests are attempted. The list of components is shown in Table V in the Appendix

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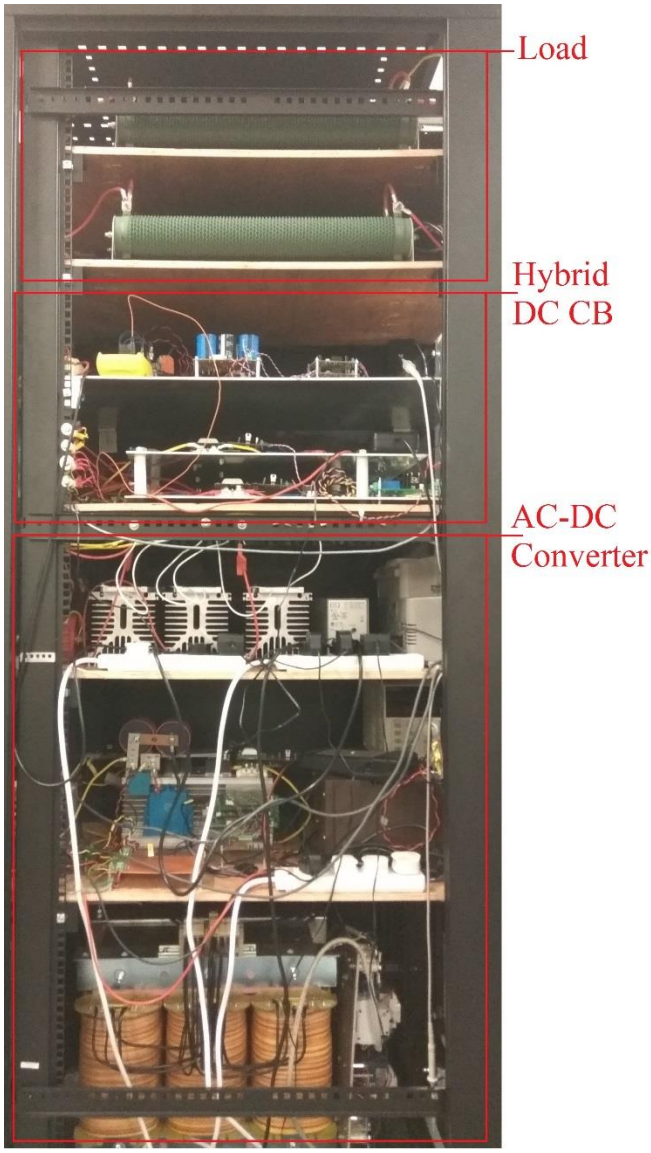

Figure 2.2 Fabricated test circuit.

When the test circuit is turned ON the chopper regulates the dc output voltage (V_{dc}) to V_{dcref1}. The V_{dc} remains the same until the fault is detected at time t_f. The fault detection is done by comparing the CB current (I_{CB}) with a threshold current (I_{TH}), if the I_{CB} is higher than the I_{TH} then the fault is detected. During this period (0-t_f) the IGBT T_2 is ON and the reference voltage is V_{dcref} =V_{dcref1}=1035V. V_{dcref1} can be set from control panel using a potentiometer. After the detection of the fault the IGBT T_2 is switched OFF and the reference voltage is changed to V_{dcref} =V_{dcref2}=900V. This ensures that V_{dc} is elevated rapidly (before Cs is charged) to provide adequate voltage stress across DCCB at the instant of current interruption. The operational sequence of the test circuit is shown in Figure 2.3.

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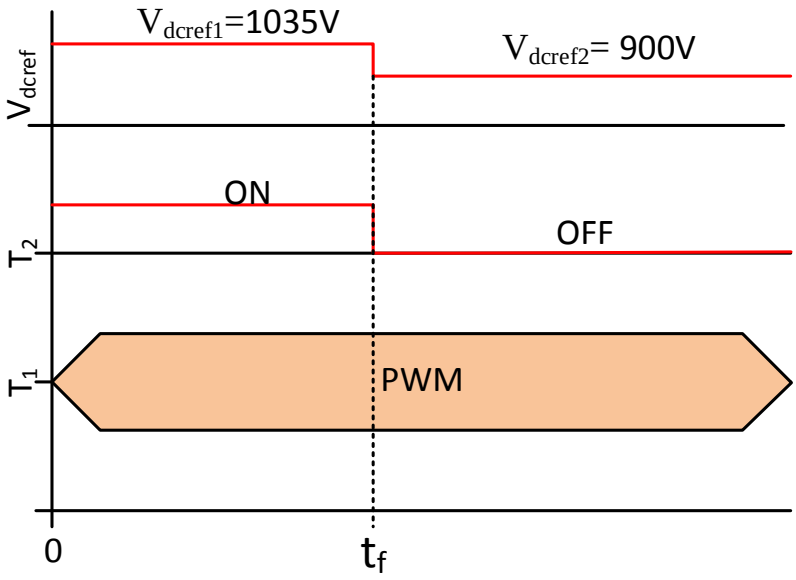

Figure 2.3 Test circuit operation.

2.6 CHOPPER CONTROL BLOCK DIAGRAM

The controller block diagram of the test circuit copper is shown in Figure 2.4. There are two controller loops using voltage feedback and current feedback. PI controllers are used in the controller loops. A Min function is used to select the minimum output of the PI's. The duty cycle is passed to the PWM block to generate the pulses for T_2. A comparator is used to detect the fault by comparing I_{CB} and I_{TH}. If the fault is detected then the IGBT T_2 is turned OFF and the reference V_{dcref} gets the V_{dcref2} value.

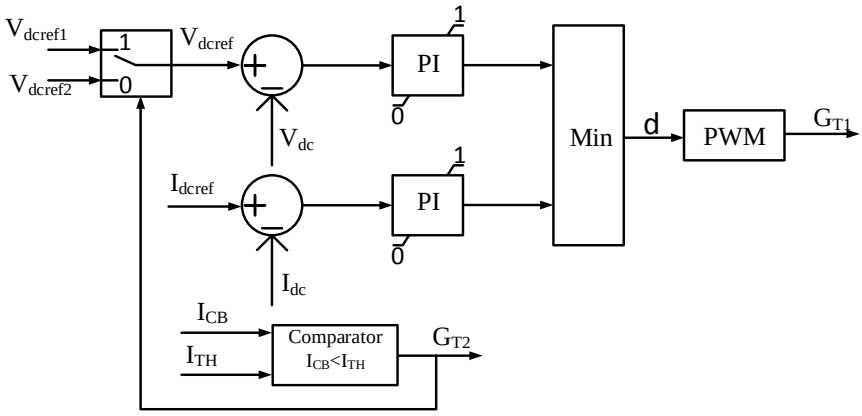

Figure 2.4 The controller block diagram of the test circuit chopper.

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2.7 CONTROL CIRCUIT DIAGRAM

The overall control diagram is shown in Figure 2.5. Each part is explained in the next subsections while the list of components for each part is provided in the Appendix.

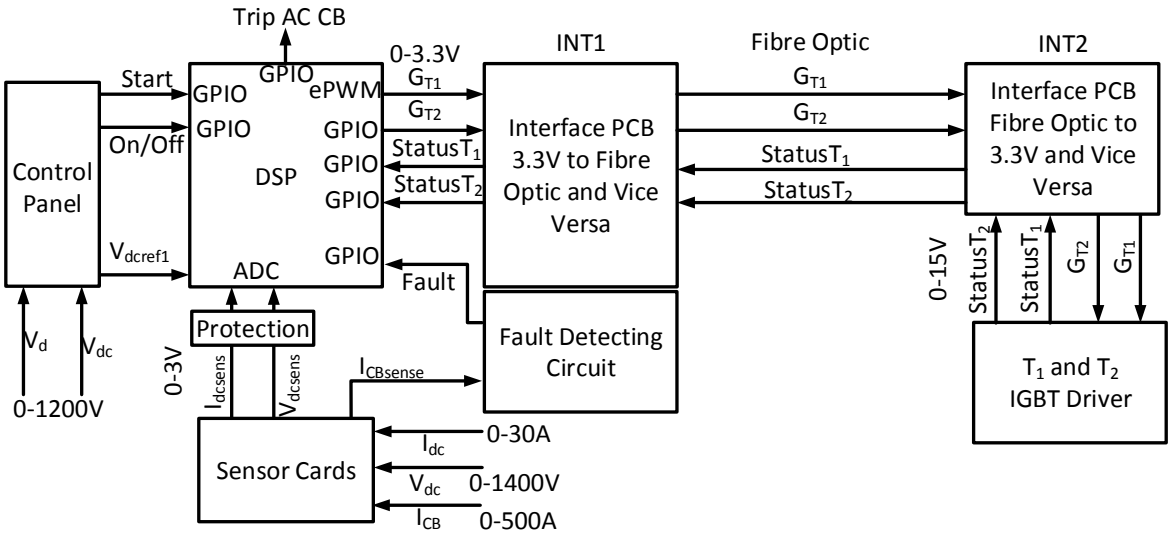

Figure 2.5 The control diagram of the test circuit.

2.7.1 DIGITAL SIGNAL PROCESSING (DSP)

The chopper is controlled using a TI DSP TMS320F28335. The controller board has On-board 12bit ADC which is used to digitize the analogue voltage from the sensors. The number of available General Purpose Inputs Outputs (GPIO) pins are more than 40 which is more than sufficient. DSP needs a 5V/1A power supply. The PWM signal connected to the IGBT T_1 is fed from ePWM of the DSP. The ADCs digitize the voltage V_{dc}, current Idc feedbacks, and V_{dcref} generated in control panel board.

2.7.2 CONTROL PANEL

Figure 2.6 shows a stand-alone control panel which has V_{dcref1}, ON/OFF switch, start buttons, and the fault initiation button. The reference value of the V_{dc} can be set using V_{dcref1}. The DSP are working in stand-alone mode and a 5V power supply is needed. The DSP boards generates a 3.3V. This is used in the control panel board. Two digital voltmeters are placed on the control panel. One of them shows the V_{dcref1}, and the other one shows measured either V_d or V_{dc}. A current meter on the control panel shows the DC CB current. Each part is explained below:

ON/OFF switch: Once switched ON, it makes the chopper ready to be turned ON. Switching OFF will turn the chopper OFF immediately.

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Start: If the ON/OFF switch is in ON position, pressing the start button will release the PWM pulses.

V_{dcref1}: the initial dc voltage can be set using V_{dcref1}.

Fault: fault is initiated by pressing the fault push button.

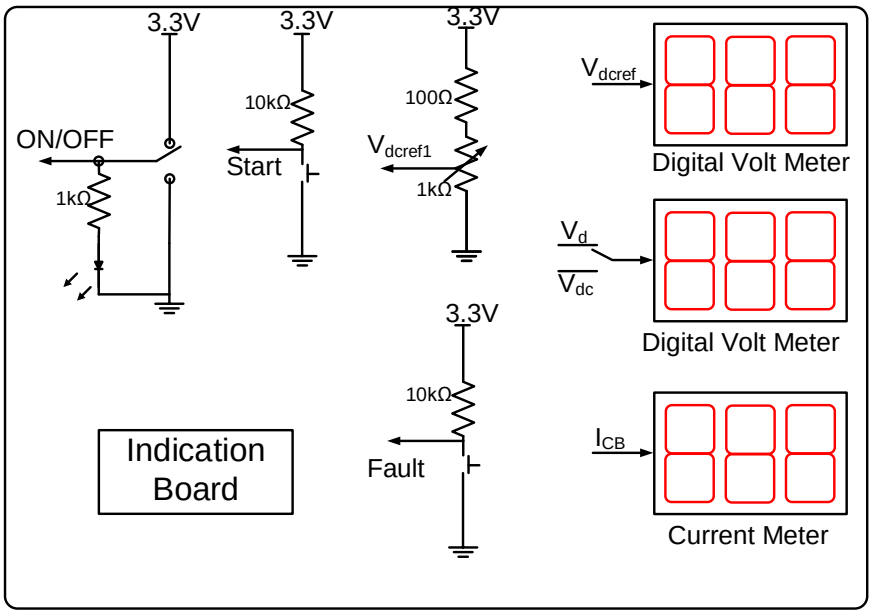

Figure 2.6 Test circuit Control Panel.

2.7.3 VOLTAGE SENSING CARD

A LEM LV 25-P voltage transducer is used which has the ratio of 2500:1000. The secondary current (Is) is 2.5 times the primary current (Ip). Series connection of 6 resistors of 22kΩ is used at the primary to convert the input voltage to current hence, $I_p = V_{in} / (6 \times 22k\Omega)$. At the output a 120Ω resistor is used to convert back the secondary current into voltage hence, $V_{out} = I_s \times 120$. The overall sensing gain would be as follows:

$$Vout = 2.5 \times \frac{Vin}{6 \times 22k} \times 120 = \frac{300}{132k} \times Vin$$
$$\Rightarrow Vin = \frac{Vout}{4.166} * 1000 \quad (0)$$

At nominal voltage, 900V, the output voltage of the sensing card is $Vout = 2.5 \times 120 \times \frac{900}{6 \times 22k} = 2.05V$. If the maximum V_{dc}=1300V is considered with the given gain above the output voltage of the voltage sensor card is: $Vout = 2.5 \times 120 \times \frac{1300}{6 \times 22k} = 2.95V$. The high precision voltage control is not essential and therefore errors are not further analyzed. The circuit diagram of the voltage sensing is shown in Figure 2.7.

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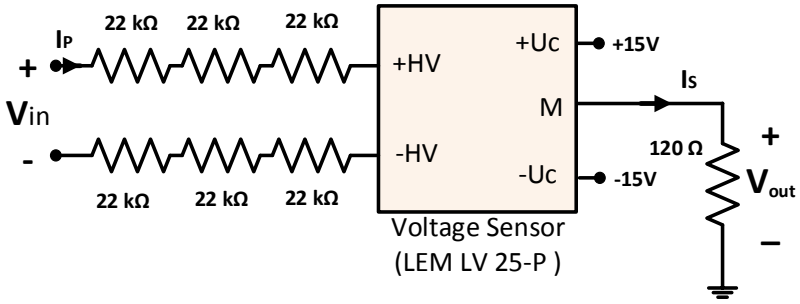

Figure 2.7 Schematic circuit of voltage sensor.

2.7.4 CURRENT SENSING CARD

Three current sensors are used in the test circuit, one measuring the dc current for controlling the chopper I_{T1}, one for measuring the CB current and creating the trip signal I_{CB}, and one for the measuring the CB current for current limiting control I_{DC}.

The circuit diagram of the current sensor for the chopper and trip signal is shown in Figure 2.8. LEM LA 100-P/SP13 current transducers are used which has the ratio of 1:1000. The secondary current (Is) is 1/1000 times the primary current (I_p). At the output a resistor R is used to convert the secondary current into voltage hence, $Vout = Is \times R = I_p / 1000 \times R$. The overall sensing gain would be as follows:

$$Ip = \frac{Vout}{R} * 1000 \tag{0}$$

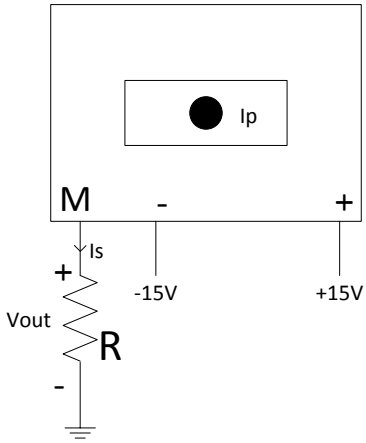

Figure 2.8 Schematic circuit of Current sensor.

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2.7.5 CURRENT SENSOR USED FOR MEASURING IDC:

The output of this sensor is connected to the DSP. The DSP ADC can measure the voltage up to 3.0V only. Hence, the maximum output voltage from the current sensor should be 3.0V. The resistor R is selected to be 50Ω. In that case, if the maximum current I_{dc}=60A is considered, with the given gain above, the output voltage of the current sensor card is: $Vout = 0.001 \times Ip \times R = 0.001 \times 60 \times 50 = 3V$ which is within the DSP limit.

2.7.6 CURRENT SENSOR USED FOR MEASURING ICB:

The output of this sensor is connected to the fault detecting circuit. The fault detecting circuit can take a voltage up to 15V. The resistor R is selected to be 100Ω. In that case, if the trip signal is activated and ICB=50A then the output voltage of the current sensor can be calculated as: $Vout = 0.001 \times Ip \times R = 5V$. This sensor is only used for activating protection which occurs around 50A, and therefore higher current measurement is not required. The test current recording is achieved using current clam probes and oscilloscopes.

2.7.7 CURRENT SENSOR USED FOR FAULT CURRENT LIMITING:

LEM HTA 1000-S current sensor is used for the fault current limiting current feedback measurement. The output of this sensor is connected to the DSP. The maximum output voltage from the current sensor should be 3.0V. This current sensor has an inbuilt potentiometer which changes the gain of the current measurement. The gain has been set so that for primary current of 1000A the sensor output voltage is 3V.

2.7.8 FAULT DETECTING CIRCUIT

For detecting the fault, the measured current I_{CB} is compared with a threshold I_{TH}, if the measured CB current is higher than the threshold level, it is considered as fault and an enable signal is sent to the DSP. The circuit schematic is shown in Figure 2.9. The threshold ITH is generated using a 5kΩ potentiometer. An op-amp is used for comparing the I_{CB} and I_{TH}. The output of the op-amp is 0-15V. This is scaled down to 0-5V and fed to the Fibre Optic (FO) driver. The FO light is sent to the INT1. Similarly there is a comparator for detecting the cleared fault. In this circuit the I_{CB} is compared with a small signal (i.e. 1A) and if the CB current is less than this signal a cleared signal is generated. This is shown in Figure 2.9. Two such boards are needed.

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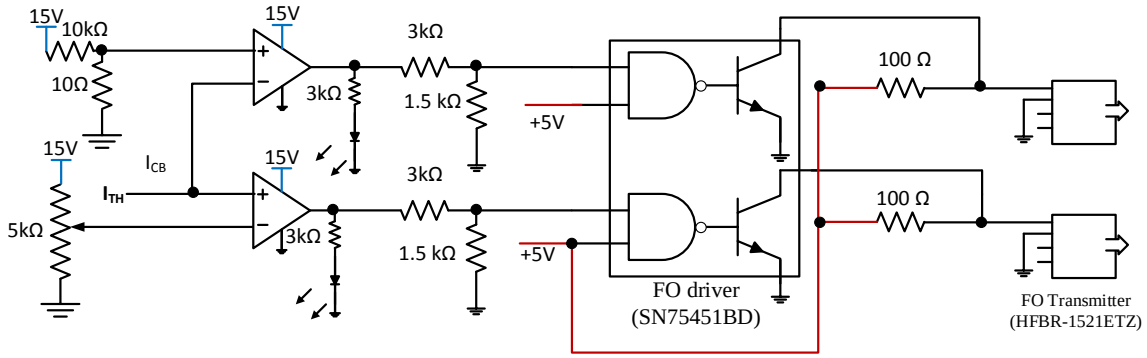

Figure 2.9 Fault detecting circuit configuration.

2.7.9 INTERFACE BOARD 1 (INT1)

To connect the GPIO pins of the DSP to the other components suitable interface boards are needed. The TMS320F28335 GPIO pins voltage is 3.3V. This voltage is converted to Fibre Optic (FO) light in the INT1. A buffer is connected to the output pins of the DSP to prevent loading of the DSP. The output of the buffer is connected to the FO transmitter driver. The designed interface board 1 converts 6 channels of 0-3.3V to FO. The INT1 converts 4 channels of FO lights to 0-3.3V signals. The circuit diagram of the INT1 is shown in Figure 7.2. in the Appendix. The PCB layout is shown in Figure 7.3 in the Appendix.

2.7.10 INTERFACE BOARD 2 (INT2)

The INT2 is connected to the IGBT drivers. It converts two FO lights, coming from the INT1, to 0-5V signal. There are two level shifters from 0-5V to 0-15V using Mosfet. The 0-15V signals are then fed to the IGBT driver. From IGBT driver there is a status signal of 0-15V. This is scaled down to 0-5V and fed to a FO transmitter driver. The FO from this transmitter will go back to the INT1. The circuit schematic of INT1 is shown in Figure 7.4. The layouts of the INT1 are shown in Figure 7.5. Totally two INT2 boards for T_1 and T_2 are needed.

2.7.11 FAULT INITIATION CIRCUIT

The fault Thyristor is triggered using a push button provided on the control panel. The trigger circuit is shown in Figure 2.10. Once the fault is initiated the DC CB opens. In case that repeated reclose control is implemented,

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the DC CB will reclose after a short time T_{rec}, and if the fault still exist the DC CB opens again. If the fault is cleared, the DC CB stays closed. This process is shown in Figure 2.11.

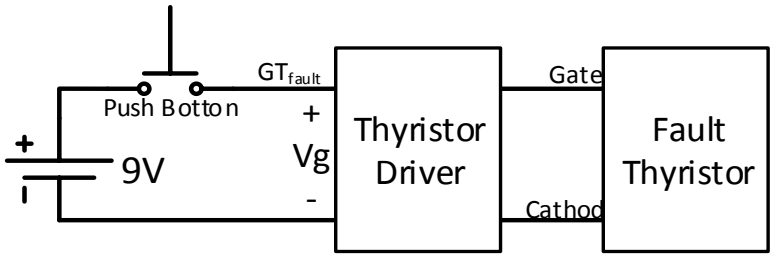

Figure 2.10 Control block diagram of triggering the fault Thyristor.

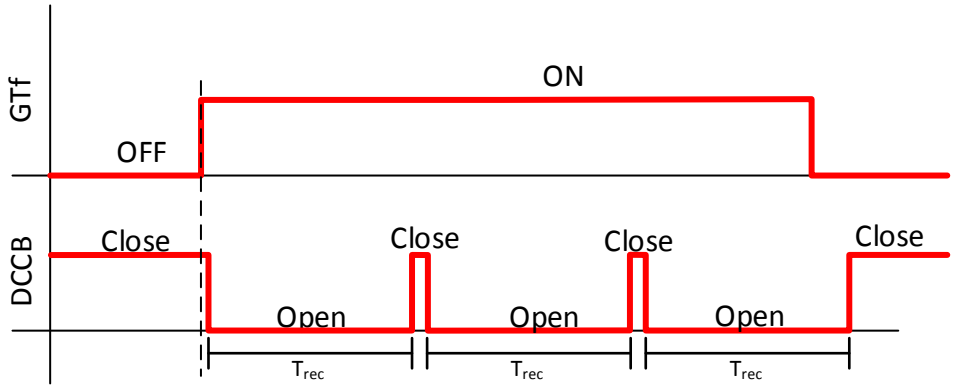

Figure 2.11 Timing of the fault signal and reclosure of the DC CB.

2.7.12 ADC OVER VOLTAGE PROTECTION

A protection circuit is used to clamp the ADC input voltages to 3.3V and prevent over voltage. The circuit diagram is shown in Figure 2.12. It is not expected that significant energy will be dissipated in the control circuit and therefore such simple overvoltage protection will suffice.

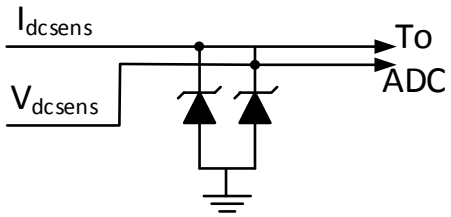

Figure 2.12 Protection circuit for the ADC.

2.8 TRANSFORMER AND DIODE BRIDGE RECTIFIER (DBR)

The power convert shown in Figure 2.1 is a buck converter and can only regulate the output to a smaller voltage than the input voltage. Based on the design specifications, the converter should be capable of controlling the output voltage to 1000V which will be tested independently. Hence the input voltage should be higher than this value by about 10%. A 30kW transformer with single 415V primary winding and double 415V secondary

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windings is used in the test circuit. The secondary windings are connected to the DBR, which are connected in series. The rectifier voltage V_d can be calculated as:

$$V_d = 2 \times 415\sqrt{2} = 1{,}174 \quad (0)$$

2.9 INRUSH CURRENT LIMITING (ICL) AND PROTECTION

2.9.1 INRUSH CURRENT LIMITING

The converter power transformer cannot be directly energized due to high inrush current and high charging current of the transformer and capacitor Cd=10μF (all component details are given in the Appendix). A circuit is employed which limits the current. The circuit practically inserts resistors in the 3-phase lines. The resistors limit the transformer inrush current as well as the capacitor currents. After few seconds the resistors are shorted and the transformer is connected to the 3-phase supply. The pre-charging circuit is shown in Figure 2.13.

By pushing the PB_NO the contactor-1 closes and the transformer is energized through the 10Ω resistors. The relay connected to the bobbin of the contactor-2 closes after few seconds. This closes the contactor-2 and shorts the 10Ω resistors.

2.9.2 PROTECTION

By pressing the PB_NC, the transformer gets disconnected from the grid. This can be used to de-energize the transformer in normal condition or in emergency situations.

In case of drawing high current by the transformer the MCB will trip which results in opening the contactor-1 and contactor-2.

Another protection signal comes from the DSP. The DSP will check the dc current (I_{dc}) and dc voltage (V_{dc}) if they are higher than the respective values the DSP will send the trip signal. It is possible to put the under voltage trip so that if the dc voltage goes below a value the DSP sends a trip signal to the contactors.

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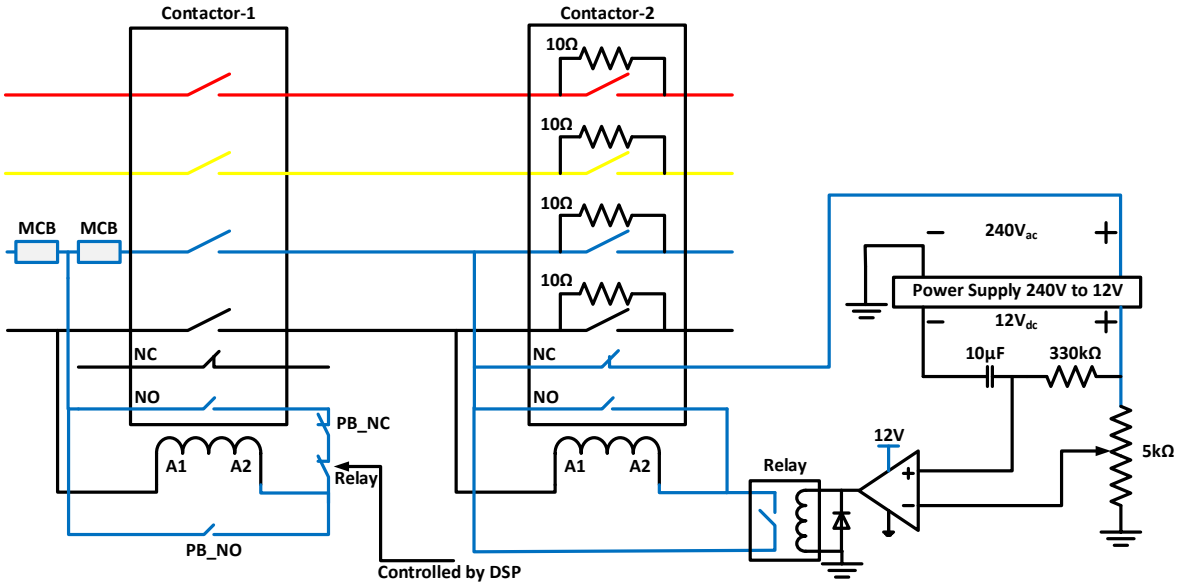

Figure 2.13 Transformer inrush current limiting and protection circuit.

2.9.3 PSCAD SIMULATION RESULTS

The test circuit model is developed in PSCAD and the start-up simulation results are shown in Figure 2.14. From 0 to 0.18 sec the chopper controller is in the current control mode. This can be seen from the dc current I_{dc} which is limited to 40A. Once the voltage reaches the reference voltage, the controller moves to the voltage control mode. The dc voltage is controlled to around 1040V. At this time the setup is ready and waiting for the fault to be initiated. The grid current I_S is also shown in Figure 2.14. The system dynamics are complex and PSCAD modelling was essential to tune all the controllers. The PSCAD model of the test circuit is shown in Figure 7.1.

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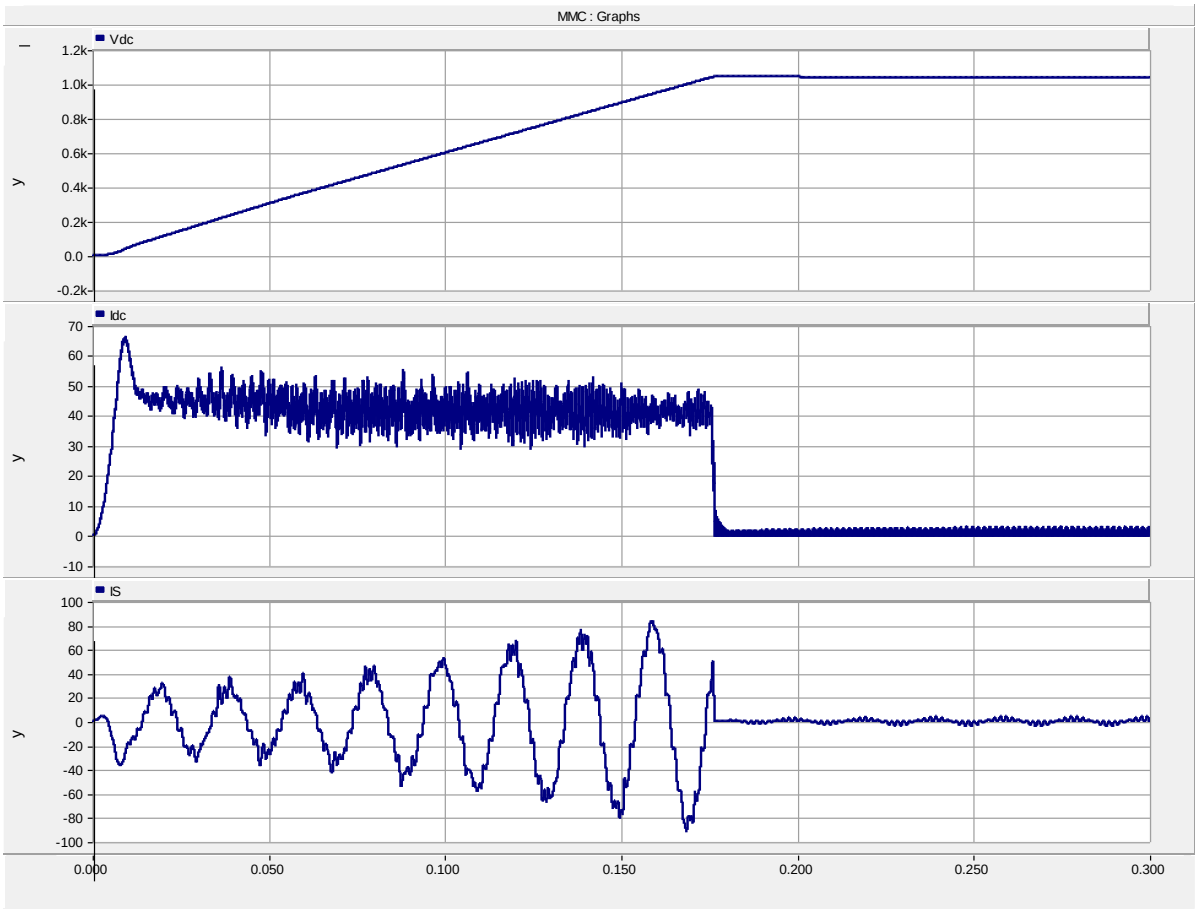

Figure 2.14 Simulation results during the start-up of the test circuit. Output voltage Vdc, dc current Idc, and the grid current I_{Sa}.

The dc voltage of the test circuit is plotted in Figure 2.15. It can be seen that the dc voltage consist of 3 components, a dc component, 13th harmonic components, and the high frequency switching components. However, the peak to peak 13th harmonic component is less than 0.05V and the peak to peak switching component is less than 0.02V.

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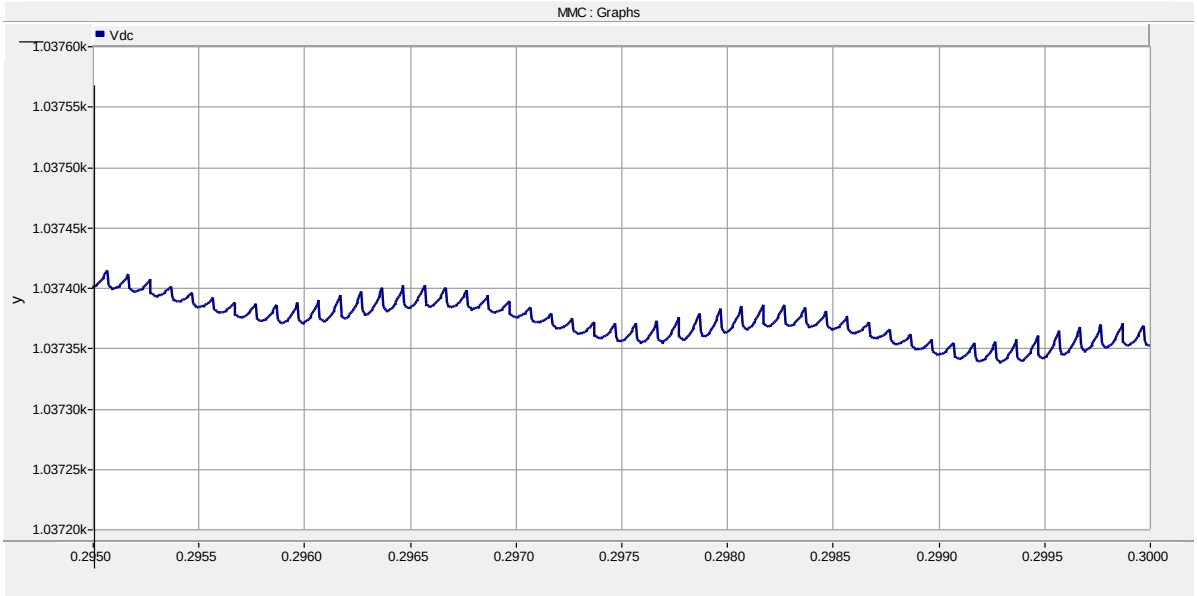

Figure 2.15 dc voltage of the test circuit.

The test circuit is equipped with over current self-protection. The PSCAD simulation results, the IGBT T1 current, are shown in Figure 2.16. A permanent fault, at t=0.25s, is applied to the test circuit. Two cases are studied here, with self-protection disabled, shown in Figure 2.16(a), and with self-protection enabled, shown in Figure 2.16(b). It can be seen that the T1 current goes up to 600A. This will damage the IGBT. However, with the self-protection activated, once the current in the T1 reaches 75A, the test circuit is shut down and the IGBTs are protected.

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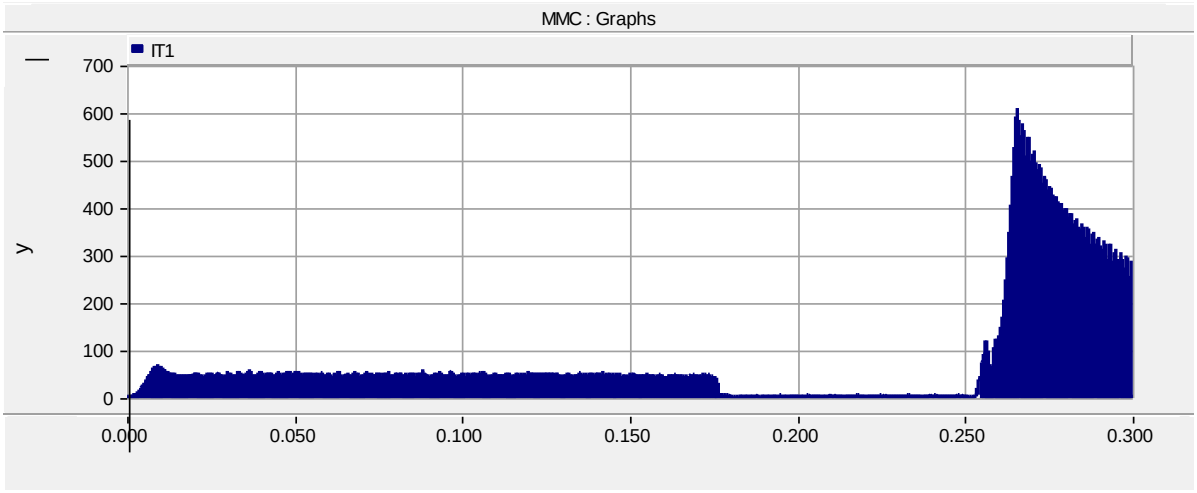
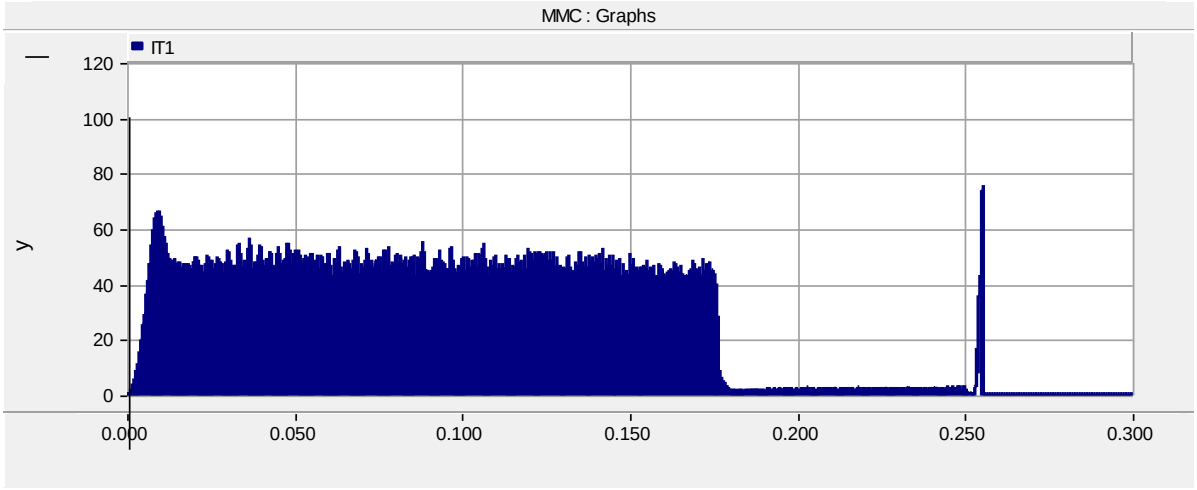


(a)



(b)

Figure 2.16 Over current protection of the test circuit (a) over current protection disabled, (b) over current protection enabled.

2.10 TEST CIRCUIT EXPERIMENTAL RESULTS

The controller is firstly verified by extensive testing on RTDS DC CB model developed in [11]. Only hardware responses are shown for brevity.

The experimental result of the test circuit during the start-up is shown in Figure 2.17. It can be seen that, once the test circuit is turned ON, the controller goes to the current control mode. During this period the current is limited to around 40A and the dc voltage rises linearly. After some time the voltage control mode takes over and the voltage is controlled to 1040V. The grid current is shown in the last figure. The test circuit draws a peak current of 70A. However, this is for a short duration of under 10μs which is not causing any issue. Once the

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voltage stabilized on 1040V, the circuit is ready for fault initiation. The line current has some noise because of diode bridge low-order harmonics.

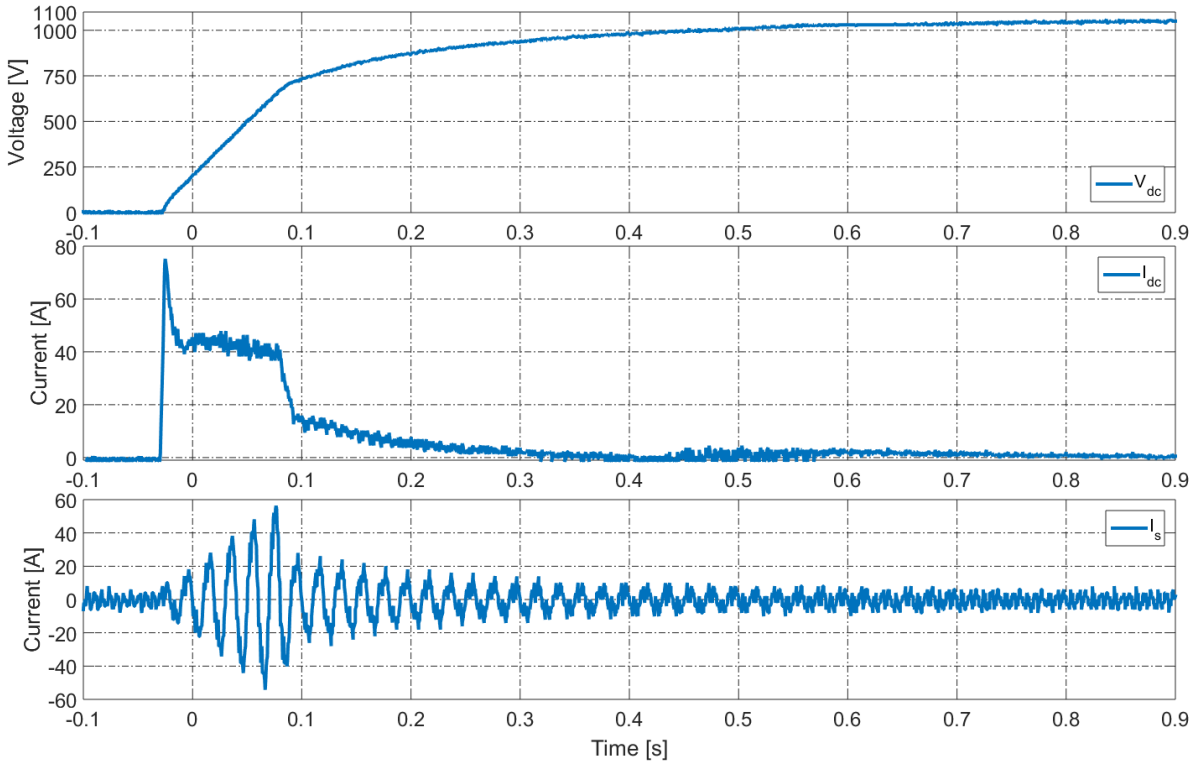

Figure 2.17 Experimental results during the start-up of the test circuit. Output voltage Vdc, dc current Idc, and the grid current ISa.

A permanent short circuit test has been carried out on the test circuit. The fault current rises up to 1000A. However this is the capacitor bank current. Once the IGBT T1 current (capacitor charging current) is higher than a threshold value, 75A, the test circuit is turned OFF. This is shown in Figure 2.18. We cannot measure the IGBT T1 current due to the sandwich bus bar structure. In this test the DC CB series inductor of 3.5mH is used as it would be the case in all tests. This inductor causes DC current flow even after DC voltage drops to zero. It is seen that at 0.01s T1 is turned off and this will disconnect the charging circuit to prevent any damage.

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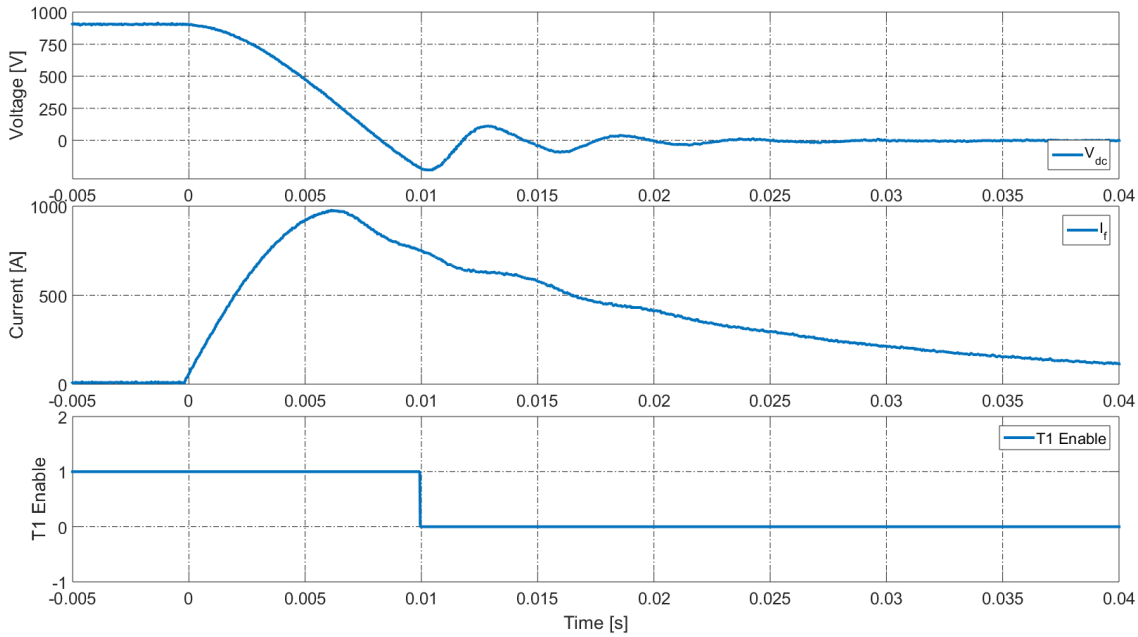

Figure 2.18 Short circuit test on the DC CB test circuit.

The circuit is grounded on one side as shown in Figure 2.1, and only positive voltage is available. The negative DC current is provided by rotating the test object.

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3 IGBT BASED HYBRID DC CB

Component design and implementation of hybrid DC CB is explained in this chapter. The PSCAD simulation results and experimental verification are presented.

3.1 HYBRID DC CB CIRCUIT CONFIGURATION

Figure 3.1 shows an IGBT based hybrid DC CB. The topology is based on ABB DC CB [4], [5], [15], [16], [22], and [22]. It consists of three parallel branches:

1. Normal current branch.
2. Main breaker branch.
3. Energy absorption branch.

The normal current branch consists of an Ultra-Fast Disconnector (UFD) S_1, and a Load commutation switch (LCS) T_1. The main breaker branch consists of series connected IGBTs.

The aim is to develop a hardware DC CB of the same topology but with lower ratings. The ratings are limited by the capability of university laboratory and the component cost considerations:

- Rated current: 30A. This gives around 30kW continuous power which is close to the limit of laboratory power supply. The charging transformer is also limited to 30A in order to limit costs.
- Rated fault current: 500A. The IGBTs in the main breaker rated 600A are selected considering the project budget. It is expected that these IGBTs will have similar basic characteristics as 3.3kV 2kA IGBTs used in the actual DC CBs.
- Rated DC voltage: 900V
- Opening time: 2ms. The opening time is restricted by the speed of ultrafast disconnector, and the 320kV ABB prototype has opening time of 2ms. Certainly faster opening time is possible at such low voltage level but it is decided to keep it at 2ms since this provides the same current flow duration in the main branch. Also developing very high speed disconnector would require high-precision mechanical design which is beyond the capabilities of University workshop.

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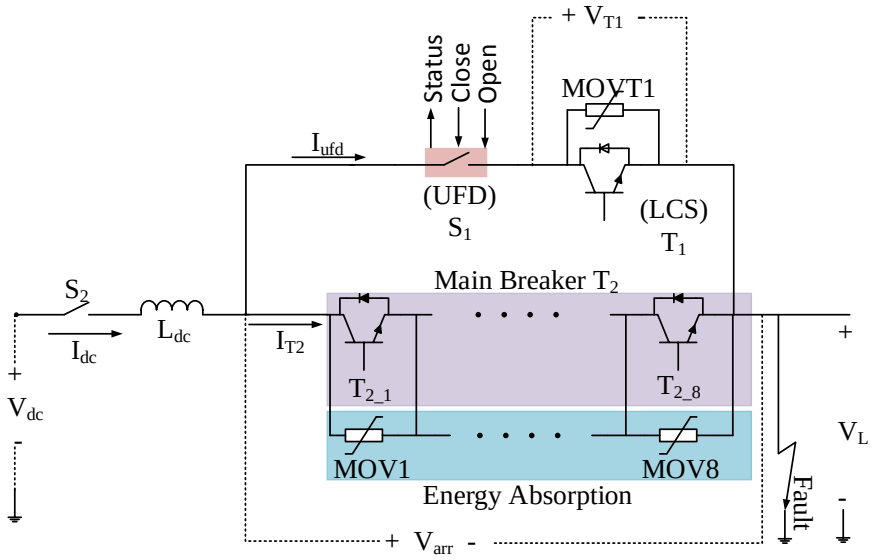

Figure 3.1 Circuit configuration of hybrid DC CB.

3.2 HYBRID DC CB OPERATIONS

The closing and opening operations of the hybrid DC CB are explained in next subsections.

3.2.1 CLOSING OPERATION

The closing operation of the hybrid DC CB is explained in this section. The green blocks in the figures show that the component is active. An active switch means it is either ON or closed, depending on the type of the switch. An active arrester means that the current is passing through it. The red lines show current carrying paths.

1. At the beginning the DC CB is open, on receiving the closing command, the switch S_2 is commanded to close its contact. The operation time of S_2 is assumed 20ms but deepening on the actual interrupter employed it may take up to 100ms. This is shown in Figure 3.2(a).
2. After the S_2 is completely closed, the switches T_2 are turned ON. This is shown in Figure 3.2(b). At this stage the DC CB is closed through S_2 and T_2. The current flows through the red lines shown in in Figure 3.2(b).
3. S_1 should be operated at zero current. S_1 is commanded to close. The operation of S_1 takes around 2ms. This is shown in Figure 3.2(c). Same opening and closing coils are used and the speed is same in both operations
4. Once S_1 is completely closed then T_1 is turned ON. This is shown in Figure 3.2(d). At this stage the DC CB is completely closed and the current passes through S_1, T_1, and S_2 shown with red lines in Figure 3.2(d).

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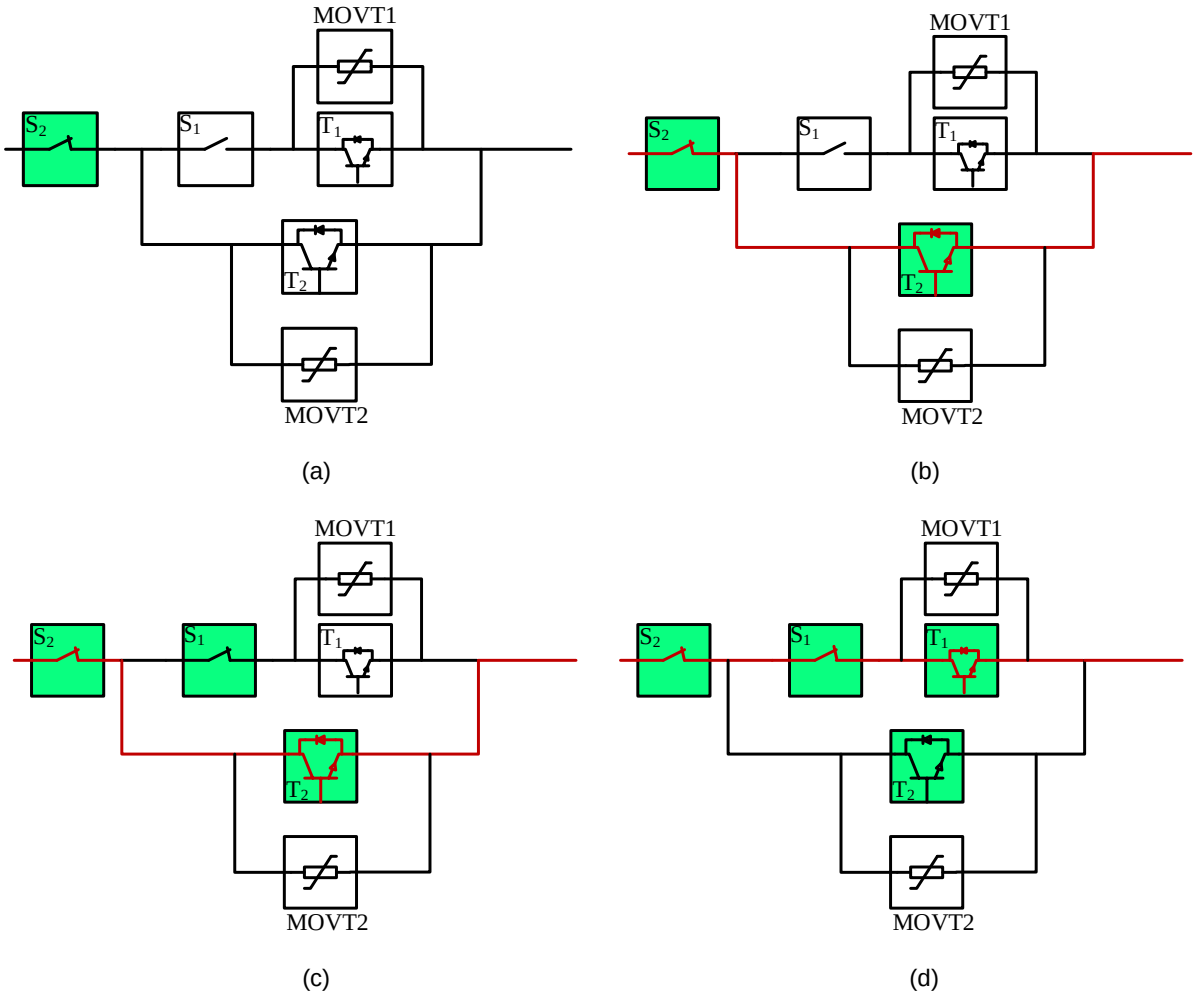

Figure 3.2 Block diagram of HYBRID DC CB in closing sequence.

3.2.2 OPENING OPERATION

The opening sequence of the DC CB is as follow:

In normal closed condition shown in Figure 3.2(d), the current is nominal load current and the voltage across the hybrid DC CB is nearly zero. The current in T_2 does exist but is negligibly small compared with T_1 current. The DC fault is applied at t = 0s and the current begins to increase.

1- Once the current hits a limit, a trip order is sent to T_1. T_1 turns OFF and makes the current to commutate to T_2. This is shown in Figure 3.3(a). The current path is shown in red lines.
2- Once the current commutates completely to T_2, S_1 is commanded to open. This operation takes around 2ms. This is shown in Figure 3.3(b).
3- Once the S1 is completely open, the T_2 is turned OFF. This force the current to commutate to the surge arrester branch and the arrester voltage facilitate current reduction. This is shown in Figure 3.3(c).

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4- Once the current goes below the residual current, the S_2 is ordered to open. By opening the S_2 the DC CB is completely open.

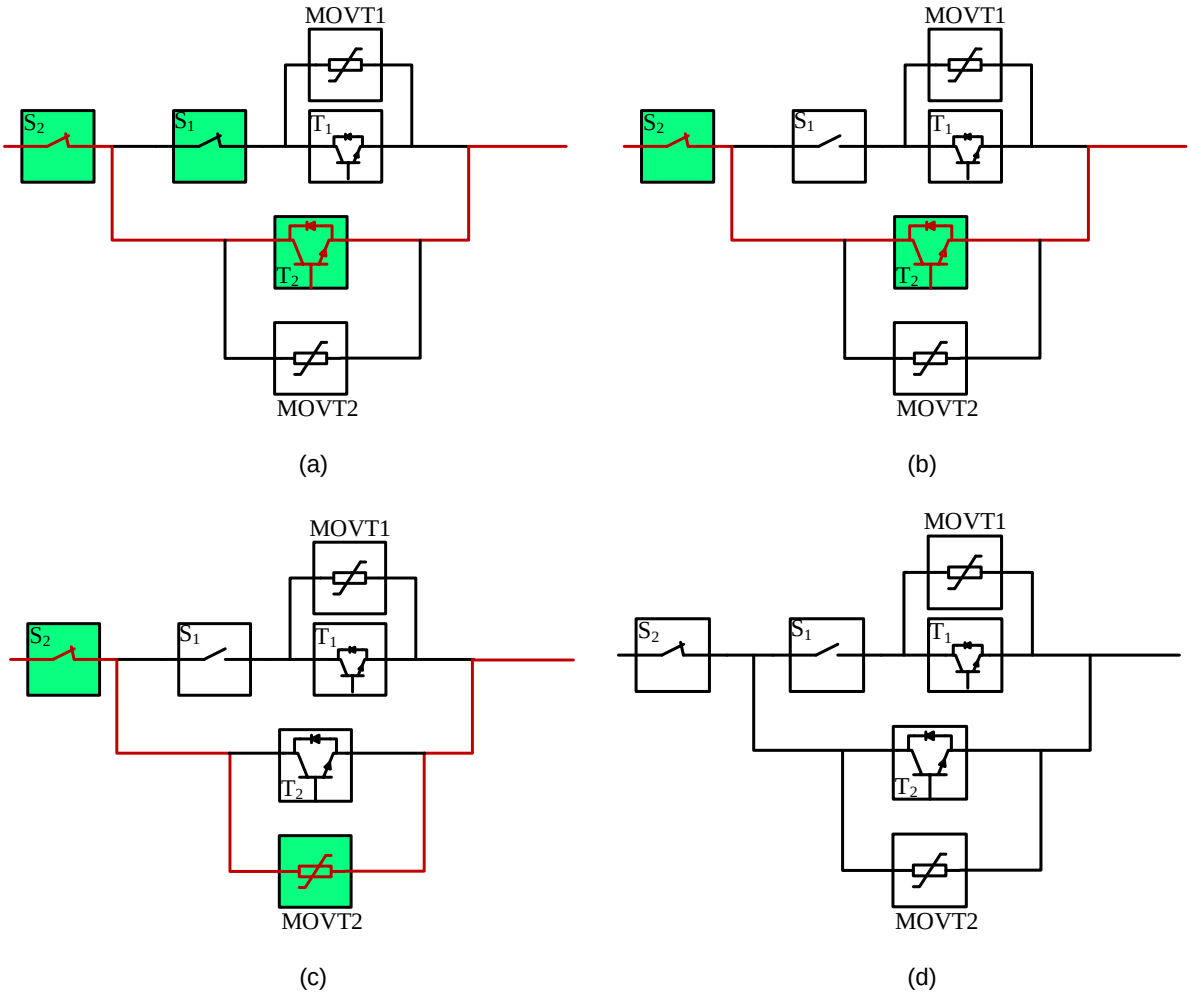

Figure 3.3 Block diagram of HYBRID DC CB in opening sequence.

3.3 ULTRA-FAST DISCONNECTOR (UFD)

The speed of operation of hybrid DC CB is crucially determined by the speed of UFD. Detail design, fabrication and testing of a low voltage UFD at a University laboratory are explained in this Section.

The UFD design will be selected to closely resemble the actual design in 320kV DC CB [18]. All other commercial contactors have totally different construction (spring driven mechanism usually) and the operating time is usually much longer than 2ms and therefore they are not suitable.

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The UFD is designed to operate in 2ms and separates the contacts by 3.0mm, which is adequate to withstand a voltage level up to 7kV in air. The nominal current is 30A and the trip signal is to around 50-100A. This implies that the maximum expected UFD current is 100A and the contacts of the UFD are designed to carry a rated current of 100A. The speed requirements demand a driver capable of supplying a current pulse of few kA, which is achieved using capacitive storage [17], [18].

Modeling of UFD is discussed in [17][18]and it is also reported in some depth in task 6.3 in [12]. Only brief summary required for UFD design is presented in this report. Some aspects of this UFD design have bene reported in [19].

3.3.1 UFD OPERATION PRINCIPLES AND CONSTRUCTION

Figure 3.4(a) shows the schematic of the designed UFD with all the main parts numbered. The fabricated UFD is shown in Figure 3.4(b).

The main parts of the UFD are, as labelled in Figure 3.4(a):

1- Bi-stable structures, labelled as “1”, which are used to hold the actuator disks in two stable positions (open or closed).
2- The Thomson Coils (TCs) for closing operation, labelled as “2”. By energizing these two TCs, forces are generated in the actuator disks and move the actuator disks away from the energized TCs.
3- The TCs for opening operation, labelled as “3”. By energizing these two TCs, forces are generated in the actuator disks and move the rods with contacts away from one another.
4- Two actuator disks with rods, labelled as “4”. Currents are induced in the actuator disks. This results in generation of forces that move the actuator disks upwards or downwards.
5- The parts labelled as “5” are the contacts which are attached to the rods using insulators. The copper contactors make or break the electrical circuit.

When the UFD is in open position, the actuator disks are close to the TCs numbered 2 and the contacts are separated. For closing the UFD the TCs numbered 2 are energized and TC currents induce high current in the actuator disk. Interaction between the current in the TC and actuator disk currents generates a force which push the actuator disks away from the TCs. The opening process is similar but TCs number 3 are energized.

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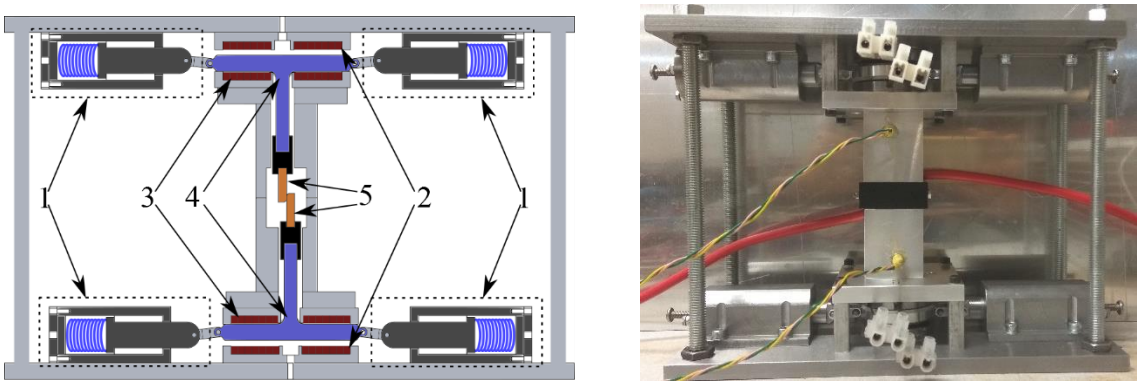

(a) (b)

Figure 3.4 (a) Schematic of the designed UFD. (b) Fabricated UFD.

3.3.2 UFD ELECTROMECHANICAL MODELING

The electromagnetic energy in the TC is discussed in [1][17]-[20]. Only a brief model is shown here. The electromagnetic energy in the TC can be represented as:

$$E_{em} = \frac{1}{2}\left(L_{coil}I_{coil}^2 + L_{arm}I_{arm}^2 - 2MI_{coil}I_{arm}\right) \quad (0)$$

Where L_{coil} and L_{arm} are the self-inductance of the TC and the actuator disk respectively. I_{coil} and I_{arm} are the TC current and the actuator disk induced currents respectively, and the M is mutual inductance between the TC and actuator disk. The electromagnetic force can be obtained by differentiating of the electromagnetic energy in (0) [20].

$$F_{em} = \frac{dE_{em}}{dz} = -\frac{dM}{dz}I_{coil}I_{arm} \quad (0)$$

The force generated on the rod is balanced by the acceleration force, bi-stable springs F_{bis}, viscous friction B, static friction F_{fric}, and weight W_g,

$$F = m\frac{dv}{dt} + Bv + F_{fric} - F_{bis} \pm W_g \quad (0)$$

m is the total moving mass. The calculated parameters are shown in Table 3.1. Figure 3.5 shows one (of four) assembled Thomson coils.

Table 3.1 UFD Parameters.

Parameter	Label	Value
viscous friction	Bv	20N
static friction	F_{fric}	4N
bi-stable springs	F_{bis}	62N

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Mutual inductance	M	0.2µH
Moving parts Weight	Wg	140g
Thomson coil turns	N	8.5turns
Actuator disc diameter	D	50mm
Copper contact s area	A	3.1mm^2
Spring constant	K	29.85

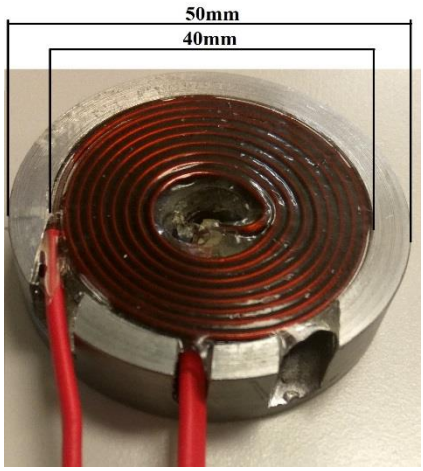

Figure 3.5 Fabricated Thomson Coil.

3.3.3 UFD POWER SUPPLY

The desired operating time of UFD is 2ms with separation distance of 3mm, which requires very large acceleration which in turn demands significant electromagnetic force. The above model indicates that several kA current pulse is required. These pulse currents are supplied by the UFD power supply based on a storage capacitor, shown in Figure 3.6. The capacitor Cd is charged using a 100VA transformer Tr and a diode bridge rectifier. The charging is controlled by the Mosfet, T_{ch}, while resistance R limits the charging current. This power supply can supply two TCs as shown in the figure. By triggering T1 or T2 the TC to be energized is selected. This power supply can work up to 200V and can supply a pulse current of up to 5kA. Totally two of such power supply boards are needed for all four TCs. The fabricated UFD Power Supply is shown in Figure 3.7. The parameters of the UFD and the power supply are tabulated in Table 2

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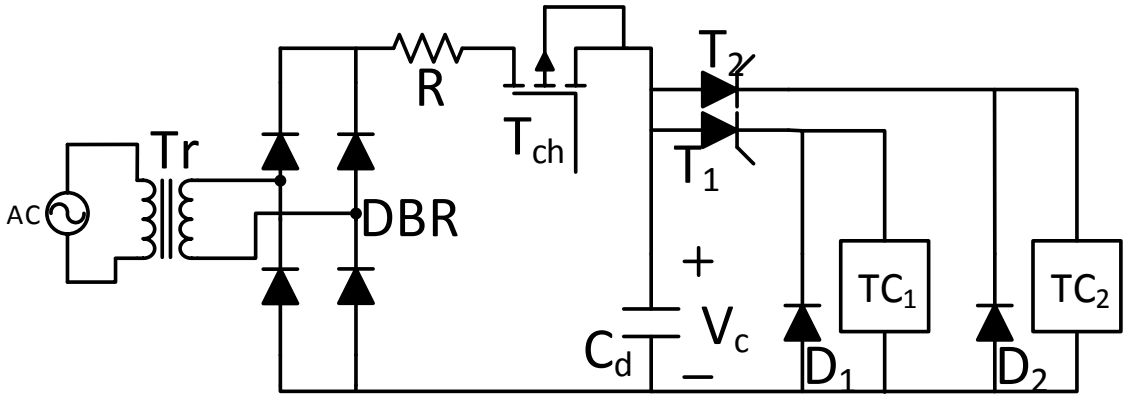

Figure 3.6 UFD Power Supply.

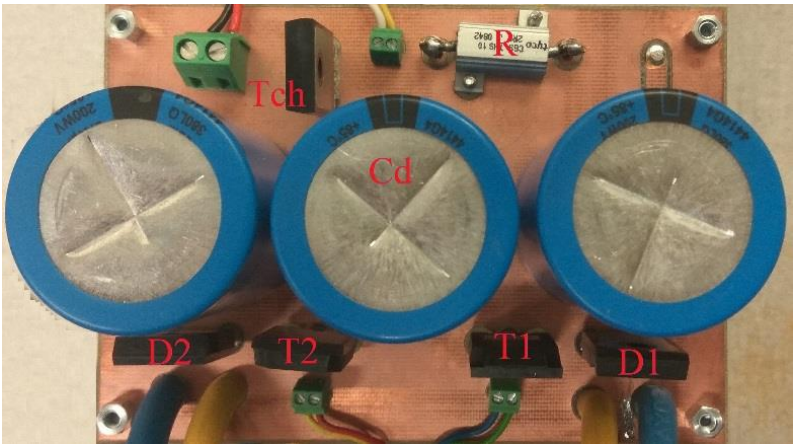

Figure 3.7 Fabricated UFD Power Supply.

3.3.4 POSITION MEASUREMENT

To detect the position of the actuator disk and measure the operation speed, hall sensors are used. A small magnet is attached to the actuator disk and a hall sensor is fixed stationary next to the magnet. The sensor gives voltage signal proportional to the position of the rod and this has proven to be sufficiently accurate to measure position of the contacts.

Table 3.2 UFD driver parameters.

Parameter	Label	Value
Charging Resistor	R	2.2
Charging Mosfet	T_{ch}	200V, 50A
Thyristor	T2, T1	1600V, 70A
Diode	D1, D2	600V, 80A
Capacitance	C_d	8.1mF
Rectifier	DBR	1000V, 50A
Transformer	Tr	100VA

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3.3.5 EXPERIMENTAL RESULTS

The UFD has been tested experimentally and the results are presented in this Section. The experimental measurements of the closing operation are shown in Figure 3.8. The closing command is send to the UFD at time t=0s. The position sensor output (yellow) shows zero at t=0, which indicates open position. The position output of 3mm indicates that the UFD is fully closed. It can be seen that the UFD closes in 1.8ms. The capacitor voltage discharges in 300μs as shown by the blue curve. The peak TC current is around 2.94kA as shown by the red curve.

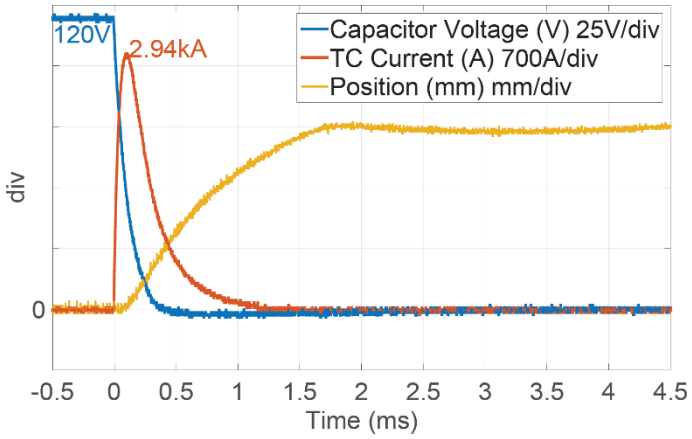

Figure 3.8 UFD closing operation with driver voltage of 120V.

The UFD opening operation is shown in Figure 3.9. The opening command is send to the UFD at time t=0s. The UFD reaches fully open position in 1.8ms. Examining the position curve, it can be seen that the actuator disk has a slight bounce of around 0.2mm. The applied driver voltage of 120V is the maximum value that results in an acceptable bounce.

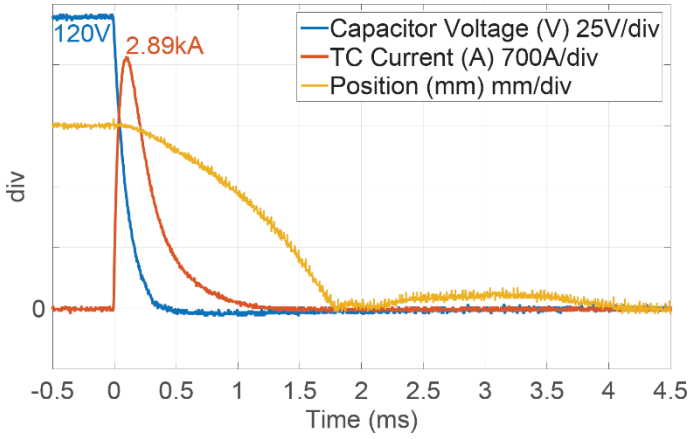

Figure 3.9 UFD opening operation with driver voltage of 120V.

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The UFD has been tested at different driver voltage from 90V to 170V and the opening time is measured, in order to explore possible increase in the operating speed. For voltages over 120V bounce is pronounced but it is assumed that bounce can be eliminated in other ways. The results are shown in Figure 3.10. It can be seen that the UFD operates in 3.7ms if the UFD power supply capacitors are charged up to 90V. As the capacitor voltage is increased the UFD operates faster. It can be observed that increasing the capacitor voltage from 90V to 130V reduces the operating time from 3.7ms to 1.5ms. In this case the input voltage is increased by 44.4% and results in operation time reduction of 59.5%. If the capacitor voltage is increased further by 30% to 170V the operation time reduces by 28% to 1.08ms. If the UFD is to operate in 2ms, the capacitor voltage should be 115V.

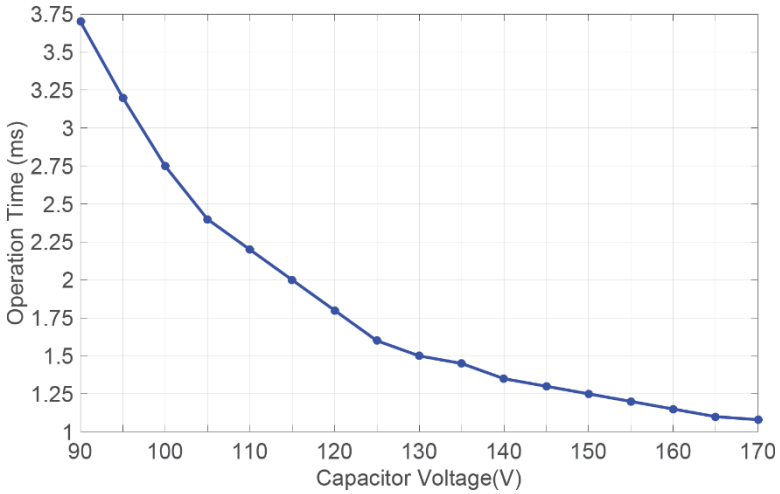

Figure 3.10 UFD opening time versus applied power supply voltage.

3.3.6 IMPROVING OPENING SPEED USING ELECTROMAGNETIC BRAKING

If the UFD is operated faster, the bounce becomes significant. Figure 9 shows experimental results with power supply voltage of 140V which results in around 40% bounce (1.3mm). This is not acceptable as this results in the lower withstand voltage of UFD and may results in arcing.

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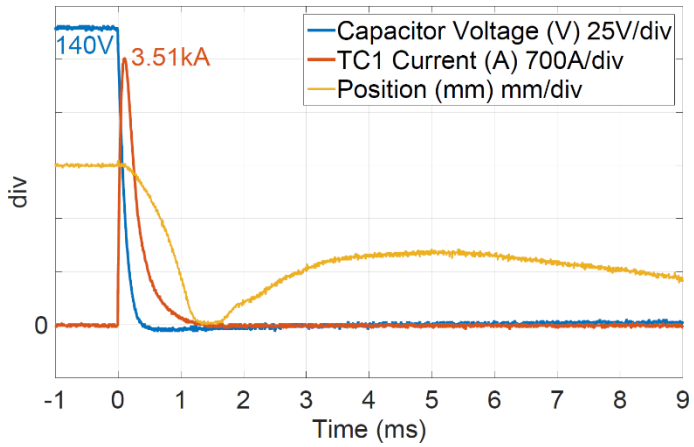

Figure 3.11 UFD opening with driver voltage of 140V.

The bounce problem has been recognized by manufacturers and pneumatic damping is achieved with the insulating SF6 gas in the initial designs [18]. Our UFD uses open air as insulator and therefore different methods are studied to damp the bounce.

Electromagnetic Braking (EMB) is a braking mechanism which creates a counter force at the end of traveling of the actuator disk. This reduces the speed of the actuator disk and hence, reduces the bounce effectively. The procedure for EMB is as follows:

1. The opening TCs are energized and the position sensor output is monitored.
2. Once the position sensor reaches the threshold (80%-90% of the traveling distance), the closing TCs are energized with lower voltage. The voltage magnitude and instant of EMB is determined experimentally.

Figure 3.12 shows the effect of EMB for different values of voltage on the braking coil. A trade off should be selected between operating speed and percentage bounce.

The experimental results for opening with selected EMB parameters are shown in Figure 3.13. It can be seen that the EMB effectively eliminates the bounce and the UFD can operate in around 1.8ms. The observed bounce is around 0.2mm which is within the acceptable margin.

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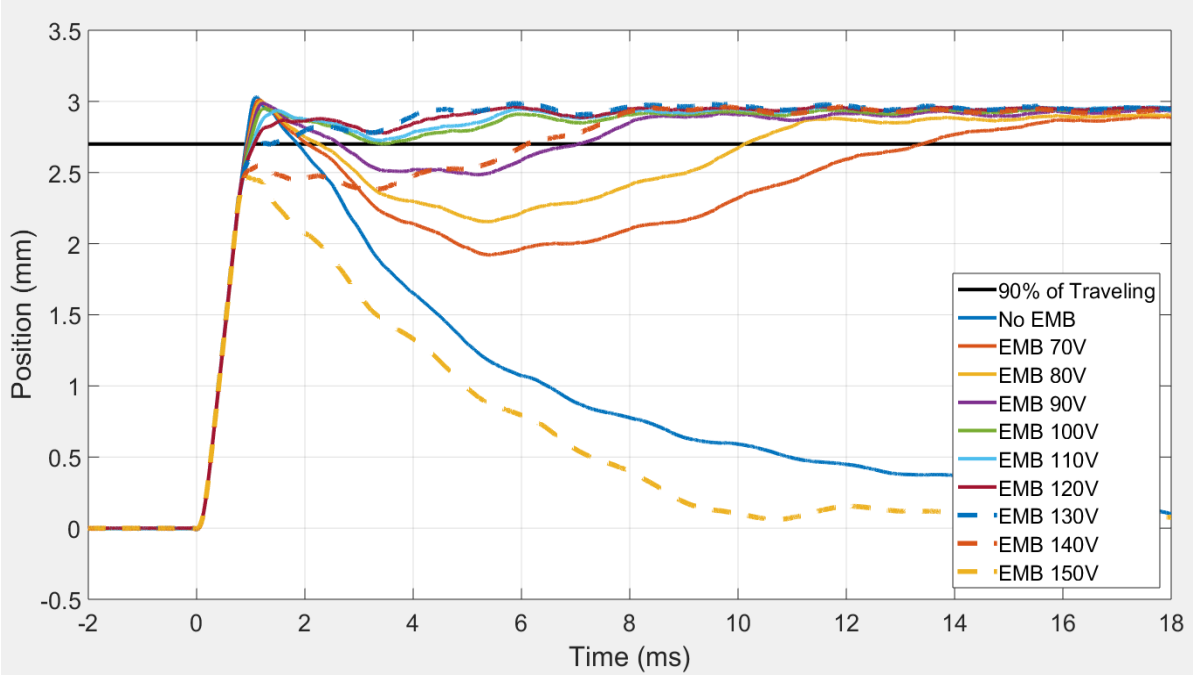

Figure 3.12 Effect of elctro-magnetic braking

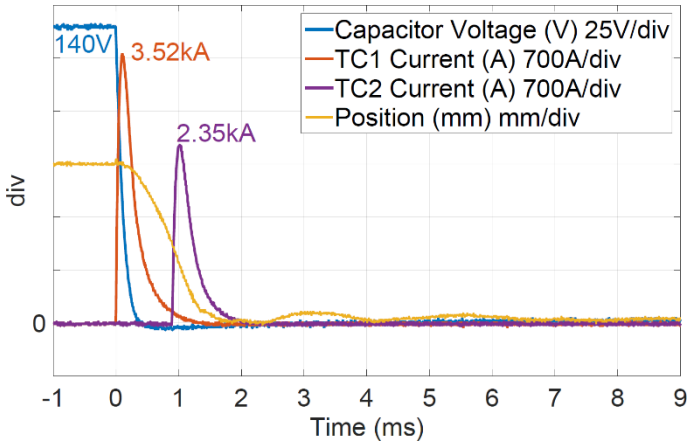

Figure 3.13 UFD opening with driver voltage of 140V and electromagnetic braking.

The full dynamic UFD modelling and comparisons with 320kV UFD are provided in [12], and will be further employed in failure mode studies in the Task 6.6.

3.3.7 IMPROVING OPENING SPEED USING RUBBER DAMPERS

Further improvement in the dynamical operation of the UFD, particularly increasing the velocity of the UFD in the opening operation, was carried out using elastic dampers. An increase in the Thomson coil voltage leads to

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further increase in the velocity of the actuator, but it is associated with increased kinetic energy of the disc. As a feasible alternative to absorb the kinetic energy of the actuator at the end of the strike is to use a damping mechanism. The feasibility of using rubber ring around the rod of actuator, as shown in Figure 3.14 was investigated through practically for the developed prototype UFD.

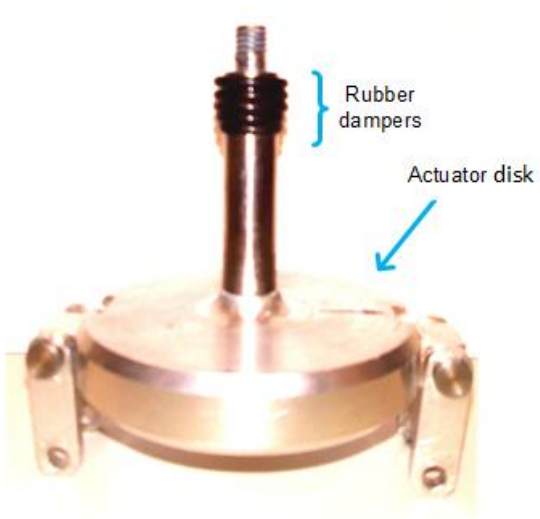
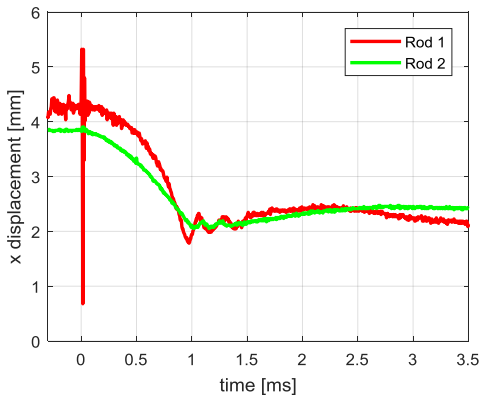


Figure 3.14 UFD actuator equiped with rubber dampers.

The experimental result for opening the UFD equipped with rubber dampers under supply voltage of 180 V is shown in Figure 3.15, where the raw sensor measurements for each rod are shown in in Figure 3.15 a). The actual gap distance is shown in in Figure 3.15b), which is obtained by adding position measurement of both rods and subtracting the initial overlap with some filtering to reduce noise. It can be seen that higher velocity of UFD contacts is obtained and the total opening time is reduced to 1.2 ms.



a) Original sensor measurements.

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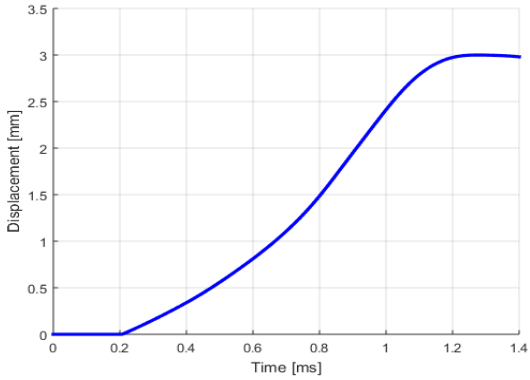

b) Calculated contact gap

Figure 3.15 Contacts displacement of UFD operated with 180 V.

3.3.8 OPERATING CYCLE TIME-CONSTRAINTS

The charging time for the power supply capacitors is about 3s since the employed transformer and diode bridge rectifier have current rating limit. Consequently, there is 3s constraint on the time between each operation of the developed UFD. In practice it may be desired to have open-close-open cycle with smaller time intervals, although standards for DC CBs do not exist yet.

The speed of open-close-open cycle can be enhanced in several ways:

1. The simplest way is to increase the charging speed is by using bigger transformer and rectifier. However, only limited improvement is possible.

2. Introduce another complete driver for the second operation. Hence, for next operation there is a charged capacitor available which can energize the TCs. Depending on the required number of operations, multiple power supplies may be needed.

3. In hybrid DC CBs it is possible to bypass UFD with the main breaker valve. Depending on heat dissipation capability of the main valve, the closing UFD operation can be delayed. This implies that main valve should be capable of conducting rated current while UFD driver is recharged.

3.4 LOAD COMMUTATION SWITCH (LCS) T_1

In high voltage DC CB the required rating of Load Commutation Switch is much lower than the nominal voltage of the DC CB [15]. The ABB load commutation switch employs 3x3 matrix of commercial IGBT's of 3.3kV-4.5kV [15].

The basic rating needed for the LCS switch can be calculated as follows. The maximum current is same as the threshold current set for the fault detection (50A). The voltage rating should be higher than the voltage drop

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across T2 during the fault which very small in the order (50V). However, in the designed prototype a single IGBT with 600V rating is selected since 600V is the minimal voltage for commercial IGBT.

The LCS voltage rating (600V) is much lower that the voltage stress across DC CB (1400V) and therefore UFD plays critical role in isolating LCS as it is the case in the high-voltage DC CB. Therefore this demonstrator will well capture basic stress sharing between components in the hybrid DC CB.

3.5 MAIN BREAKER SWITCH T_2

Totally eight IGBTs connected in series are used as the main breaker T_2. Although in the actual DC CB there will be 200-300 IGBTs in series, this design will enable study of series connected switches and will enable fault current limiting. Once the T2 turns OFF during the fault, the voltage across it goes to 1500V. This voltage would appear across 8 IGBT. The minimum voltage rating requirement for each IGBT is 200V. The peak fault current can go up to 500A. However this current is a short period and is not repetitive. The IGBTs in T2 are rated 600V, 500A.

The HV DC CB will be available as unidirectional or bidirectional version. Bidirectional version has two main valves T2 (one for each direction of fault current) and therefore cost is expected to double compared to unidirectional version. There is no fundamental difference in the principle of operation and therefore it is decided that bidirectional version is not necessary for this demonstrator.

3.6 ENERGY ABSORBER

The arresters are used to protect the IGBT's and absorb stored energy in the series inductor and the line. The arresters are rated such that the clamping voltage of each arresters is lower than the IGBT's nominal voltage. One arrester is connected each of 8 IGBTs in T2. The clamping voltage of the arresters is below the IGBT voltage rating. Additionally the voltage across all the arresters should not be higher than 1500V. The voltage rating of the individual arresters should be around 180V.

The PSCAD simulation results show that the energy dissipation in the arresters during fault clearing is around 870J, which is considered in selecting proper sized arrester. All the components are listed in the Appendix.

3.7 SERIES INDUCTOR L_{DC}

The series inductor limits the fault current rate. The fault current is much higher than the load rating current. Air core inductor is selected, rather than iron-core to prevent the core from saturation. The inductor copper wire (i.e. $10mm^2$) is selected based on the nominal current rating 30A and considering also high fault currents. Fault current duration is very short and the wire can withstand the amount of heat generated during the fault. The inductor is firmly fastened to the frame. The number of turns are calculated based on the equation provided below:

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$$L = \frac{31.49a^2N^2}{6a+9b+10c} \quad (0)$$

Where, L is the inductance of the coil in micro-Henry, N is the number of turns, a, b, and c are the dimensions of the coil shown in Figure 3.16 in meters. The parameters of the inductor are given below:

- The core radius r=0.04m
- Number of turns N=250
- a=0.065m, b=0.15m, c=0.05m
- Calculated L=3.71mH
- Wire size 10mm^2
- The inductance value of the fabricated inductor is 3.5mH.

Figure 3.17 shows the series inductor L_{dc}.

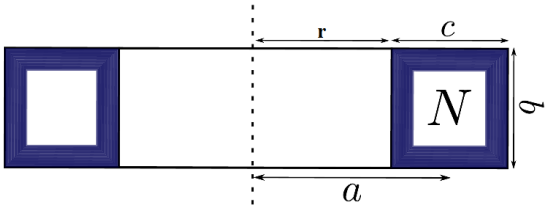

Figure 3.16 The dimensions of multilayer coil.

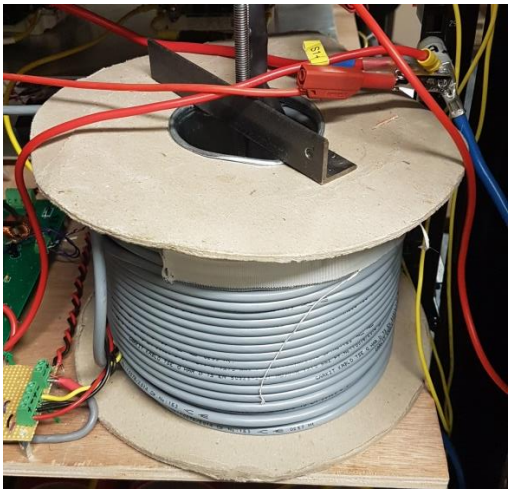

Figure 3.17 Inductor Ldc.

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3.8 RESIDUAL SWITCH S_2

The residual switch should be capable of breaking a small current of around 1A dc at 900V. The residual switch is a dc contactor with operating time of around 20ms. This switch breaks the residual current and prevents the Varistors from dissipating energy. The selected contactor is a Kilovac air sealed 900V/500A (EV200HAANA).

3.9 DC CB CONTROLLER

The DC CB is controlled using a TI DSP TMS320F28335. The overall block diagram of the control circuit is shown in Figure 3.18.

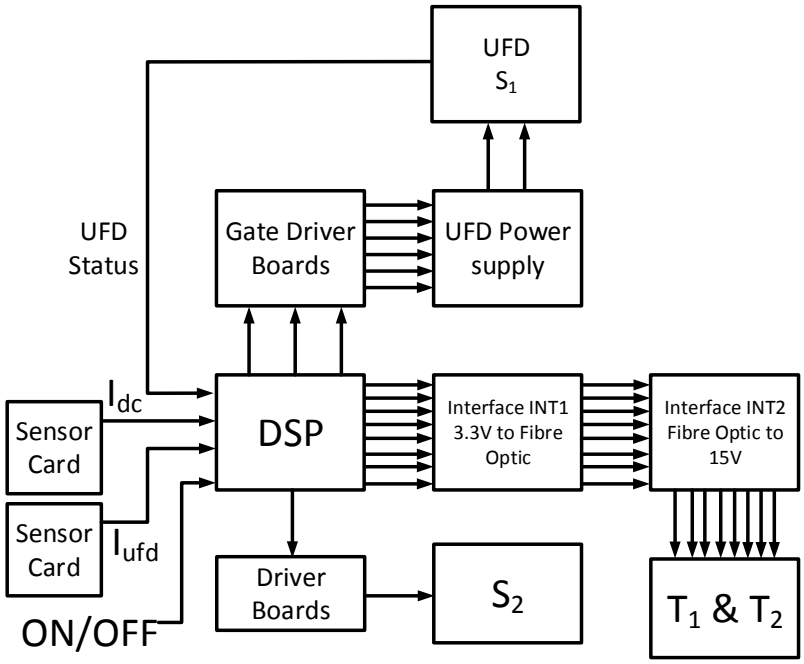

Figure 3.18 The control block diagram of the hybrid DC CB.

The DSP make the decision of opening and closing the DC CB based on the signals that are received.

3.9.1 INTERFACE BOARDS (INT1 AND INT2)

The interface boards (INT1 and INT2) are connected between the DSP and the IGBTs, Interface board 1 is shown in same as with test circuit shown in Figure 7.3 while interface board 2 is shown in Figure 7.6. The output pins of DSP can give a signal of 3.3V. This signal is converted to Fibre optics in INT1. The fibre optics are sent to INT2 and are converted to 15V signal. These signals are then fed to the IGBTs.

3.9.2 S2 AND S1 DRIVER BOARD

S2 needs a 12V input voltage and around 3A inrush current. The driver board receives signal from DSP, amplifies that and fed it to the residual switch S2.

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The S1 operates with 120V and needs a pulse current of few thousands amps. The S1 driver boards receive signals from the DSP and convert them to appropriate signal 0-10V.

3.9.3 FEEDBACKS AND SELF-PROTECTION

The DSP measures three feedbacks Idc, Iufd, and the UFD position. These signals are used in the decision making and self-protection of the DC CB. The fault tripping signal is generated based on the Idc.

The self-protection check some condition and if the conditions are satisfied it proceed with operation. The UFD is only a disconnector and cannot operate under load. Hence, the controller checks the UFD current and if the current is close to zero then it send signal to open the UFD. To prevent damaging T1, the UFD should always be open during the operation of T2. The controller checks the position of UFD before operating the T2. The S1 is residual current breaker and can only operate under a small load. The controller always check the Idc current and if this current is less than the breaking capability of the S2 then the S2 is opened. The complete sequence diagram of DC CB controller is explained and implemented/tested in PSCAD in the report D6.1 [9].

3.10 ENERGY BALANCING IMPLEMENTATION

The energy balancing keeps track of all the energy dissipations in the arresters and tries to insert the arrester with least energy dissipation. This process is particularly important for fault current limiting mode, which is proposed in [5] and studied also in this project in previous deliverable [12].

The energy monitoring is done at every 100µs (f_s=10kHz). To implement the energy balancing, the measurement of current through and voltage across each of the arresters are needed. The number of voltage and current sensors is high, and in particular this becomes issue if the method is adopted for high voltage DC CB. A simpler method is used here which requires only the available current sensor I_{dc} and voltage sensor V_{arr}. Based on the number of arresters inserted (i.e. N), and the gating signal of each IGBTs (i.e. G_{T2i}) the voltage and the current of each arrester are calculated as:

$$\begin{aligned} I_{arri} &= I_{dc}\left(1-G_{t2i}\right) \\ V_{arri} &= \frac{V_{arr}}{N}\left(1-G_{t2i}\right) \\ P_{arri} &= V_{arr} \times I_{dc} \\ E_{arri} &= \int_0^t P_{arri}\,dt \end{aligned} \tag{0}$$

where i denote the i^{th} arrester. This method is valid with the assumption that all the arresters are identical and have the same thermal characteristics. In our hardware testing, the accuracy of this method has been verified by measuring temperature on individual arresters.

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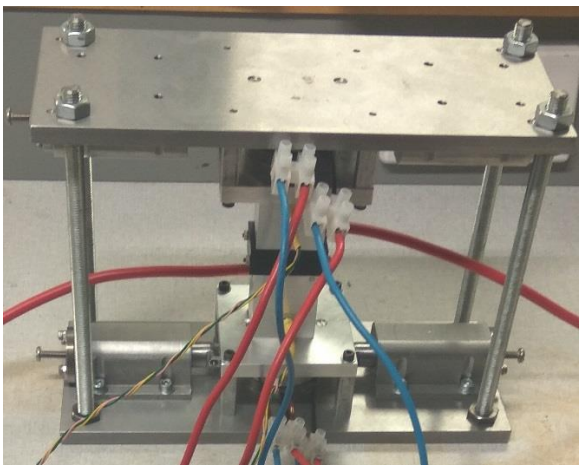
One arrester is placed across each IGBT and Figure 3.19 shows the photograph.

3.11 EXPERIMENTAL VERIFICATION

The hybrid DCCB is firstly modelled in PSCAD in previous deliverables as shown in [11] and [21] but PSCAD results are not repeated. The controller is extensively tested on RTDS model from [11] before proceeding to experimental tests. RTDS has enabled fast tuning of energy balancing controller and the overall controller without risking component damage.

A range of experimental tests have been carried out on the hybrid DC CB. The results are summarised in this section. The fabricated hybrid DC CB is shown in Figure 3.19. The components are listed in Table VI-Table XII.

(a)



(b)

Figure 3.19 Fabricated Hybrid DC CB. (a) the CB main breaker T1 and arresters, (b) the UFD.

3.11.1 TESTING THE DC CB FOR RATED FAULT CURRENT (900V AND 500A) WITH CONVENTIONAL CONTROL

The DC CB has been tested at rated fault current. The fault is created using the fault thyristors at time t=0. The results are shown in Figure 3.20. The UFD current is shown in Figure 3.20(a). The trip signal is generated once the current passes 40A. At this time the fault signal is sent to the controller. The trip signal is received at t=0.2ms. At this time, the fault current has reached 50A, the LCS is turned OFF and the current commutates to T_2. Once the current in the UFD is below the residual current, the UFD is commanded to open. The controller waits until the UFD is open completely (2ms) and then switch OFF all the IGBTs in T_2. This is shown in Figure

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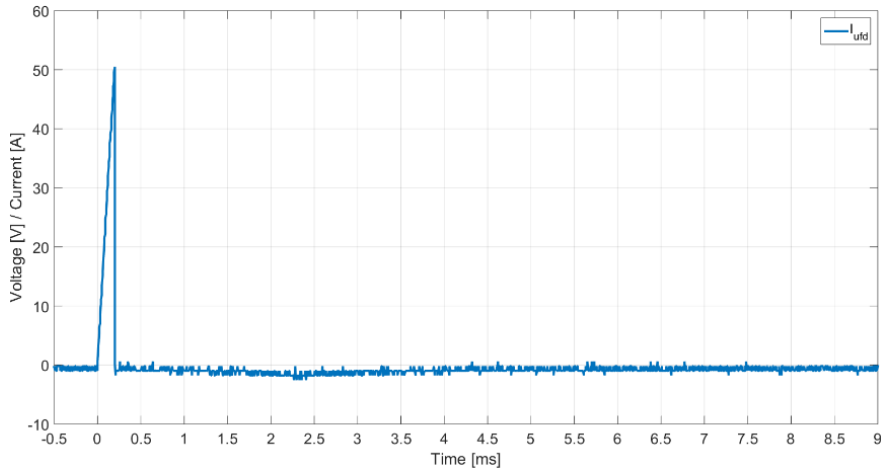
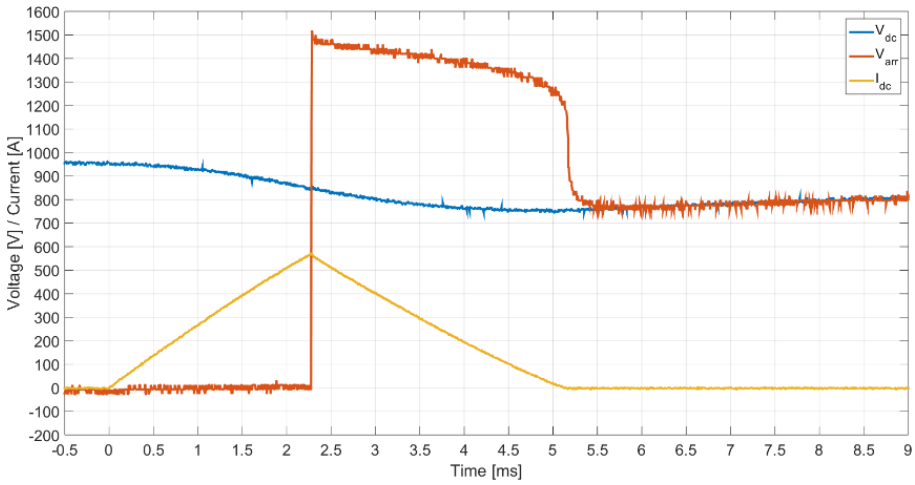
3.20(b). Dc voltage V_{dc}, arrester voltage V_{arr} and dc current I_{dc} are shown in Figure 3.20(b). The IGBTs in T_2 are turned OFF at t=2.275ms. This results in insertion of all the arresters in the circuit. At this time the fault current has reached 575A. Once the arresters are inserted the fault current decays to zero. During this period the arrester voltage increases to 1.6pu (1pu=900V), as seen in Figure 3.20(b). Once the fault current reduces below the residual current the RCB is turned OFF.

The figure also illustrates operation of the test circuit at rated fault current. The initial capacitor voltage is around 980V, which drops to 750V as capacitor supplies energy during the fault clearing. When fault is cleared the controller regulates the DC voltage to 900V which enables DCCB voltage stress withstand testing just after opening.



(a)



(b)

Figure 3.20 DC CB opening at rated fault current. (a) UFD current, (b) dc voltage, arrester voltage, and dc current.

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3.11.2 DC CB OPERATION AT LOW CURRENT

The DC CB is opened at normal load current (28A) in this test. The results are shown in Figure 3.21. The UFD current and the dc current are shown in the figure. There is a small difference in the current level in UFD current and the dc current. This is because the dc current consists of UFD current and the T_2 current, and small current is passing through the T_2. This will show that the on state resistance of the normal branch is much lower than the main breaker branch. In a high voltage installation, T2 would consist of many more IGBTs and T2 current would be considerable smaller than T1 in closed state.

The IGBTs in T_2 are turned OFF at time t=0. Resulting the current decaying to zero.

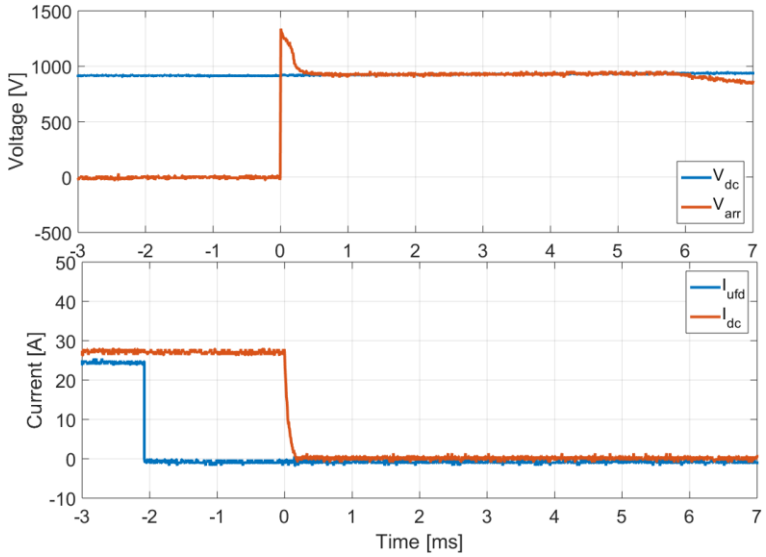

Figure 3.21 DC CB operation at normal load current.

3.11.3 DC CB OPERATION WITH DIFFERENT VALUES OF L_{DC} ($7mH$)

The size of current limiting inductor L_{dc} has been increased to twice the original value (7mH). The DC CB has been tested at full voltage. The experimental results are shown in Figure 3.22. It can be seen that the DC CB successfully clears the fault. In this case the fault current only reaches 300A, since inductor L_{dc}, is twice the size, while opening time is the same.

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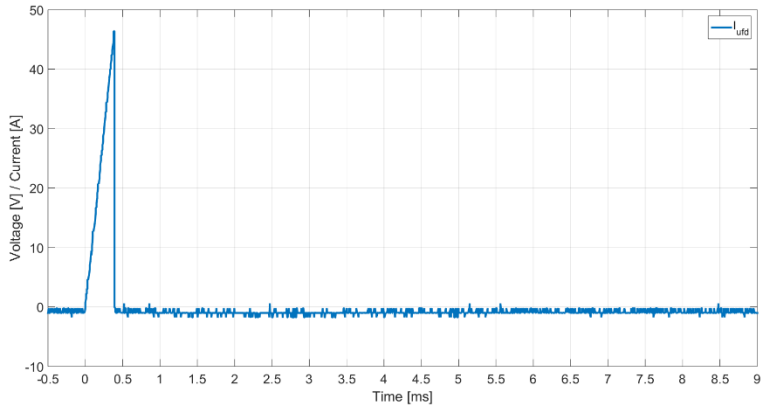
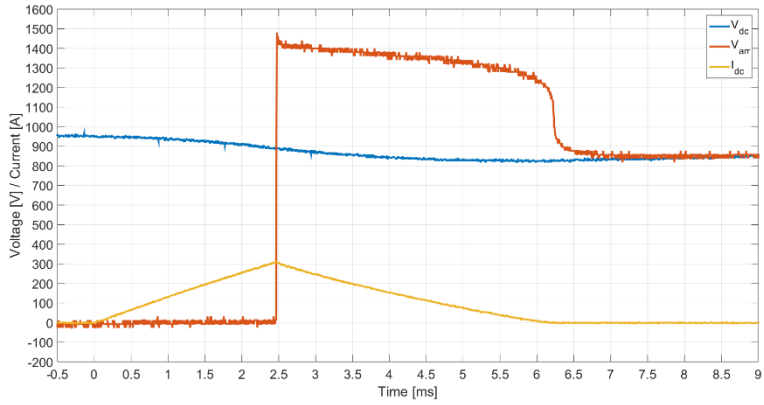


(a)



(b)

Figure 3.22 DC CB fault clearing with L_{dc}=7mH. (a) UFD current, (b) dc voltage, arrester voltage, and dc current.

3.11.4 DC CB RECLOSURE OPERATIONS

The reclosing is one of the important features of protection systems. The reclosing is also important for dc grid so that in case of temporary fault the system can be restored as early as possible. Two parameters are important in the reclosing procedure.

1- Number of reclosing operations (Rn).

2- Time between each reclosure (ΔT1, ΔT2, …, ΔTn).

Three different case are considered here with 3 different delays.

3.11.4.1 DC CB PERMANENT FAULT CLEARING WITH THREE RECLOSURE WITH 0.01S DELAYS BETWEEN EACH RECLOSURE

The CB has been coded to reclose three times with 10ms delay between each reclosure. A permanent fault test has been carried out on the hybrid DC CB. The results are shown in Figure 3.21. The fault is initiated at time t=0. The fault signal is shown in in Figure 3.21 c).

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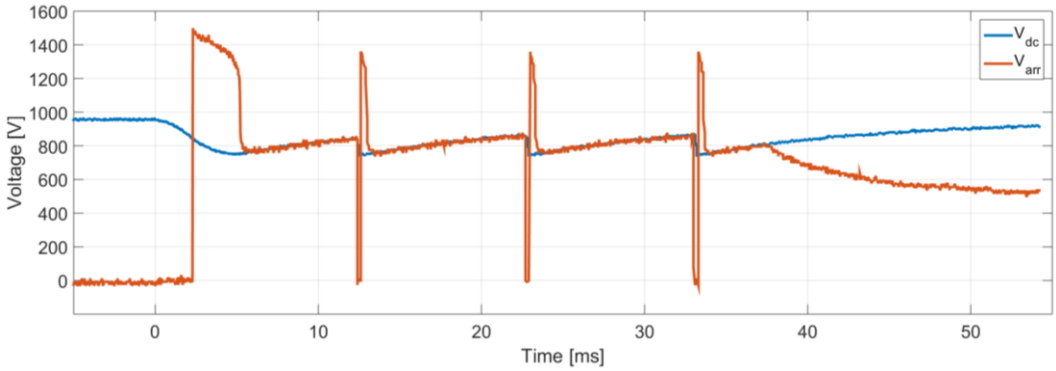
Once the fault is initiated the current rises and when the fault is detected the LCS is turned OFF. When LCS current drop to zero, the UFD is commanded to open. The UFD takes around 2ms to open. During this time the fault current rises to 575A. Once the T2 turns OFF, the current decays to zero and UFD remains closed. Then the controller tries to turn ON T2 after 10ms. As soon as the T2 is ON the fault current starts rising. Once the current reaches the current threshold, T2 turns OFF. This happens for the number of reclosing Rn set by the user.

The fault current during the reclosing is quite low compared to the fault current in first opening. This is because during the reclosure the UFD remains opened, and the opening time of T2 is very short (in µs range). This is demonstration of the expected operating regime of actual hybrid DC CBs and it has been discussed in some depth in [9] and [11]. Transistors in the main valve are capable of taking load current for short time while re-closures are attempted.



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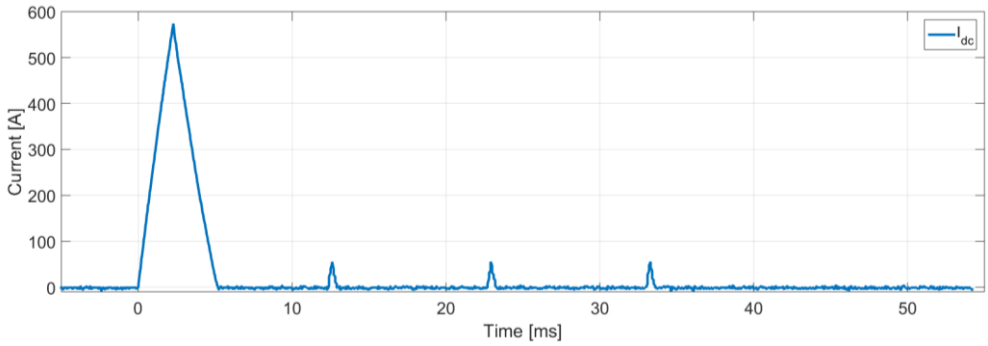

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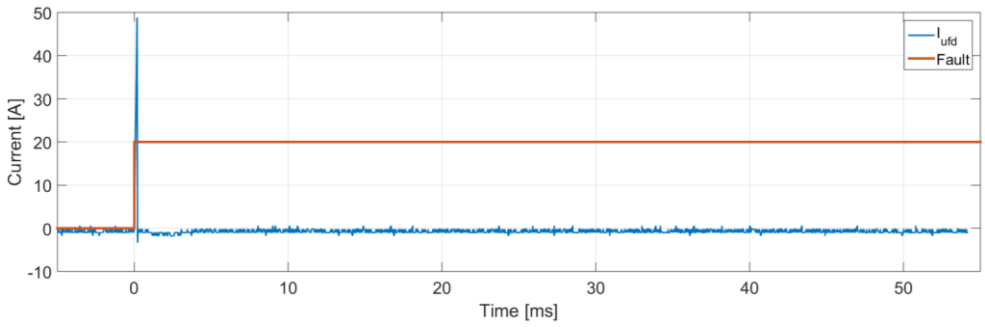

(c)

Figure 3.21 DC CB fault clearing with reclosing. (a) DC and arrester voltage, (b) DC current, (c) UFD curret and fault signal.

3.11.4.2 DC CB PERMANENT FAULT CLEARING WITH THREE RECLOSURE WITH VARIABLE DELAYS BETWEEN EACH RECLOSURE

The CB has been coded to reclose three times with 10ms, 20ms, and 50ms delays between the first, second and third reclosure respectively. A permanent fault test has been applied and therefore DC CB moves to final open state. The results are shown in Figure 3.22. The fault is initiated at time t=0. The results are similar as in the previous test but the second time the controller switches T2 ON after 20ms and proceeds to open immediately since fault still exists. In the third reclosure the controller waits for 50ms and turn T2 ON. Since fault still exist the controller proceeds to open the CB completely. In this case also, the number of reclosing Rn and the time between each reclosings can be set by the user.

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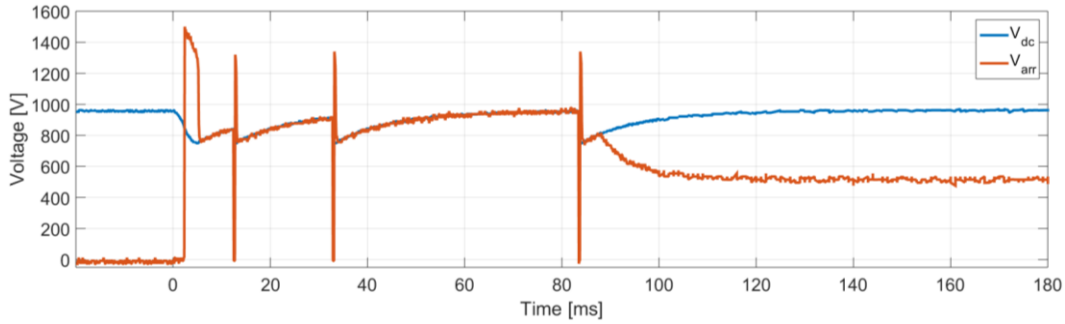

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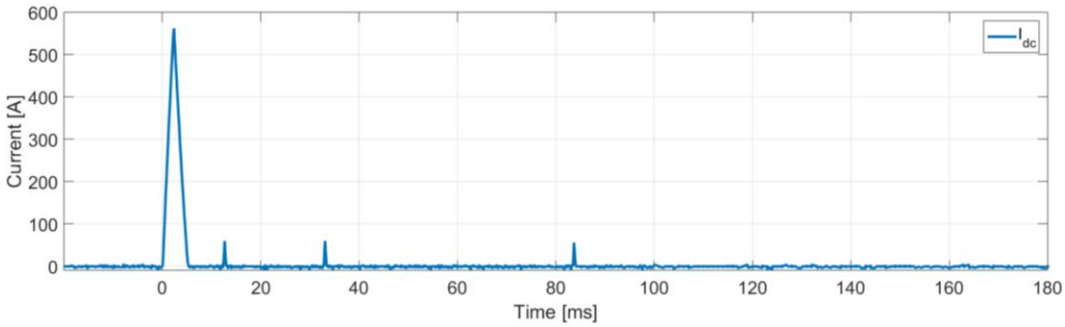

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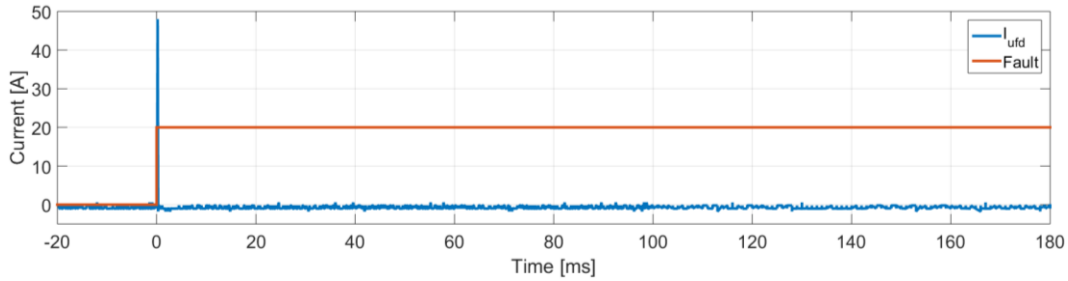

(C)

Figure 3.22 DC CB fault clearing with variable time reclosing. (a) DC and arrester voltage, (b) DC current, (c) UFD curret and fault signal.

3.11.4.3 DC CB TEMPORARY FAULT CLEARING WITH RECLOSURE

A temporary fault test has been carried as shown in Figure 3.23. The fault is initiated at time t=0 and removed at around 38ms as shown in the lower graph of Figure 3.23. The controller is set to reclose firstly after 10ms, then after 20ms and then for the last time after 50ms. After second opening the fault is cleared (labelled in Figure 3.23 as 1) and once T2 is turned ON for the third time it will stay ON (labelled in Figure 3.23 as 2).

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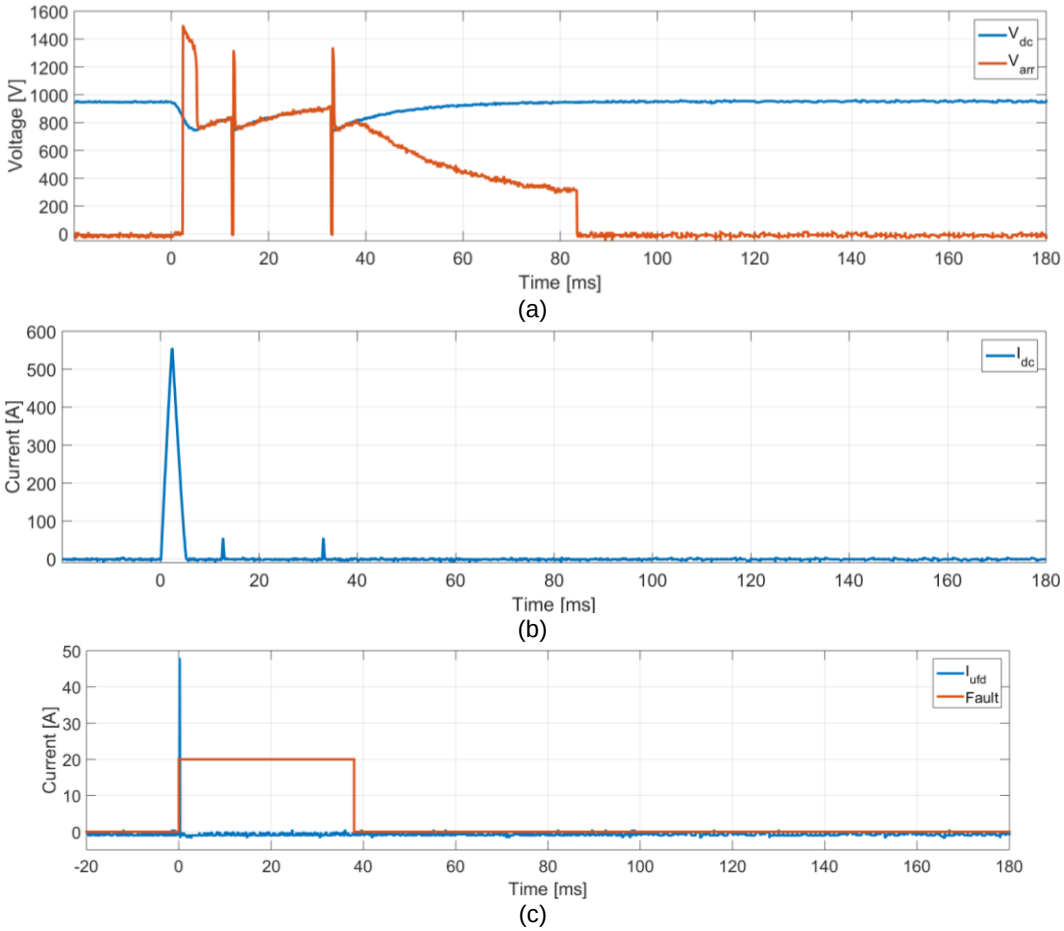

Figure 3.23 DC CB temporary fault clearing with variable time reclosing. (a) DC and arrester voltage, (b) DC current, (c) UFD curret and fault signal.

3.11.5 TESTING THE HYBRID DC CB WITH THE NEW UFD VOLTAGE CONTROL METHOD AND FAULT CURRENT LIMITING

The hybrid DC CB is capable of achieving fault current limiting since it can control individually each switch in the main valve [5]. This operating mode has been studied in some depth in other tasks in this project [12], [30] and the hardware demonstration has been explained.

The hardware hybrid DC CB demonstrator has been used also with the proposed UFD voltage control while its contacts are moving which is explained in [12] and [23]. This method inserts arresters one at a time to gradually increase voltage across UFD, and this enables early insertion of DC CB voltage which leads to fast reduction in fault current. The method includes substantial theoretical studies and simulation verification in addition to experimental results.

Figure 3.24 shows the experimental confirmation of voltage control of ultrafast disconnector. It is seen that hybrid DCCB demonstrator enables gradual voltage control in the 2ms interval while contact are moving apart, and this results in lower peak fault current. For ease of reference the whole study with all experimental results is presented in [12] and it is not repeated here.

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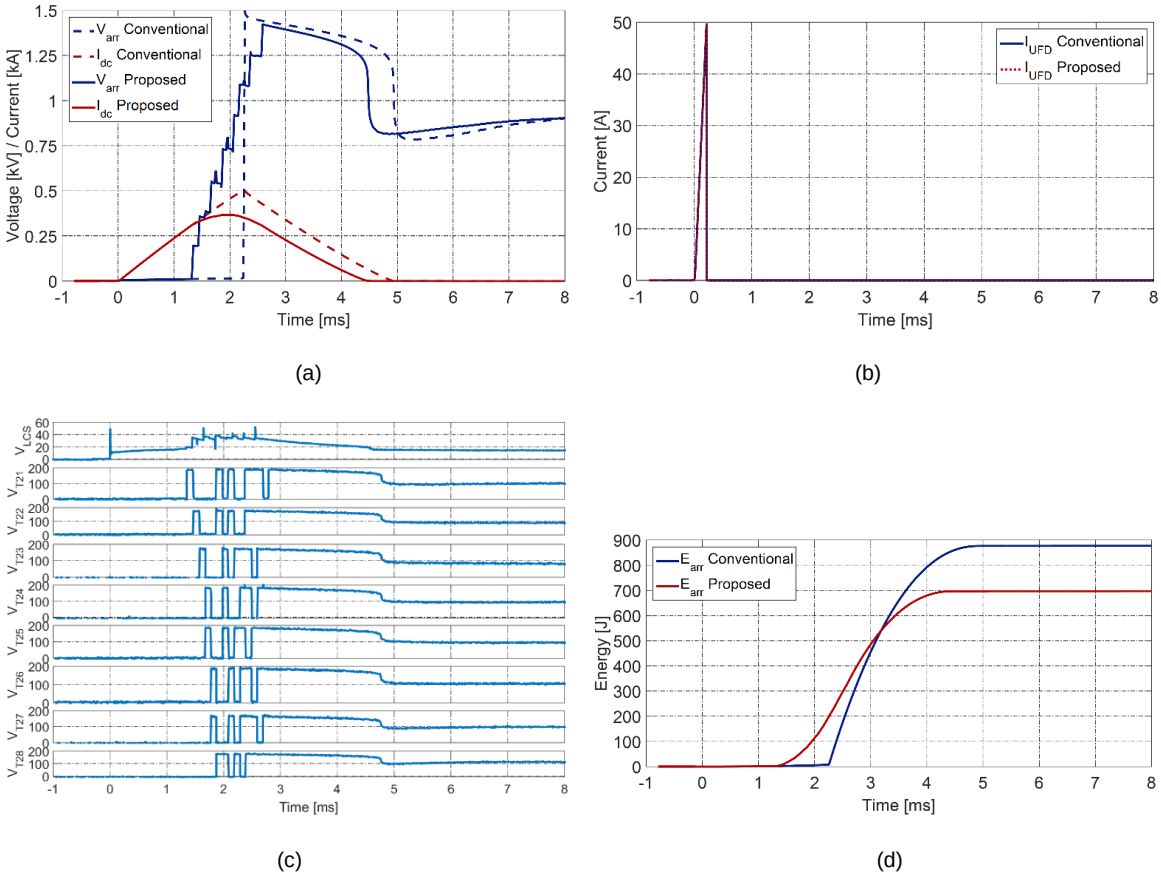

Figure 3.24 DCCB experimental results with conventional and proposed controls. (a) Arrester voltage and dc current, (b) UFD Currents, (c) Voltage across IGBTs in T1 and T2, and (d) total Energy in surge arresters.

Figure 3.25 shows the experimental results with integrated voltage control and fault current limiting. While contacts are moving the voltage control is used, and then the controller moves to fault current limiting and keeps fault current at 30A (1pu). The details of this control are provided in [12].

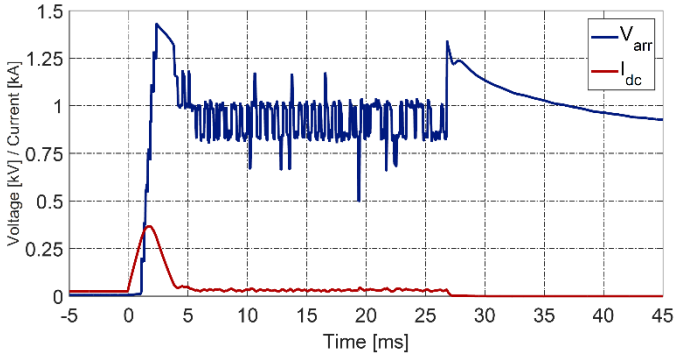

Figure 3.25 Experimental results of integrated UFD voltage and dc current control

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4 MECHANICAL DC CB DEMONSTRATOR

4.1 INTRODUCTION

The mechanical DC CBs for HVDC applications have been known for over 30 years but the original designs used passive resonance which suffered long operating time [24].

The latest mechanical DC CB designs [8], [25], are based on current injection technology, and they are particularly attractive for future DC grid applications since operating speed is reasonable (5-10ms) while costs are expected to amount perhaps to several percent of the VSC converter costs. The basic operating principle of the current injection DC CBs is well understood, but there has been very little publically reported research on the technology. In particular, there are no experimental results reported by independent research centres.

The goal of this research project is to analyse: design, operation, component stresses, power scaling and failure modes on a laboratory-scale DC CB demonstrator with ratings of around *500A* and *1000V.* This chapter reports on the first stage of the project, describing the developed DC CB demonstrator, design choices, and it presents successful tests on interrupting both rated DC current and lower fault current. PSCAD modelling will be used in design stage. Some further details are given in [26].

4.2 DESIGN REQUIREMENTS

The mechanical DC CB demonstrator should be designed that it meets the given requirements below:

1- The topology should closely represent the high power mechanical DC CB with reduced current and voltage level. The concept of operation also should be the same as the high power DC CB [27].
2- The demonstrator mechanical DC CB should be capable of interrupting a peak fault current in the range of 500A.
3- The rated voltage of the demonstrator mechanical DC CB should be of the order of 900V to 1000V. The transient recovery voltage will be much higher.
4- The resonance circuit should be designed such that the S1 current during the fault interruption has multiple zero crossing. The resonant frequency should be around 3kHz in agreement with high power designs.
5- The amount of energy dissipation in the surge arresters to be in the range of 1000-2000J.
6- The speed of operation should be around 5-10ms.

4.3 DEMONSTRATOR MECHANICAL DC CB TOPOLOGY

The mechanical CB topology is shown in Figure 4.1. It represents the actual demonstrator which has some differences compared with [25][27] as explained in the sections below. The normal current path is through the switches S1, S2, and inductor L_{dc}. As there are no natural current zero crossing during the DC fault, in order to

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force current zero crossing a resonance circuit consist of L, C, and the switch S3 is introduced. In this configuration the capacitor of the resonance circuit is pre-charged using a permanent charging resistor R_{ch} and hence, there is no need for external charging circuit.

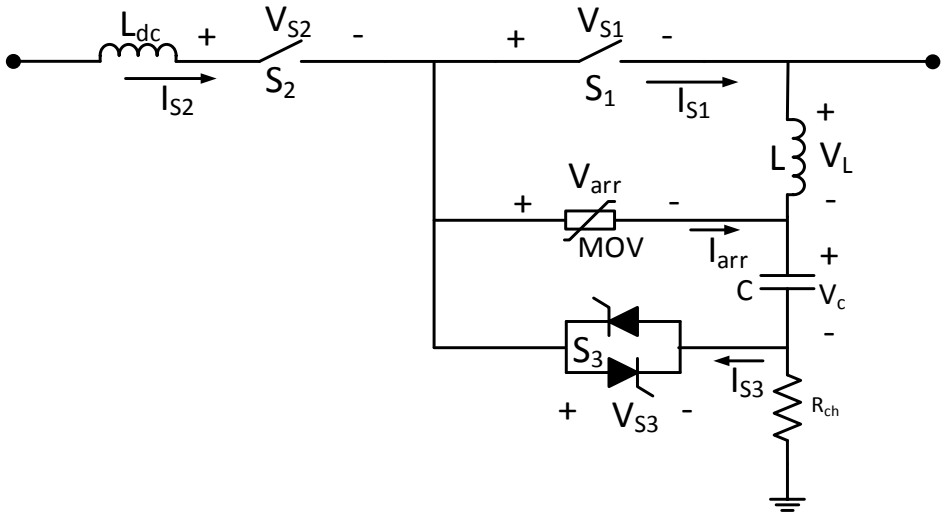

Figure 4.1. The developed mechanical DC CB topology.

4.4 OPERATING SEQUENCE

4.4.1 CLOSING

In closing operation S2 is closed first. After a delay of 15s the S1 is closed. This long delay is required to let the resonance capacitor C charge up. By closing the S2 the charging path is closed.

4.4.2 OPENING

In opening operation, the S1 is commanded to open first. By opening the S1, it starts arcing. The resonance circuit is activated by turning the S3 ON. The resonance current creates a current zero crossing in the S1 and S1 stops conducting. The remaining large DC current from L_{dc} is commutated to arresters. Once the current in S2 is lower than the residual current, the S2 is commanded to open.

4.5 COMPONENTS AND PARAMETERS OF THE MECHANICAL CB DEMONSTRATOR

4.5.1 THE MAIN SWITCH (S1)

The main switch opens first when the fault current is passing through the CB. The S1 arcs from the instant when it's contacts become separated until the resonance current create the current zero crossing. Hence, the switch

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S1 should be capable of withstanding the arc. However, this arcing is for a short duration of few milliseconds. The voltage and current rating of the S1 should be equal to transient recovery voltage which is normally 50% higher than the nominal DC voltage.

It has been quite challenging to locate a switch with required operating speed and ratings. In the HV DC CB vacuum switch is used but they are only available in middle voltage range and are not available at voltages of around 1kV. Also vacuum switches have quite slow driving mechanism and it would be beyond university capability to upgrade driving mechanism on a commercial switch. Furthermore the cost of commercial MV vacuum interrupter would be beyond project budget.

We have finally selected Kilovac, 900V, 500A, air-sealed EV200HAANA contactor. The test in laboratory demonstrated opening speed (time for contacts to begin separation) of around 3.2ms as shown in Figure 4.2. The travel time for the contacts has not been determined.

At the rated voltage of 900V this contactor is capable of interrupting around 70A DC current with 300μH inductive load (manufacturer data. The interruption capability of the contactor reduces as the load becomes more inductive further leading to a prolong arcing time.

It was necessary to connect 3 contactors in series (S_{1a}, S_{1b} and S_{1c}) in order to provide required current and voltage rating. We have confirmed experimentally that characteristics of operating mechanism could vary notably with these mechanical switches, and this results in an unequal sharing of the voltage across 3 units. We have connected grading resistors R_g =7.5kΩ and capacitors C_g =50nF in parallel with each unit, according to methodology in [29]. The final parameters and the datasheet for S1 are given in the Appendix.

The fast that an air switch is used in this demonstrator will imply some differences compared with the HV design with vacuum switches. Firstly, the arc voltage is substantially higher with air switches. Also, as a consequence, heat dissipation is much larger. Furthermore, the critical current derivative for successful interruption is higher in vacuum switches.

4.5.2 THE RESIDUAL SWITCH (S2)

The residual switch does not open if its current is higher than the residual current (few amps). It opens once S1 has opened and the fault current is neutralized. Hence, S2 needs to be rated such that it is capable of breaking residual current. The selected residual switch is a single Kilovac switch (same as S_1). The voltage rating should be nominal DC voltage.

4.5.3 THE CURRENT INJECTION SWITCH (S3)

This switch closes the resonance circuit and creates current zero crossing in S1. In HV DC CB case a similar vacuum switch as S1 is employed and the making time of S3 (measured from the moment the coil supply is switched on to initial contact of the main poles) is adjusted to be same as the opening time of S1 (measured from the moment coil supply is switched off to the moment the main poles separate) . The operation timing of the Kilovac contactors (used for S1) are shown in Figure 4.2. It can be seen that the opening time is around

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3.2ms, however the closing time for the contacts is 16ms. Hence, this switch cannot be used as S3. It was not possible to locate a commercially available mechanical switch with such short closing time and therefore decision was made to use back to back thyristors. A 75A, 1600V thyristor is selected. Also, thyristors enable precise control of injection timing, which is important for research studies. The voltage rating of the thyristors should be nominal DC voltage.

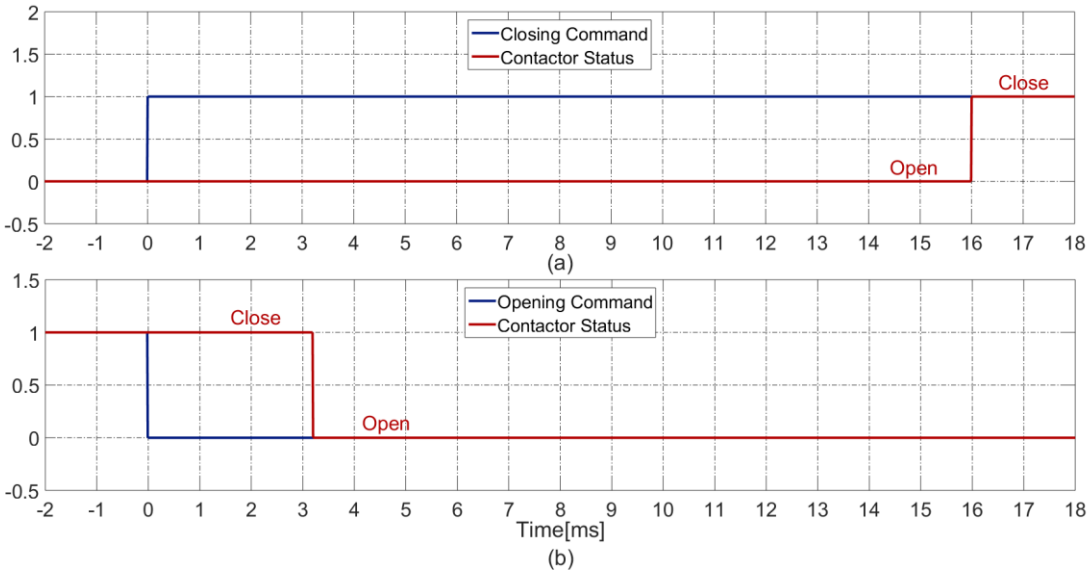

Figure 4.2 Measured operating timing of the Kilovac contactor.

4.5.4 SURGE ARRESTER (MOV)

Once the S1 is open and the current crosses zero, the fault current commutates to arresters. The arresters are selected such that the voltage overshoot during the fault current neutralization is in the range of 1.5pu. Another criterion is that the residual current in the surge arrester, with voltage of 1pu, should be sufficiently low to avoid thermal runaway, and less than the residual current of S2. Also, arresters must be selected properly so that they can sink all the energy without excessive heating in the arresters. The selected arresters are similar as hybrid DC CB (energy is different) 4x EPCOS B72260B0131K001 (170 Vdc).

4.5.5 LIMITING INDUCTOR (L_{dc})

During the fault, the current limiting inductor L_{dc} limits the current derivative. With a dc voltage (V_{dc}), peak fault current (I_p), the trip level current (I_{tr}) and opening time of S1 (t_{op}), the L_{dc} can be calculated as:

$$L_{dc} = \frac{V_{dc} \times t_{op}}{I_p - I_{tr}} = \frac{900 \times t_{op}}{500 - 50} \quad (1)$$

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Where $V_{dc} = 900V, I_p = 500A, I_{tr} = 50A$.

For the values above, the required values for L_{dc} is plotted versus different values of operating time (top) in Figure 4.3. If the operation time is considered to be 4ms the inductor size needed is 8mH.

The current limiting inductor consists of two air core inductors connected in series with parameters given below

- The core radius 0.04m
- Number of turns 250
- Calculated inductance 3.71mH
- Wire size 10mm^2
- Current rating 50A

Each inductor is identical as the inductor with hybrid DC CB, Figure 3.17.

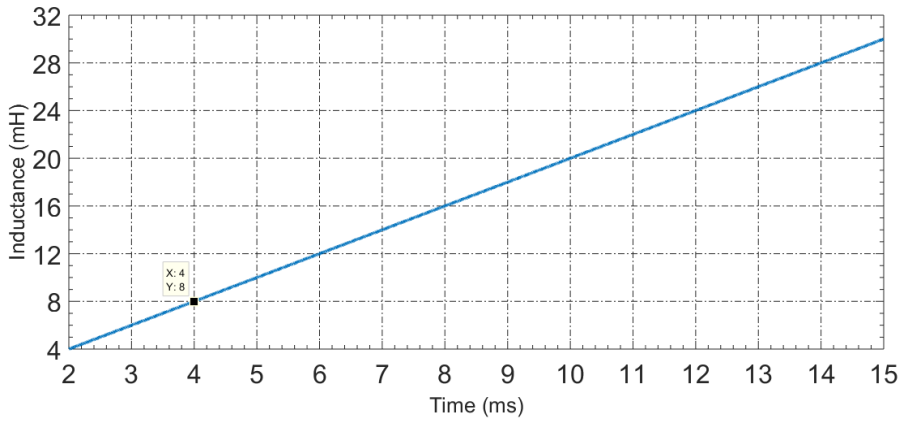

Figure 4.3. The limiting inductor value versus the operating time of S1.

4.5.6 THE RESONANCE CIRCUIT

The resonance circuit generates a counter current in S1 and creating a current zero crossing in S1. It consists of a capacitor C and an inductor L. The components L and C should be designed such that the peak resonance current is higher than the fault current with some reasonable margin. The frequency of the resonance should be in the range of 3 kHz (as used by the manufacturer in high-power designs). Low resonance frequency results in delayed operation, while very high resonance frequency will generate high di/dt and the interrupting would not be possible.

The resonant frequency is important in two aspects:

1. It determines di/dt which has impact on probability of current interruption. Critical current derivative depends on many factors including the insulating medium. Since HV DC CBs use vacuum interrupters, the results with air interrupters will be different.

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2. If has influence on the operation of the resonant circuit. The functioning of the resonant circuit depends on the frequency, initial current value, internal damping caused by parasitic and the ratio between L and C. In this aspect the demonstrator can support best analysis if the frequency is similar as in HV DC CBs. It is understood that internal damping will be different, but the relative impact of various parameters will be retained in the demonstrator.

In the task 6.6 the resonant circuit parameters LC will be varied and their impact will be analyzed in more depth.

The frequency of the oscillations depends on the values of L and C as:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{2}$$

The inductance versus capacitance for the resonance frequency of 3 kHz is shown in Figure 4.4.

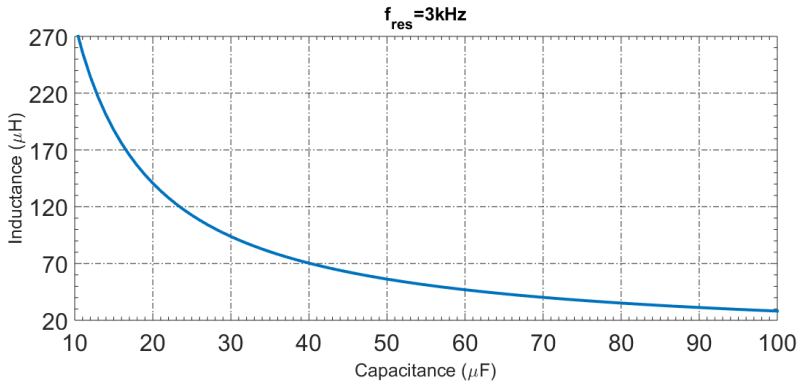

Figure 4.4. Inductance vs. capacitance of the resonance circuit for 3 kHz.

When the switch S3 is closed the resonance current is the same as the current in switch S3. It is essential to accurately analyse this resonant circuit since this determines existence and number of zero crossings. Zero crossings will depend on the peak of initial current, which in turn depends on the size of LC. High initial pulse is desired, but to high value may lead to excessive stress on components.

The equivalent circuit when the S3 is closed and S1 is trying to open is as shown in Figure 4.5. where V_{C0} is the initial capacitor voltage, R_{eq} is the parasitic resistance in the current path, L is the inductor of the resonance circuit, and I_{S3} is the current through switch $S3$

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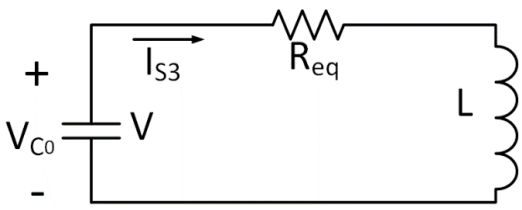

Figure 4.5. The resonance equivalent circuit when the S3 is closed and S1 is trying to open.

The current I_{S3} can be calculated using LRC circuit equation as follows:

$$\frac{V_{C0}}{s} = \frac{I_{S3}}{Cs} + R_{eq} I_{S3} + L I_{S3} s \tag{3}$$

Where the V_{C0} is the initial capacitor voltage, and the R_{eq} is the parasitic resistance in the current path, while other variables are shown in circuit figures. Rearranging (3) results in (4).

$$I_{S3} = V_{C0} \frac{\frac{1}{L}}{S^2 + \frac{R_{eq}}{L} s + \frac{1}{LC}} \tag{4}$$

The LaPlace domain equation (4) is solved in time domain is given below:

$$I_{S3} = V_{c0} \frac{\sin(\alpha t) e^{-\frac{R_{eq}}{2L} t}}{\alpha L}, \quad \alpha = \frac{\sqrt{4L - C R_{eq}^{\,2}}}{2\sqrt{C}\, L} \tag{4}$$

The resonance current for the given values is shown in Figure 4.6. Considering the experimental responses, the value for parasitic resistance is selected as R_{eq}=0.05Ω. The parameters (L and C) are selected such that the peak resonance current is about 1000A, which is twice the DC CB breaking current (I_p=500A).

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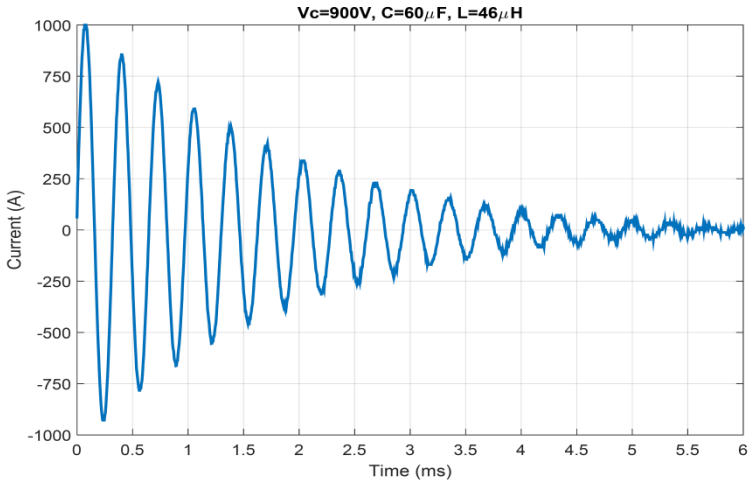
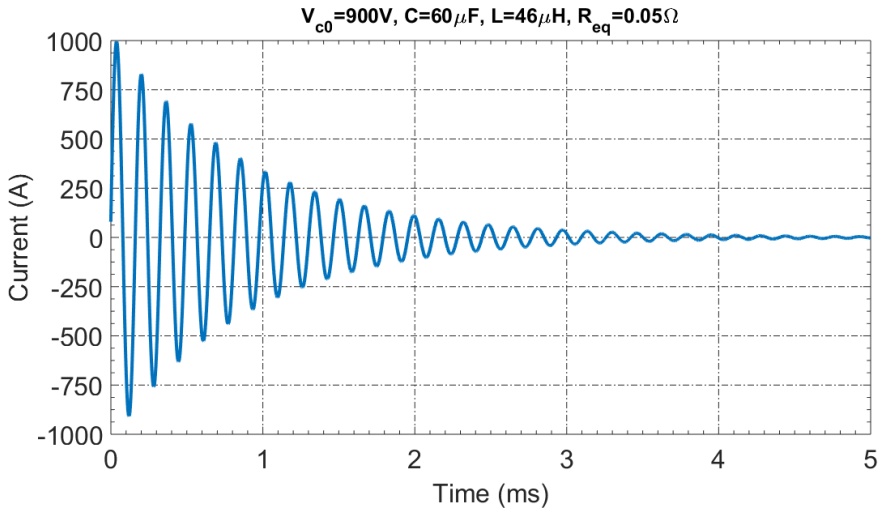


a) Measured on demonstrator



b) Simulated on PSCAD

Figure 4.6. The resonance current.

It can be seen in (4) that the peak current is dictated by the term $V_{c0}/\alpha L$, which is plotted in Figure 4.7 for different values of L and C in. It can be seen that the value of $V_{c0}/\alpha L$ is high for higher C and lower L.

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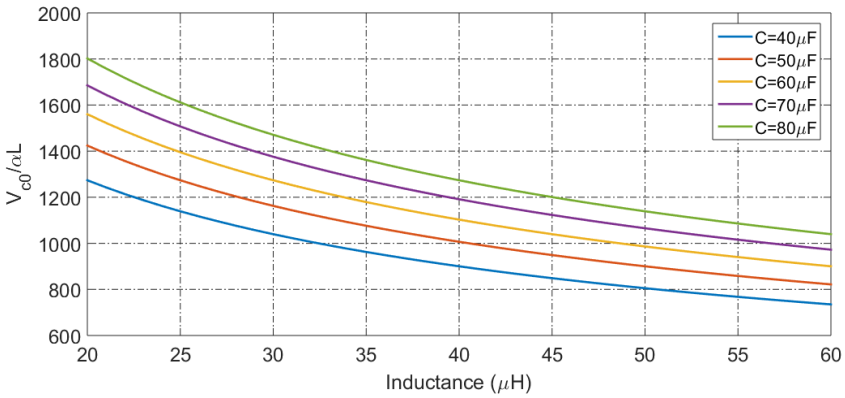

Figure 4.7. The term $V_{c0}/\alpha L$ for different values of L and C.

However it is not possible to select very low L, as this determines the decaying of the current, which can be observed by the damping factor ($e^{-\frac{R}{2L}t}$) in (4). Low damping is required to enable multiple current zero crossings which improve reliability. The magnitude of the transient oscillating response (damping factor values) for different values of R/L are plotted in Figure 4.8. It can be seen that, to have a low damping factor we need to reduce ratio R/L. Since it is not possible to manipulate R this is done by increasing the inductor size L.

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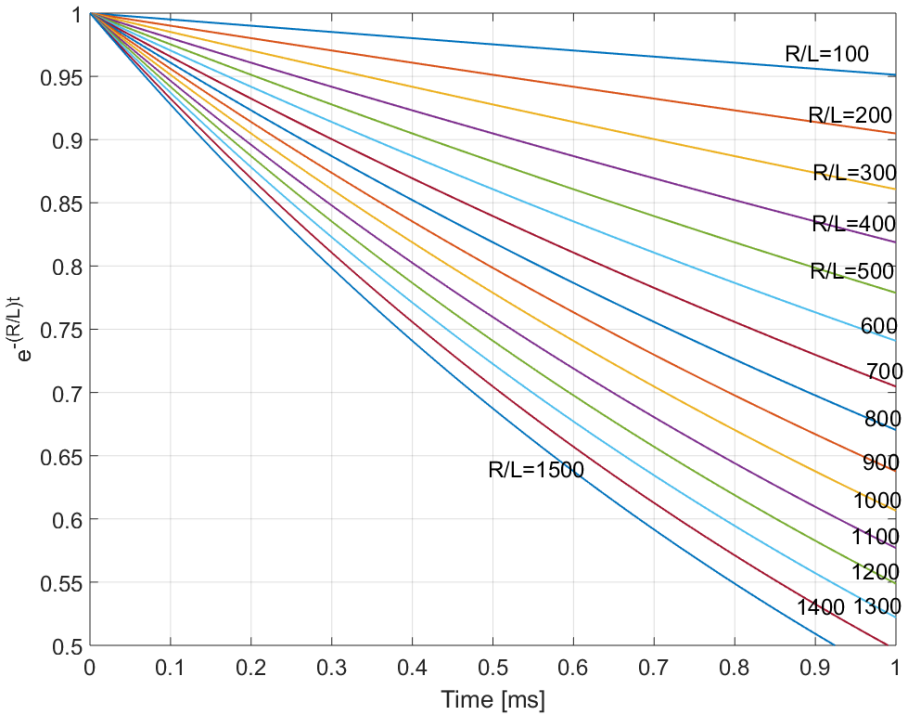

Figure 4.8. Time-domain response of damping factor $\left(e^{-\frac{R}{2L}t}\right)$ for different values of $\frac{R}{L}$.

The Selected value for the resonance capacitor is 60µF. The capacitor peak voltage reaches 1400V, and therefore the capacitor voltage rating should be 1500V. Aluminium film capacitors are used so that it can pass the required high current (the resonance current rating is in the range of 1000A).

The resonance circuit inductance is selected as 46µH. The inductor voltage rating is 1500V. High current is passing through the inductor for a short time hence air core inductor is used where high current density is allowed for short time period.

4.5.7 CAPACITOR CHARGING

A charging resistor is used to charge the resonance circuit capacitor. The charging resistor should be high so that during the fault the capacitor does not discharge through the fault. Also heat dissipation should be limited. The selected value for the charging resistor is 50kΩ. This results in charging time of around 10s.

4.6 THE DC CB CONTROLLER DESIGN

4.6.1 CLOSING PROCESS

The closing process of the mechanical CB is explained here and the control sequence is depicted in Figure 4.9.

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1- Upon closing command swithch S2 is firtsly closed and then S1. In our test system load is passive and the capacitor charging can only be achieved if S2 and S1 are closed. In practice lne will be enrgised in most cases and therfore charging can be achieved from the line side.
2- The capacitor is charged during the interval of 10s. After the delay the DCCB is reday for operation.

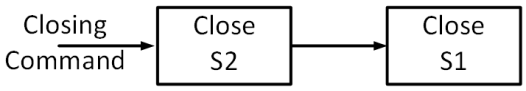

Figure 4.9. Closing control sequence of the mechanical CB.

4.6.2 OPENING PROCESS

The opening control sequence is depicted in Figure 4.10.

1- On receiving the opening signal the switch S1 is commanded to open.
2- The S3 is turned ON after a time of t_{op} so that the S1 contacts are open and the current zero crossing is created by resonance current.
3- The switch S2 is opened once the dc current is lower than the residual current.
4- The swith S3 gate pulses are turned OFF.

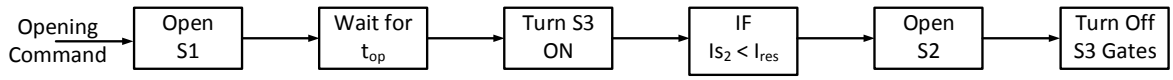

Figure 4.10. Opening control sequence of the mechanical CB.

4.7 PSCAD SIMULATION

4.7.1 PSCAD SIMULATION PARAMETERS

A detailed PSCAD model of DC CB is developed in order to study operation and component stresses [11]. The PSCAD model parameters are listed In Table 3. The results from PSCAD simulation will be used to finalise ratings of components and to confirm operation.

Table 3 the parameters used in PSCAD.

V_{dc}=900V	L_{dc}=8mH
I_p=500A	L=46μH
$_{Itr}$=50A	C=60μF
I_{load}=25A	R_{eq}=0.15Ω

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R_{load}=35 Ω	R_{ch}=100 Ω
T_{op}=4ms	
S1 close delay= 20ms	S2 close delay= 40ms
S1 open delay= 4ms	S2 open delay= 40ms

4.7.2 CLOSING WITH POSSITIVE CURRENT

The PSCAD simulation results are presented for closing the CB at positive current. The control signals of the DC CB are shown in Figure 4.11.

The CB currents are shown in Figure 4.12 and respective CB voltages are shown in Figure 4.13.

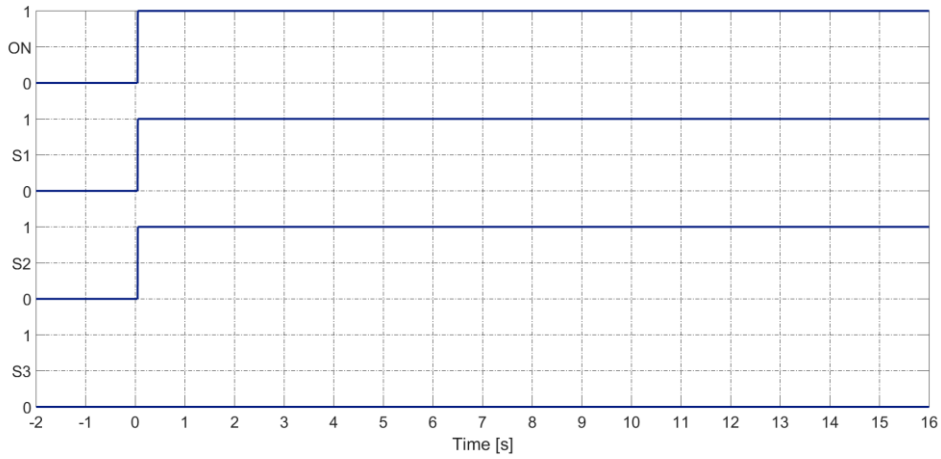

Figure 4.11. The control signals of DC CB during closing.

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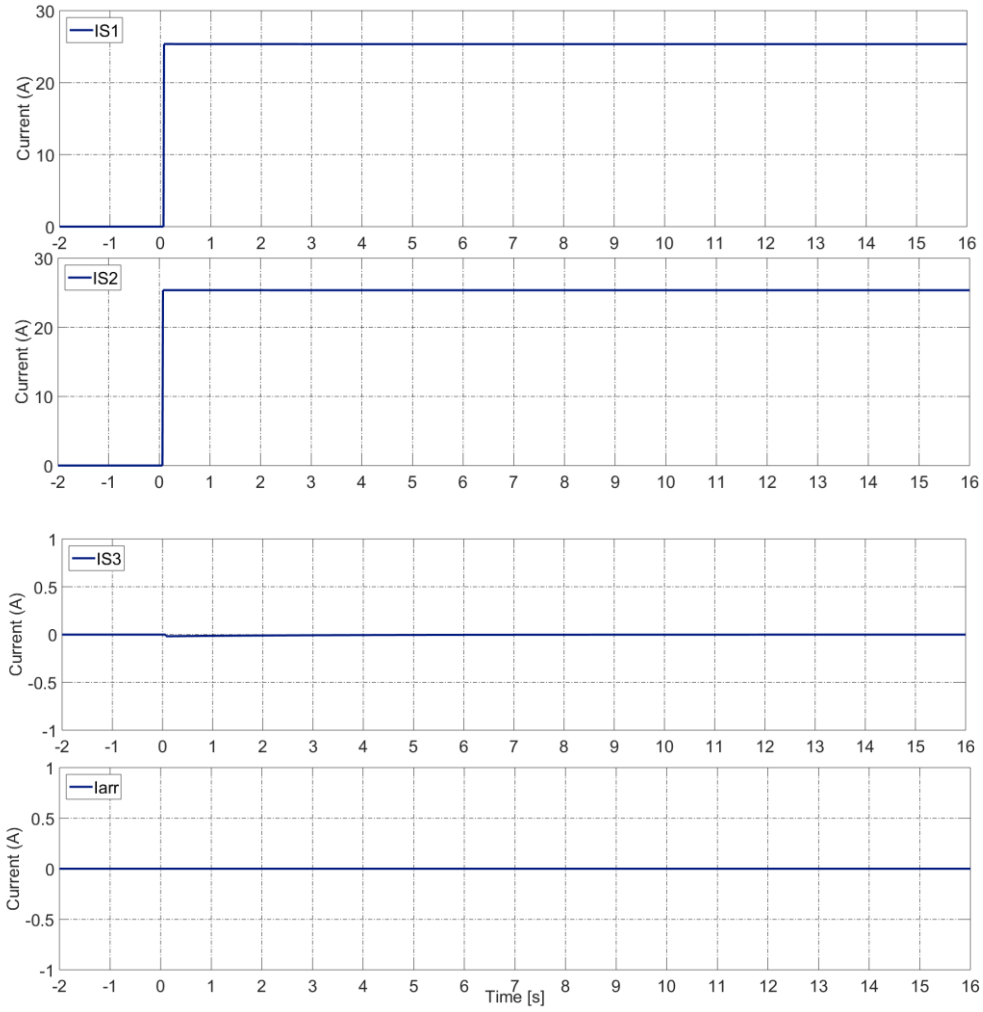

Figure 4.12. Mechanical DC CB currents during closing.

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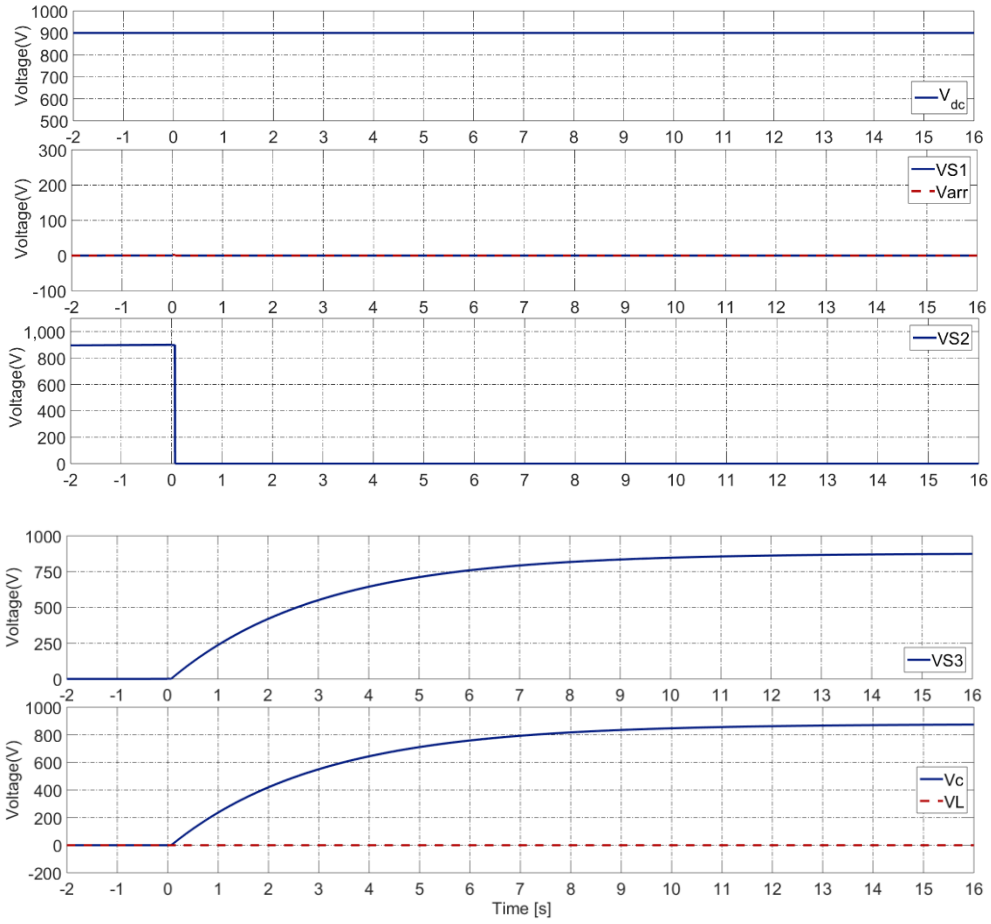

Figure 4.13. Mechanical DC CB Voltage during closing.

4.7.3 OPENING UNDER RATED POSITIVE FAULT CURRENT

The PSCAD simulation results are presented here for opening under positive rated fault current. The fault is detected at time t=0s. The control signals of the DC CB are shown in Figure 4.14. The dotted lines show the demand signals sent to S1 and S2. The solid lines for the S1 and S2 show the state of the switches. The CB currents are shown in Figure 4.15 and respective CB voltages are shown in Figure 4.16. Figure 4.17 shows the energy dissipation.

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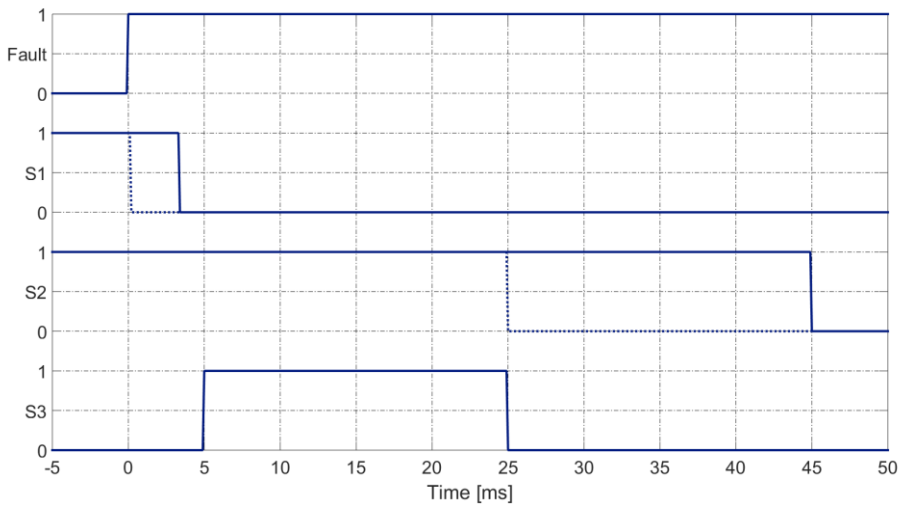

Figure 4.14. The control signals of DC CB during opening.

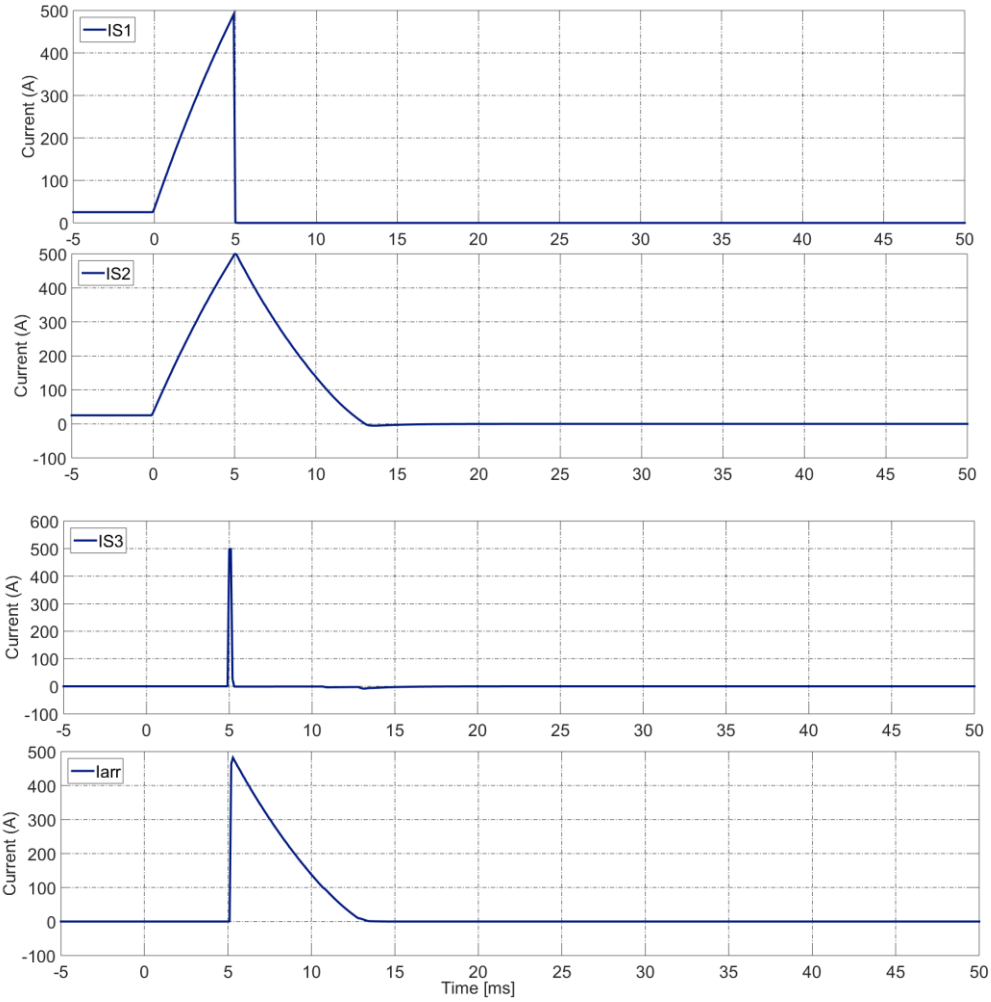

Figure 4.15. Mechanical DC CB current during opening.

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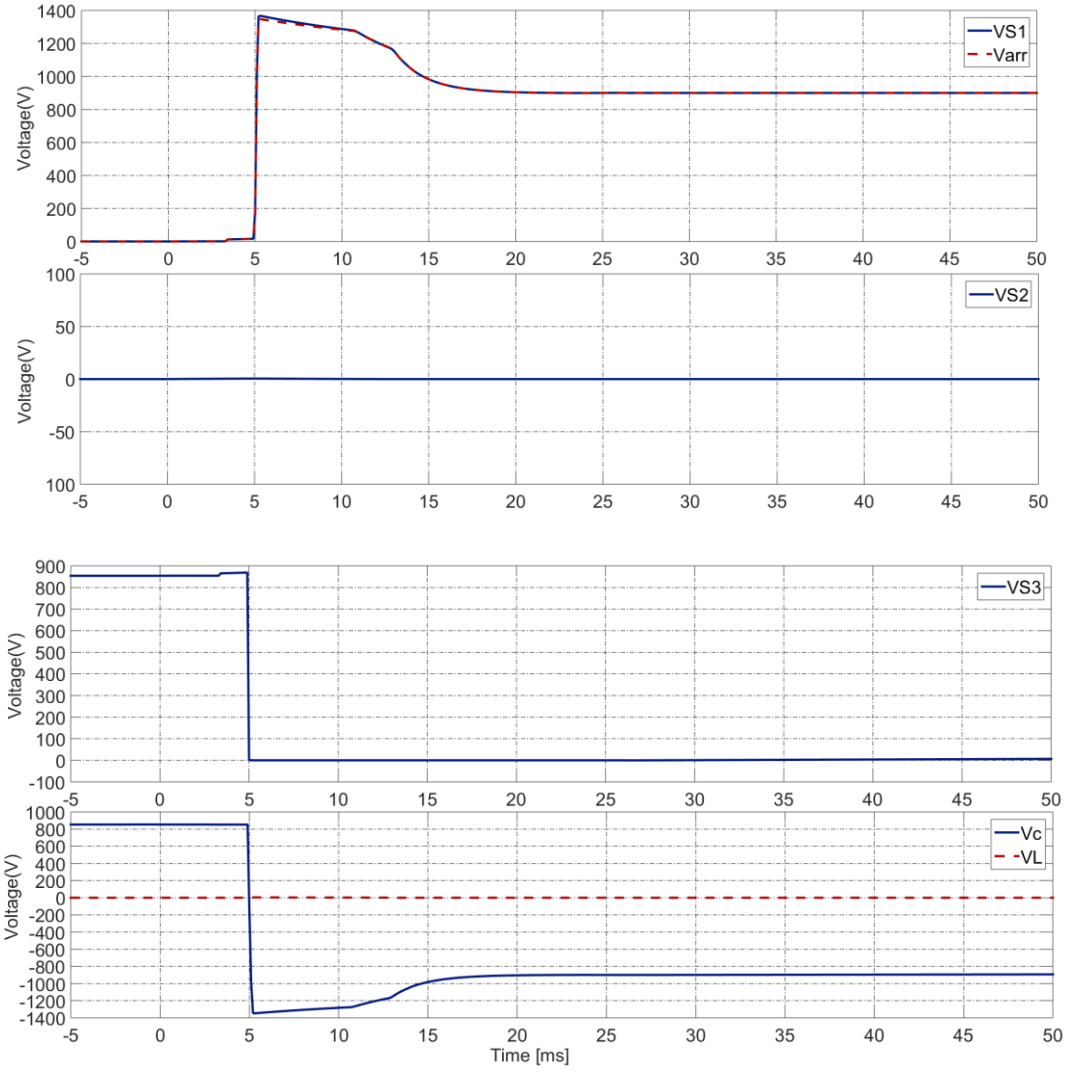

Figure 4.16. Mechanical DC CB Voltages during opening.

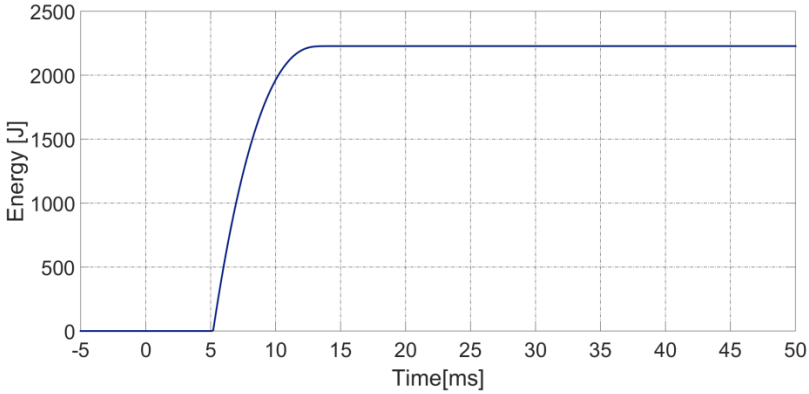

Figure 4.17. Mechanical DC CB Energy.

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4.7.4 OPENING UNDER HIGH IMPEDANCE FAULT WITH POSITIVE CURRENT

The PSCAD simulation of opening the CB under high impedance fault is illustrated here. The fault is detected at time t=0s. The control signals of the DC CB are the same as shown in Figure 4.14. The CB currents are shown in Figure 4.18 and respective CB voltages are shown in Figure 4.19.

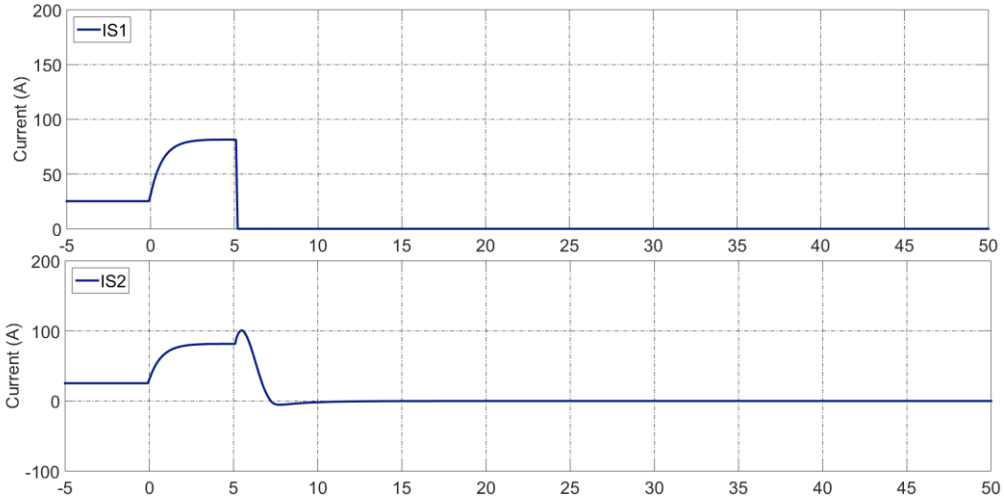

Figure 4.18. Mechanical DC CB currents during opening under high impedance fault.

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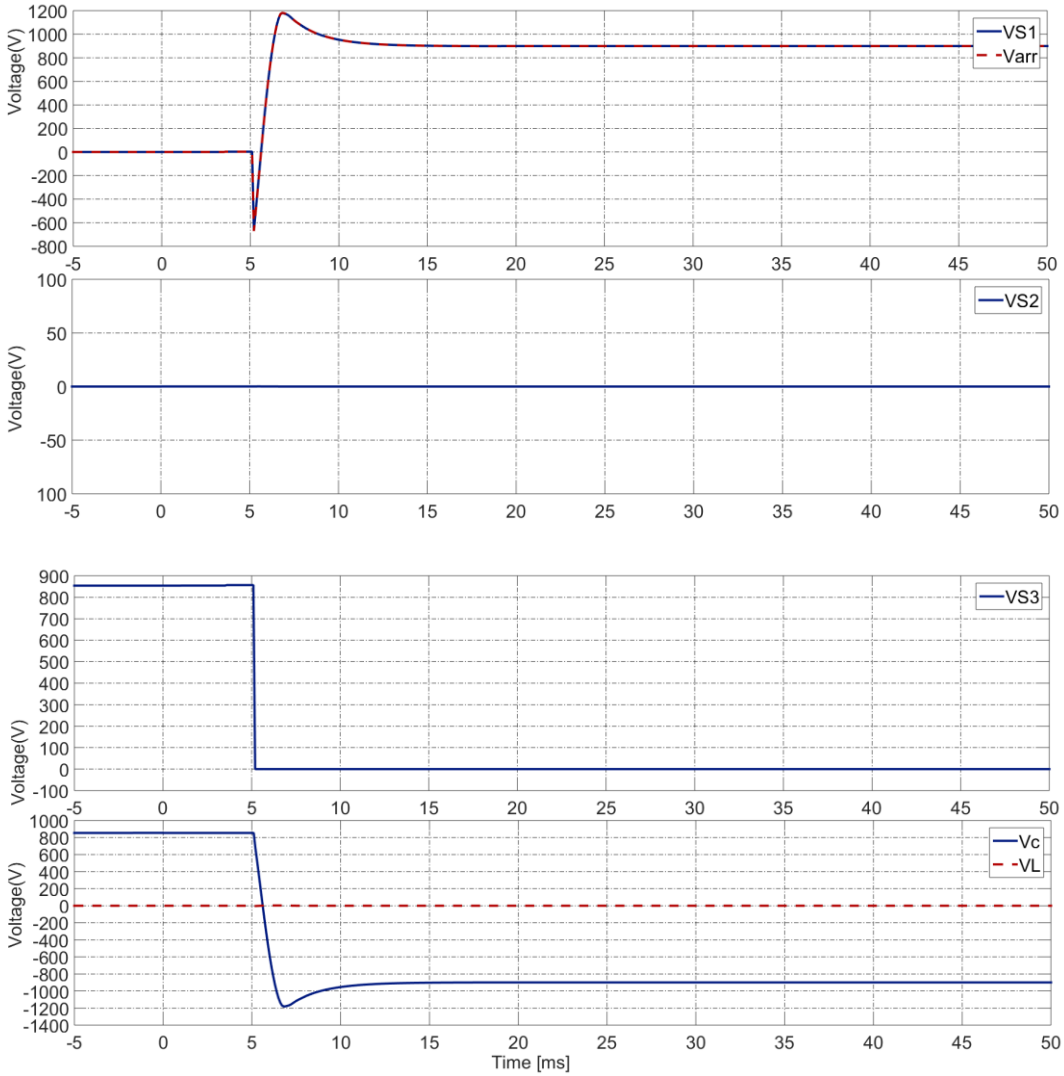

Figure 4.19. Mechanical DC CB Voltage during opening under high impedance fault.

4.7.5 OPENING UNDER FAULT WITH NEGATIVE CURRENT

The PSCAD simulation results for opening the CB with negative fault current are presented here. The fault is initiated at time t=0s. The control signals of the DC CB are the same as shown in Figure 4.14. The CB currents are shown in Figure 4.20 and respective CB voltages are shown in Figure 4.21.

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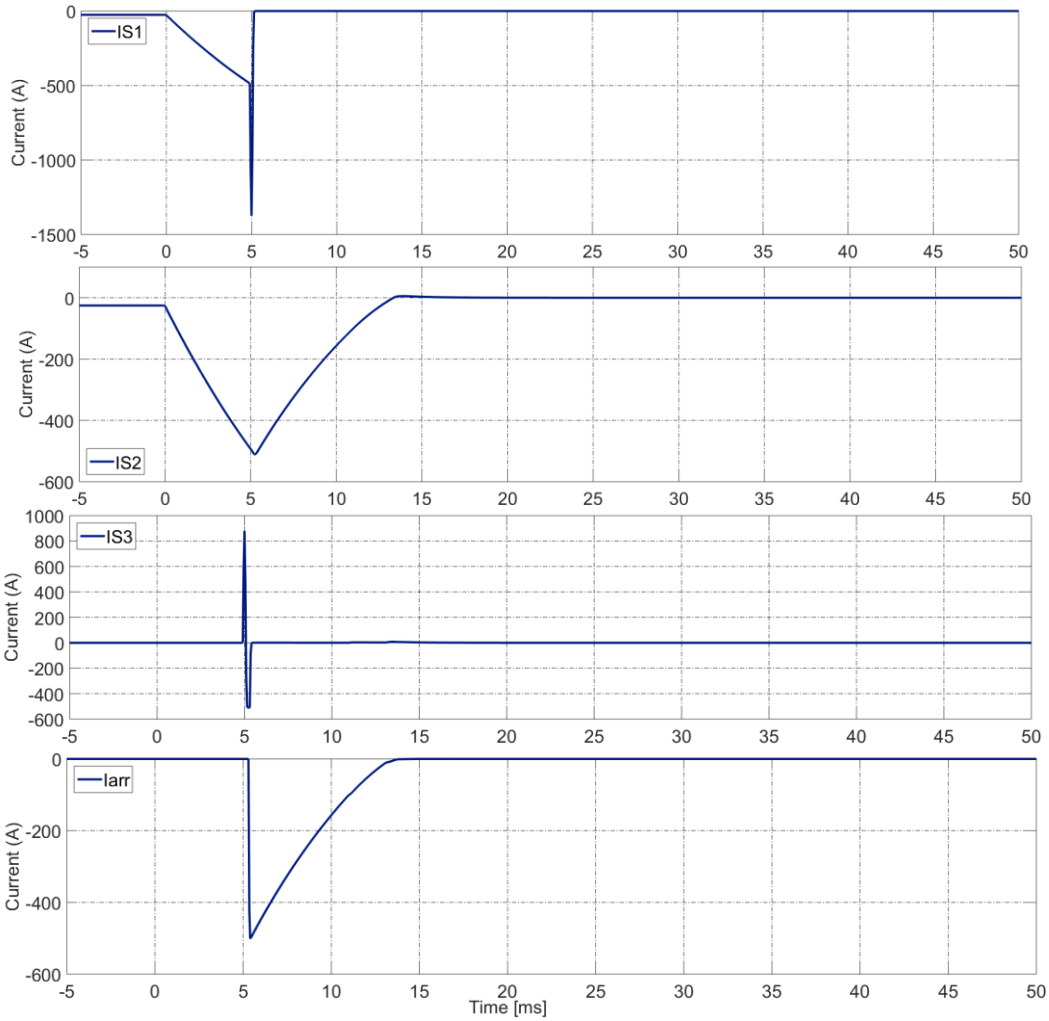

Figure 4.20. Mechanical DC CB current during opening with negative fault current.

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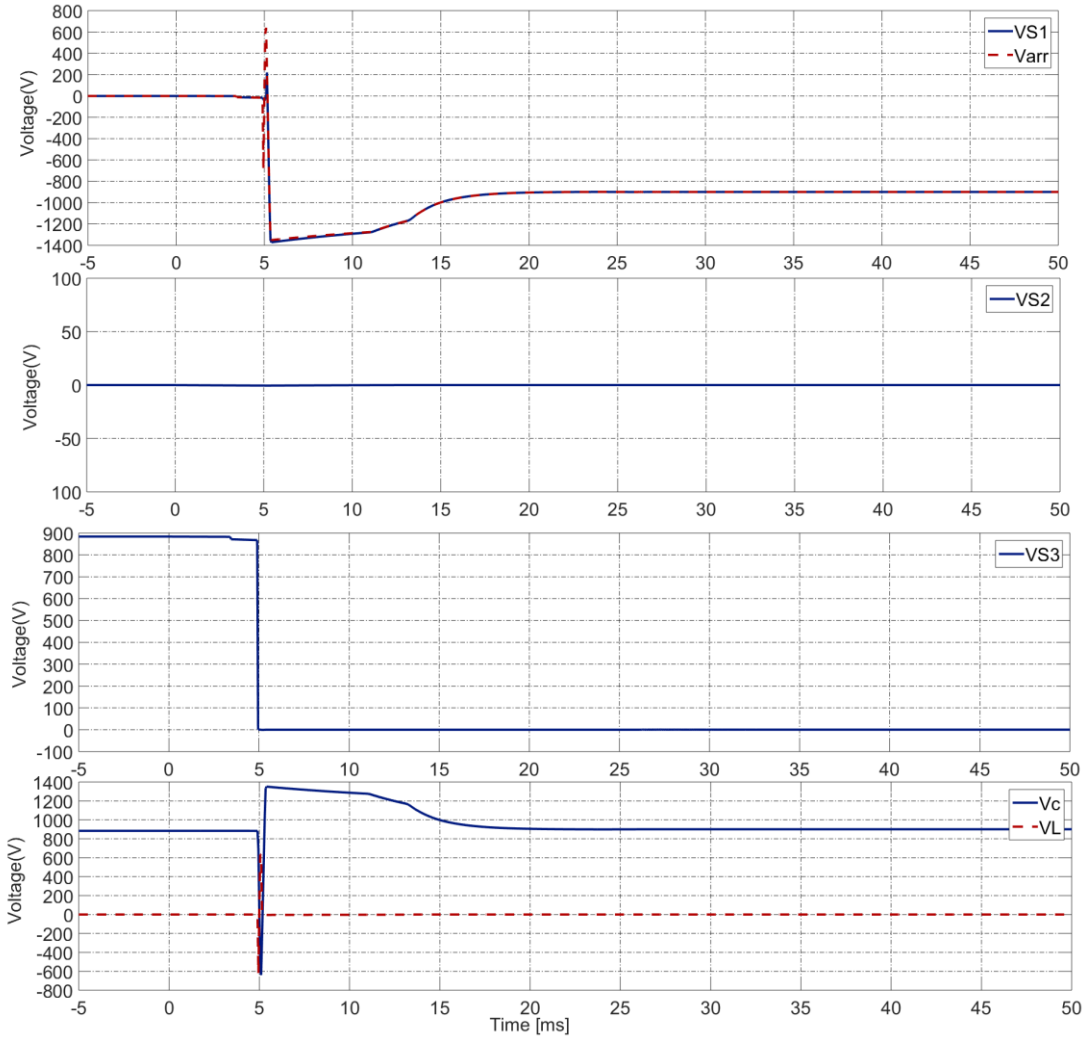

Figure 4.21. Mechanical DC CB Voltage during opening with negative fault current.

Table 4 summarises the PSCAD analysis of component stresses.

Table 4. The voltage and current stress on the components.

Component	Voltage Stress (V)	Current Stress (A)
S1	1400	500
S2	1000	500
S3	1000	1000
C=60μF	1400	1000
L=46μH	1400	1000

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4.7.6 VERIFYING ZERO CROSSINGS

Figure 4.22 shows the simulation results for the case when S1 intentionally stays closed. It can be seen that the S1 current has crossed zero four times. The number of crossings can be changed by changing the resonance circuit parameters. The resonance current is sensitive to the parasitic resistance of the circuit. Higher parasitic results in lower resonance current and higher the rate of current decaying. The parasitic resistance of the experimental setup is measured and used in the simulation.

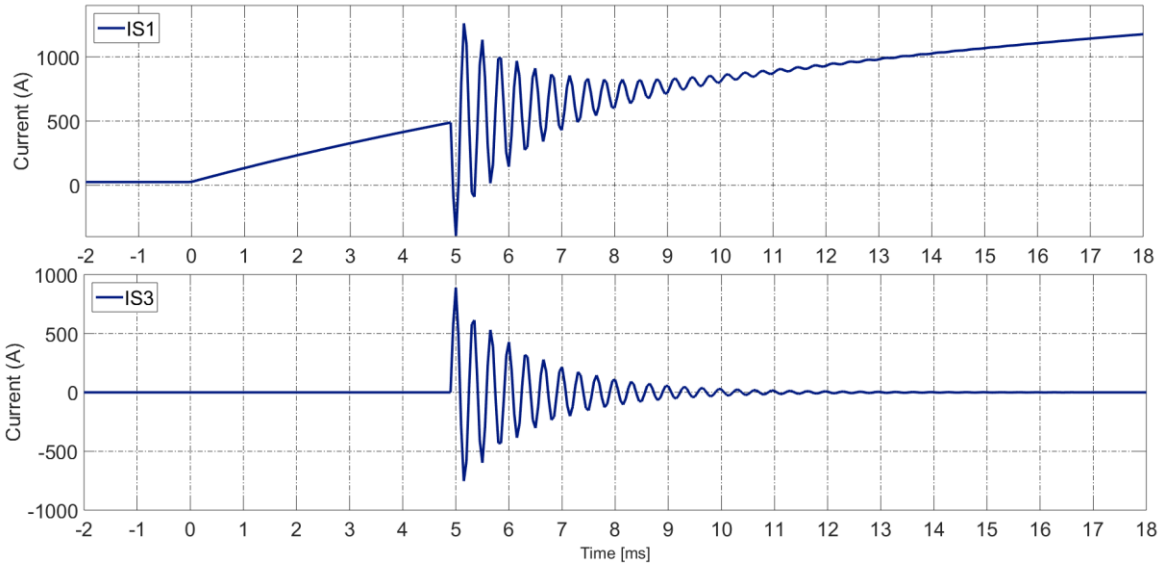

Figure 4.22. The PSCAD simulation results of Mechanical DC CB in case the S1 remain closed through the fault.

4.8 EXPERIMENTAL TESTING

4.8.1 EXPERIMENTAL CIRCUIT SET UP

The experimental circuit configuration is shown in Figure 4.23, while photograph is shown in Figure 4.24. The list of components is shown in Table XIII. The CB has been tested at different conditions, different timing of current injection and different grading components.

In particular, the following operating conditions are verified:

- Positive rated fault current
- Postive low fault current,
- Negative rated fault current,
- Negative low fault current,

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With mechanical DC CB there is substernal difference between interruption in positive and negative directions as it is seen in simulations in the previous section. Therefore negative fault current will be tested experimentally.

The selection of grading parameters is very difficult since variation in operating speed of interrupters is not known and also parasitic parameters are uncertain. Therefore procedure from [29] is used for initial value of parameters and experimental testing is adopted to select final values. The following parameters are varied:

- Cg,
- Rg,
- Time delay of S3 switch.

All the tests have been carried out at the initial dc voltage (Vdc) of 1000V (controlled voltage is 900V). Table XIII in the Appendix shows the parameters of the mechanical DCCB demonstrator.

It is noted that each test is repeated twice. However the contactors have been replaced several times during these tests because of wearing. This makes some small inconsistencies between the results. Much more detailed testing will be done in task 6.6 which studies failure modes.

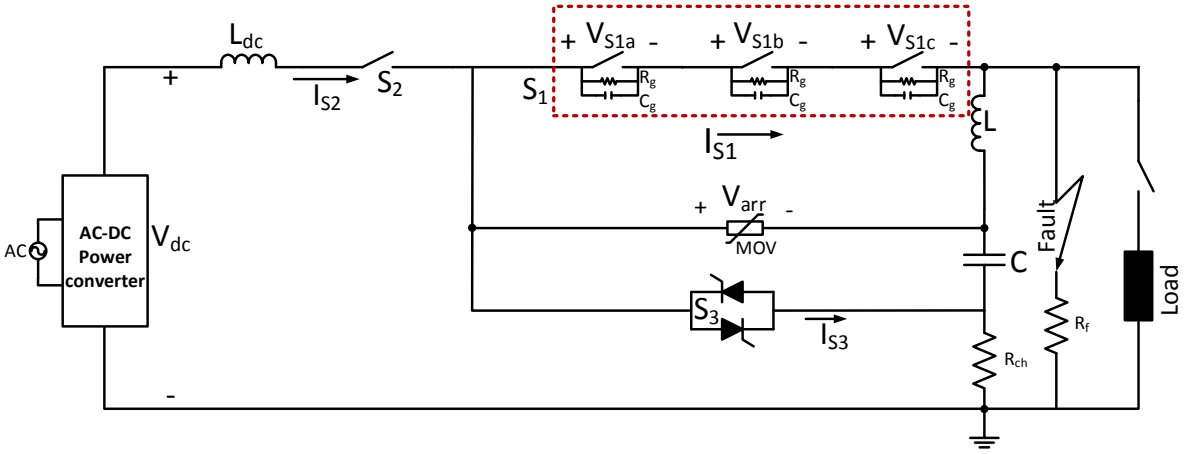

Figure 4.23. Experimental circuit configuration.

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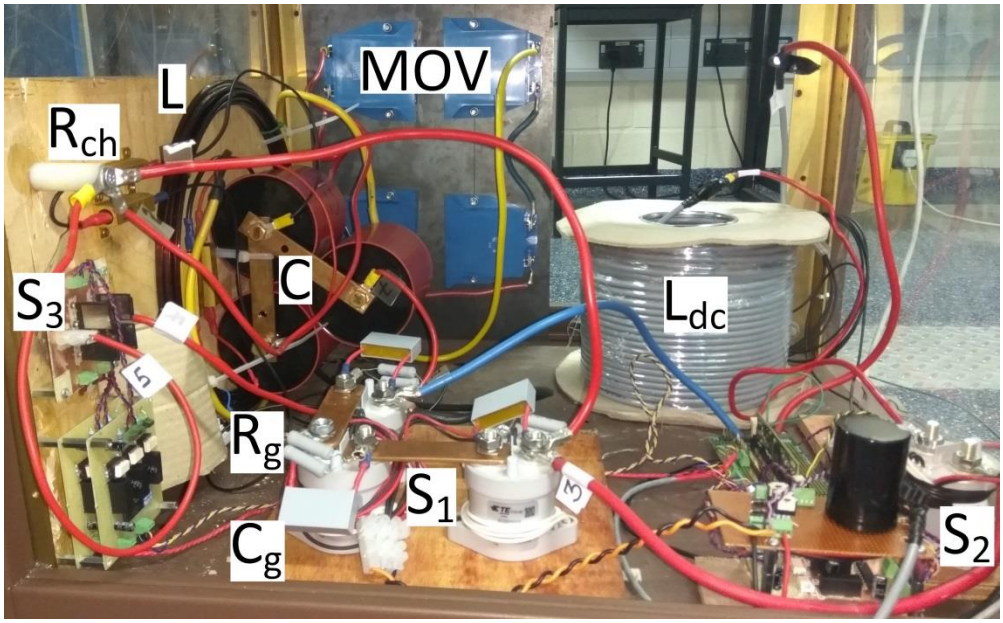

Figure 4.24. Photograph of the mechanical DC CB low voltage demonstrator.

4.8.2 POSITIVE RATED FAULT CURRENT, $R_g = 7.5k\Omega, C_g = 50nF,$ S3 TRIGGERED $5ms$ AFTER S1

In the first test, the grading resistors and capacitors are 7.5kΩ, and 50nF respectively. The fault is initiated at t=-0.4ms. Fault current detection threshold is 50A which occurs at t=0s. At this time the S1 is commanded to open. The contacts of the S1 begin to separate at around t=3.2ms. The contacts start arcing as soon as the contacts get separated. This can be seen from the voltage increase in arrester voltage shown in Figure 4.25. Once the contacts are separated sufficiently, the injection switch S3 is triggered. In this test S3 is triggered at t=5ms and the resonance current (Is3) creates a current zero crossing in S1 and turns the S1 OFF. Once the S1 is OFF the fault current is commutated to the arresters and decays to zero, as shown in Figure 4.26.

The voltages across the contactors in S1 are shown in Figure 4.27. It can be seen that while the contactors are arcing, their voltages are different. This is due to small mismatch between the contactors opening speed. Once the arcing is extinguished by the resonance current, all the voltages are the same.

It is seen that the arc voltage across three contactors raises to the same level as the DC voltage just before the current injection. This has the effect of limiting current but clearly the abrupt current interrupting occurs because of injection of resonant current. The high arc voltage is a consequence of air insulating medium and multiple break points in the contactors. This phenomenon will be different in the high-voltage DCCB which uses vacuum interrupter.

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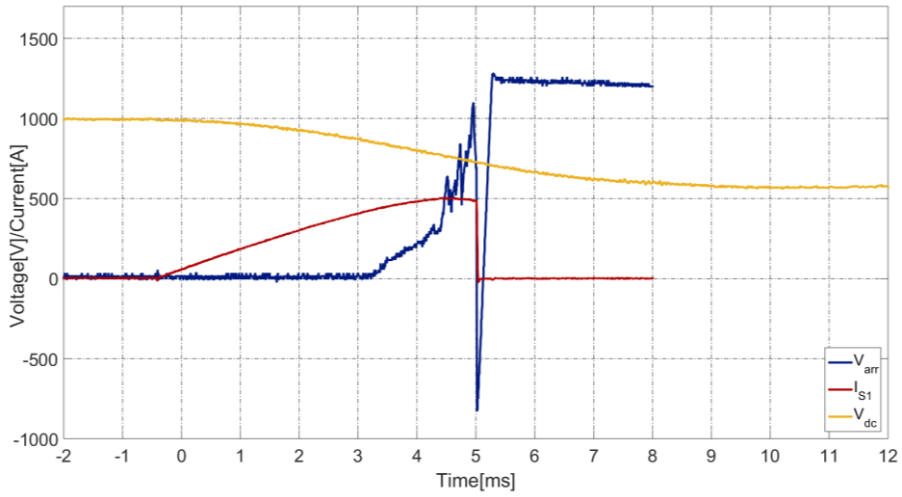

Figure 4.25. DC voltage, S1 current and arrester voltage during fault clearing.

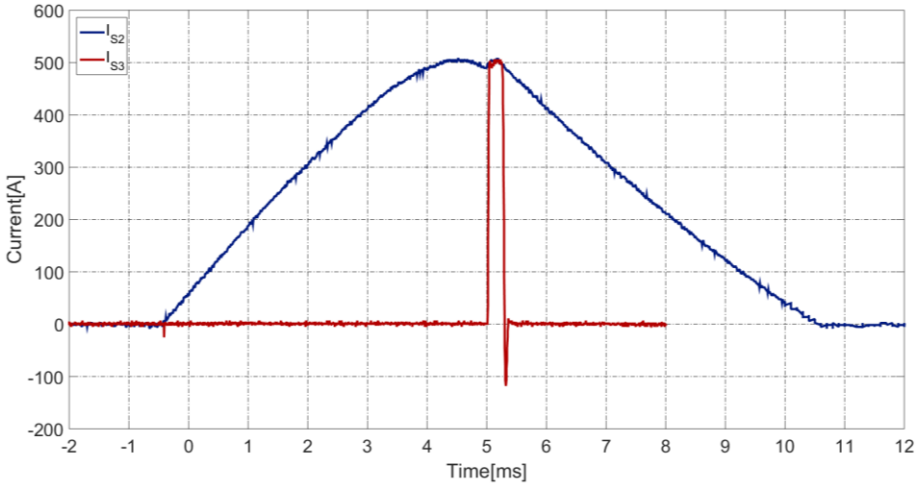

Figure 4.26. Residual switch (S2), and resonance switch (S3) current during fault clearing.

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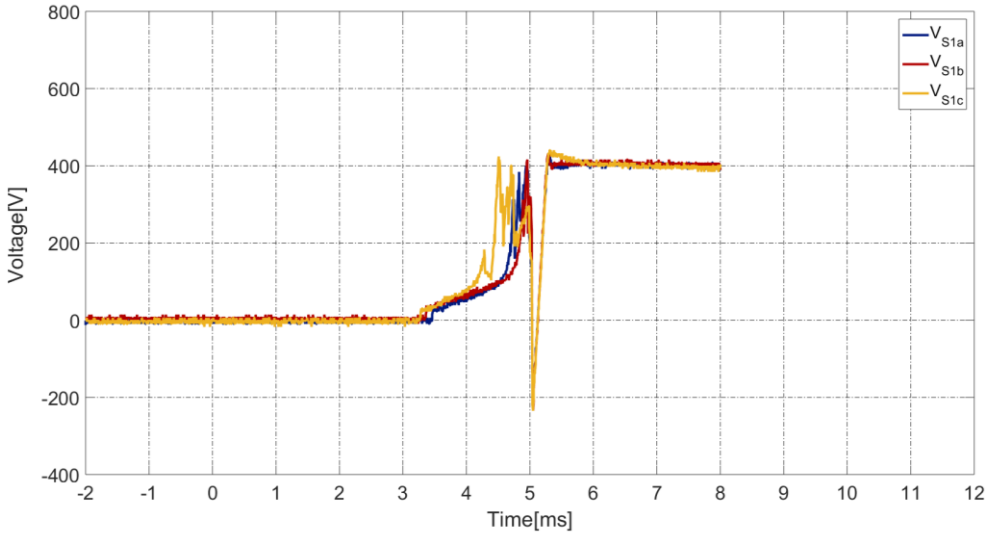

Figure 4.27 Voltages across the contactors in S1 during fault clearing.

4.8.3 POSITIVE RATED FAULT CURRENT $R_g = 7.5k\Omega, C_g = 50nF$, S3 TRIGGERED $4.7ms$ AFTER S1

In this test S3 is triggered 4.7ms after S1 with the same grading resistors and capacitors as in the previous test. The results are shown in Figure 4.28, Figure 4.29, and Figure 4.30. It is seen that waveform is better since arcing lasts for shorter period which means that contact separation distance at 4.7ms is adequate for the applied voltage stress. Shorter arcing is better since contact wearing is reduced. Figure 4.31 shows the measured energy dissipation which is derived by multiplying voltage and current through arrester with the concerned time interval. The energy is slightly different form PSCAD results in Figure 4.17 since DC voltage drop is not accurately represented in PSCAD.

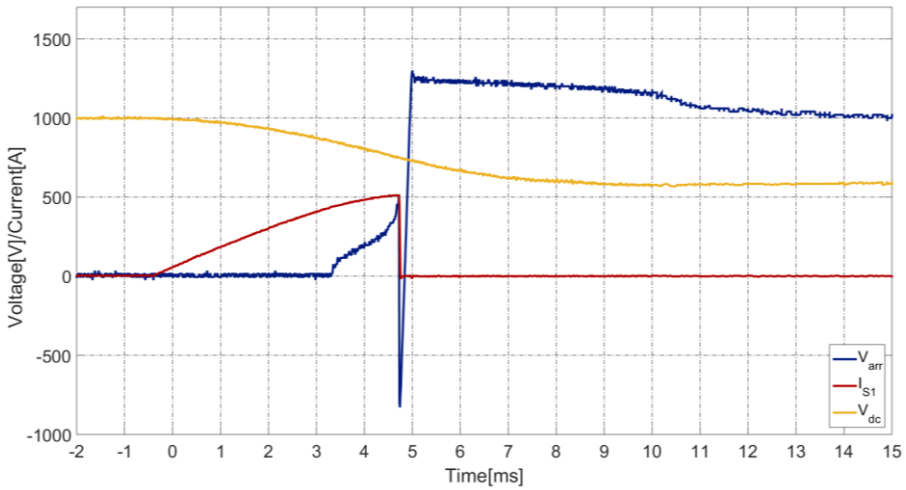

Figure 4.28 DC voltage, S1 current and arrester voltage during fault clearing.

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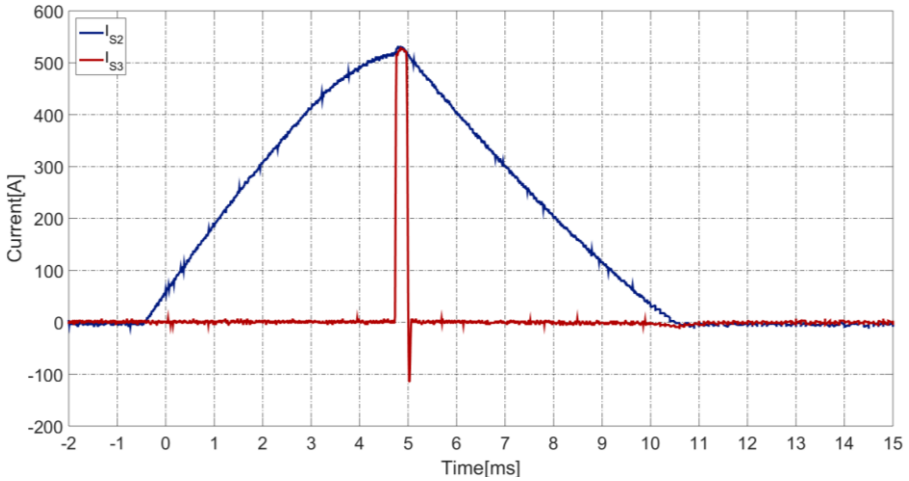

Figure 4.29 Residual switch (S2), and resonance switch (S3) current during fault clearing.

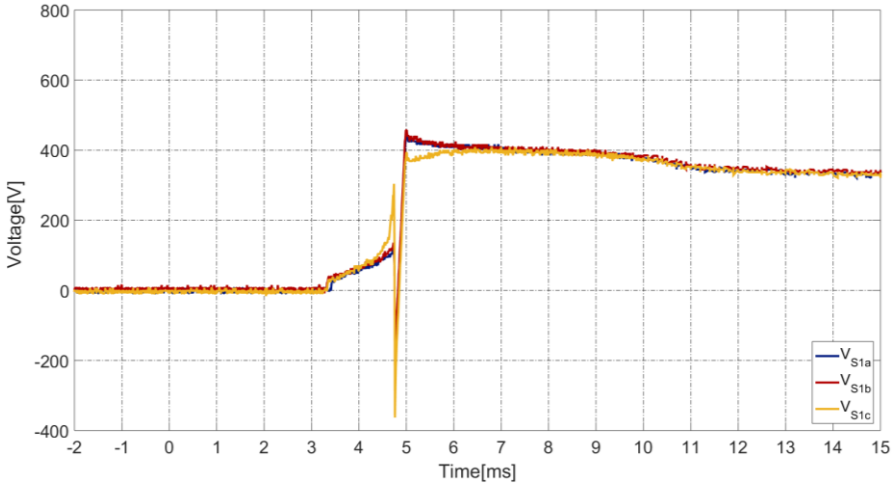

Figure 4.30 Voltages across the contactors in S1 during fault clearing.

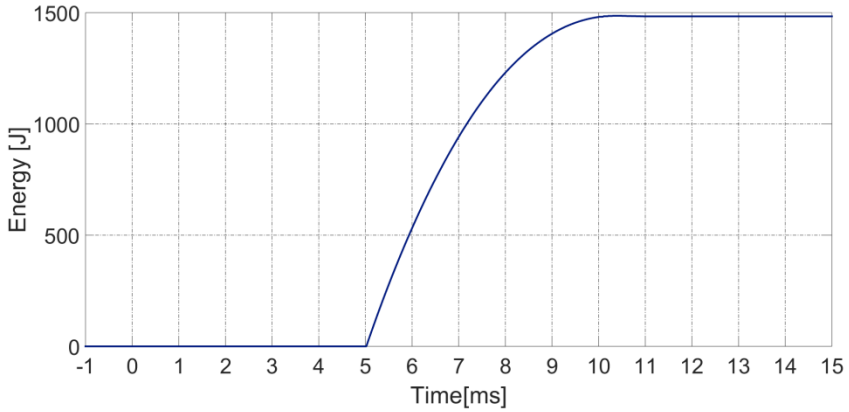

Figure 4.31 Energy dissipated during fault clearing.

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4.8.4 POSITIVE RATED FAULT CURRENT $R_g = 7.5k\Omega, C_g = 100nF$, S3 TRIGGERED $4.7ms$ AFTER S1

Figure 4.32 and Figure 4.33 illustrate the test results for $V_{dc} = 900\ V$, with grading capacitor $C_g = 100\ nF(\pm 5\%)$ and resistor $R_g = 7.5\ k\Omega$. It shows that the arc voltage sharing has not been improved compared to the previous case in 4.8.3. This is due to the asynchronous opening time of the contactors. In addition, the tolerances in grading elements (±5%) contribute to imperfect sharing.

Detailed studies will be performed in task 6.6 to evaluate possible impact on dc cb failures.

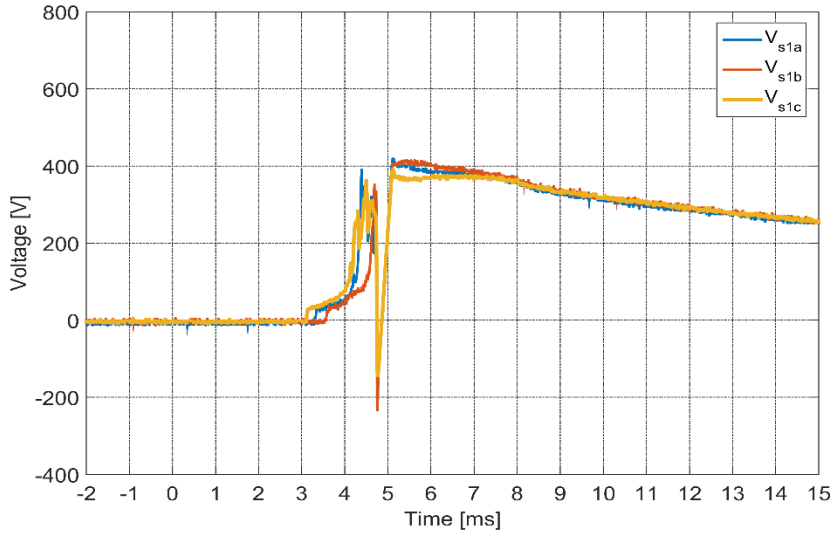

Figure 4.32 Voltages across the contactors in S1, and arrester during fault clearing.

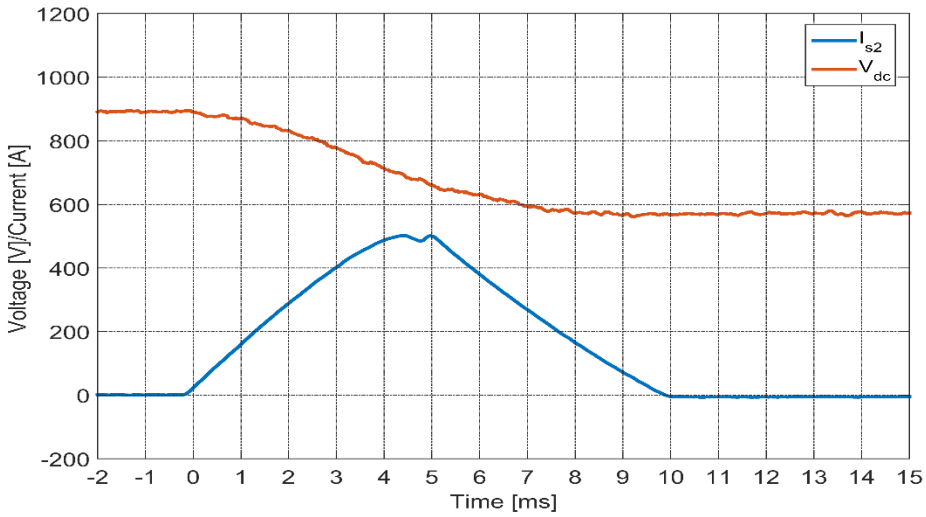

Figure 4.33 Supply voltage and current through S2.

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4.8.5 POSITIVE RATED FAULT CURRENT $R_g = 7.5k\Omega$, NOC_g, S3 TRIGGERED $4.7ms$ AFTER S1

In this test the S3 is triggered 4.7ms after S1 with the same grading resistors as in the previous test. However, the grading capacitors are removed from the CB in order to evaluate the impact of capacitors. The results are shown in Figure 4.34, Figure 4.35, and Figure 4.36. It is seen that voltage balancing across S1a, S1b and S1c is deteriorated compared with the topology using grading capacitors in the previous section.

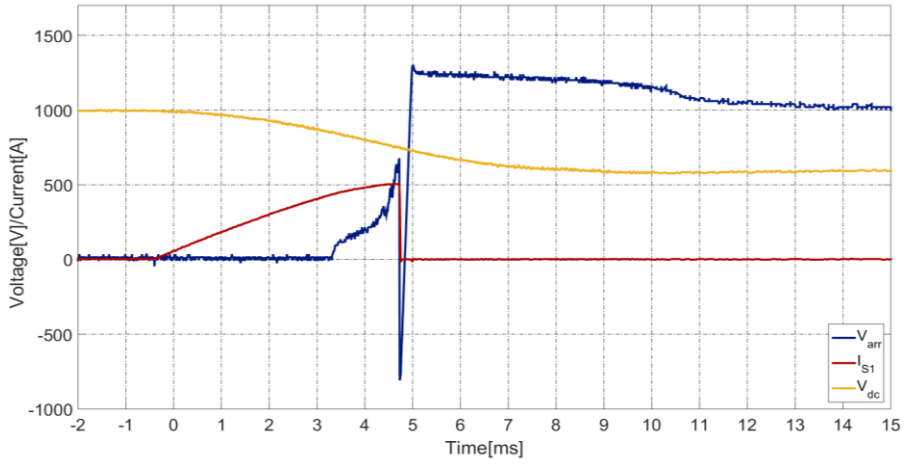

Figure 4.34 DC voltage, S1 current and arrester voltage of mechanical DC CB during fault clearing.

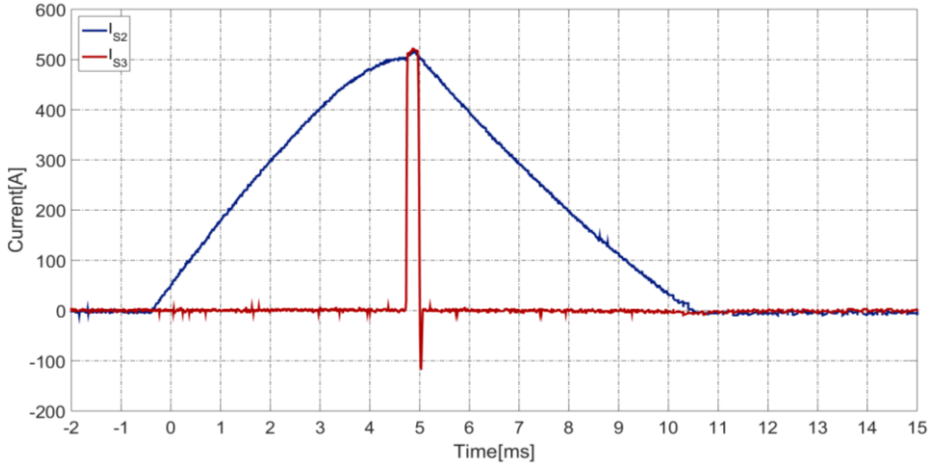

Figure 4.35 Residual switch (S2), and resonance switch (S3) current during fault clearing.

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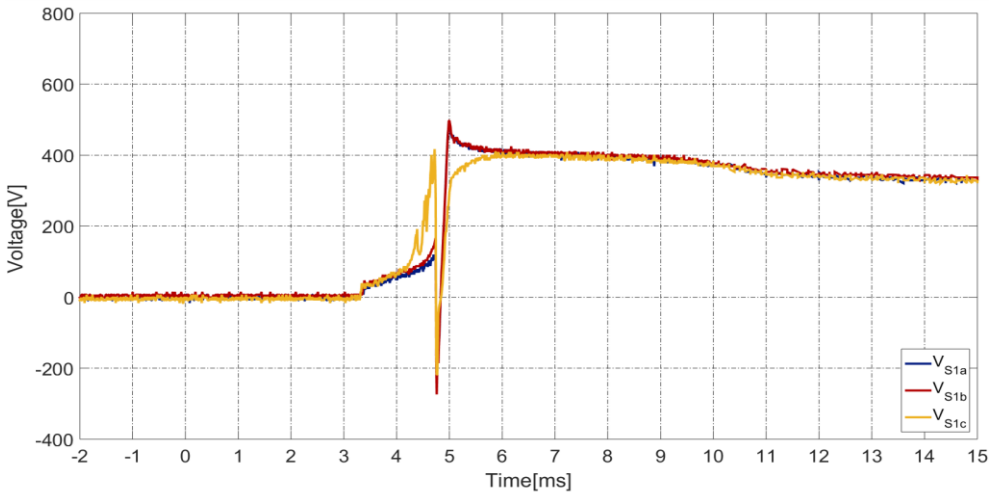

Figure 4.36 Voltages across the contactors in S1 during fault clearing.

4.8.6 POSITIVE RATED FAULT CURRENT $R_g = 22k\Omega$, NOC_g, S3 TRIGGERED $4.7ms$ AFTER S1

In this test the S3 is triggered 4.7ms after S1 with the grading resistors increased to 22kΩ, and the grading capacitors are removed. The results are shown in Figure 4.37, Figure 4.38, and Figure 4. It is seen that larger grading resistors deteriorate voltage balance across three switches.

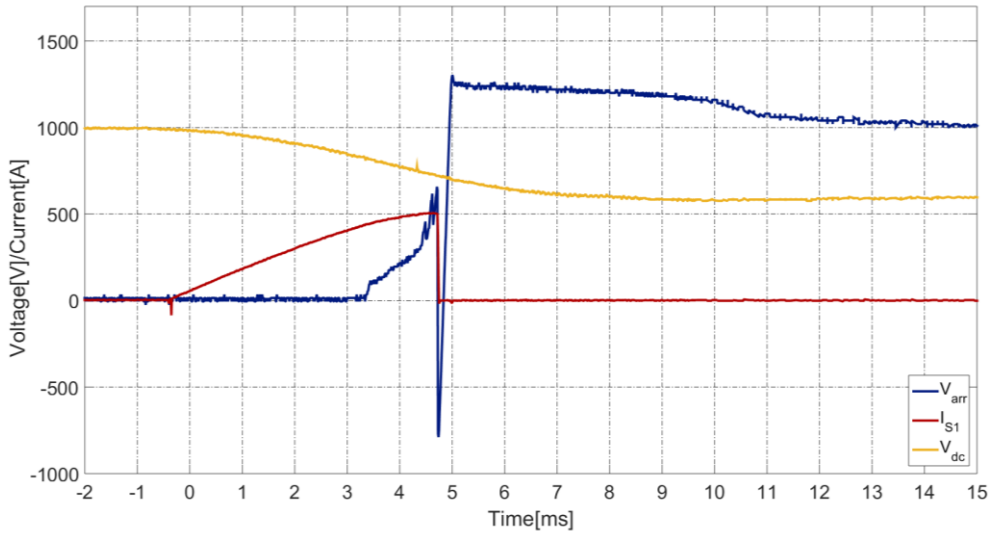

Figure 4.37 DC voltage, S1 current and arrester voltage during fault clearing.

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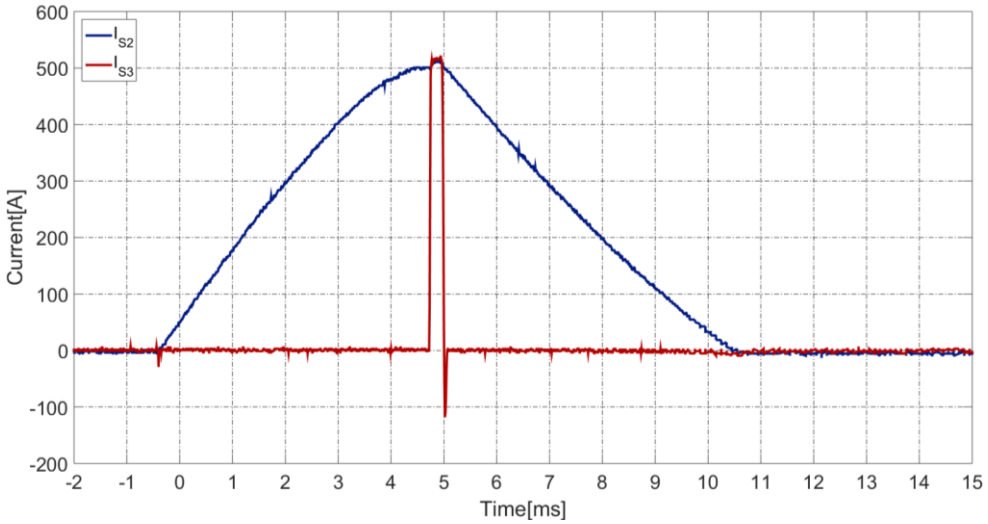

Figure 4.38 Residual switch (S2), and resonance switch (S3) current during fault clearing.

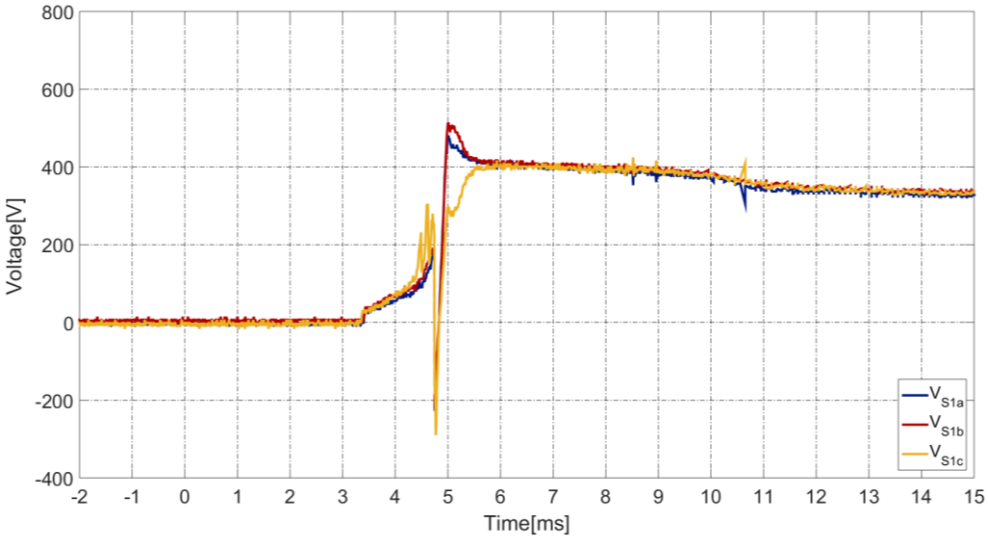

Figure 4.39 Voltages across the contactors in S1 during fault clearing.

4.8.7 NEGATIVE RATED FAULT CURRENT $R_g = 7.5k\Omega, C_g = 50nF,$ S3 TRIGGERED $4.7ms$ AFTER S1

In this test the CB is tested to interrupt a negative fault current which is achieved by reversing polarity of DC CB connections. Hence all the voltages and currents of the CB are negative. The test is carried with grading resistors and capacitors of 7.5kΩ and 50nF respectively. The S3 is triggered at 4.7ms after S1 for consistency with positive current test. Better results are obtained with slightly earlier triggering for negative fault current since the first peak of resonance current is in-phase with the fault current and only the second half cycle creates current zero crossing in S1. However it for comparisons DCCB operates with a fixed trigger time for all possible fault scenarios.

The results are shown in Figure 4.40, Figure 4.41, and Figure 4.42. Successful opening at 500A is demonstrated. The results are in agreement with the studies in [10].

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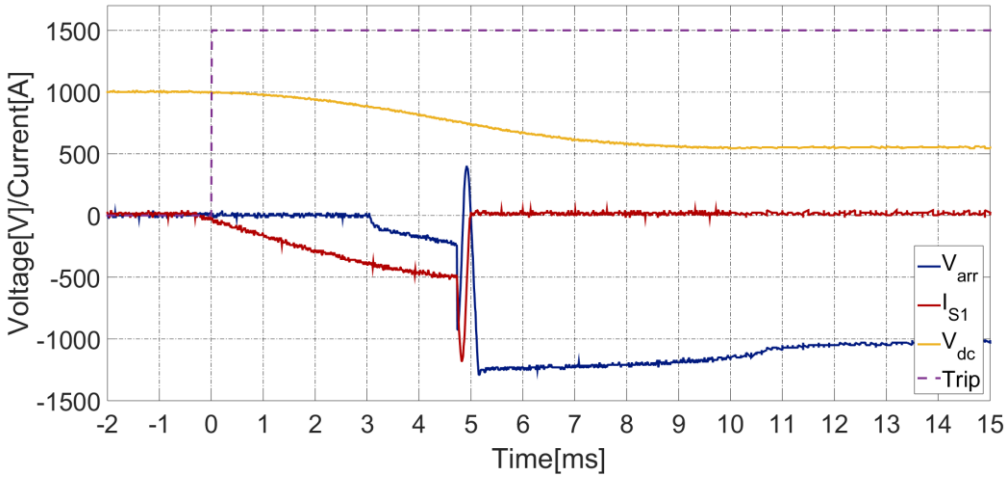

Figure 4.40 DC voltage, S1 current and arrester voltage of mechanical DC CB during fault clearing.

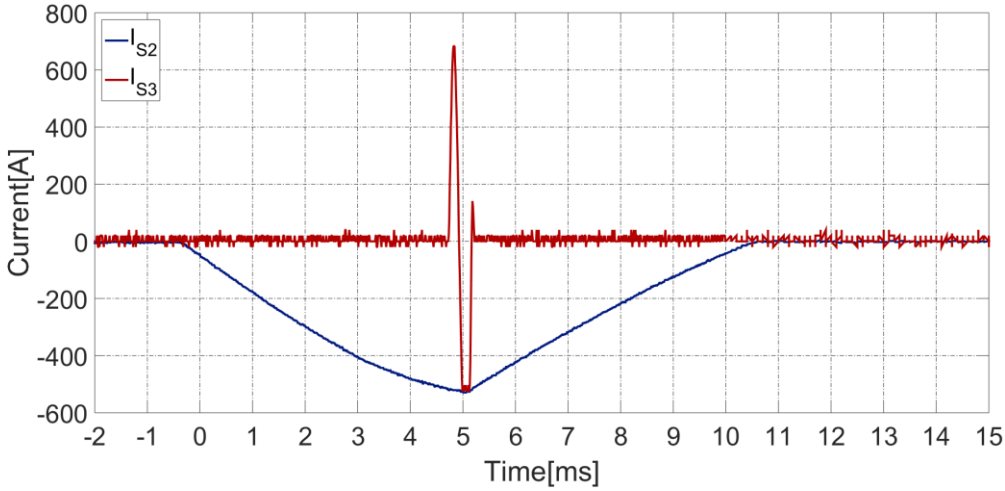

Figure 4.41 Residual switch (S2), and resonance switch (S3) current of mechanical DC CB during fault clearing.

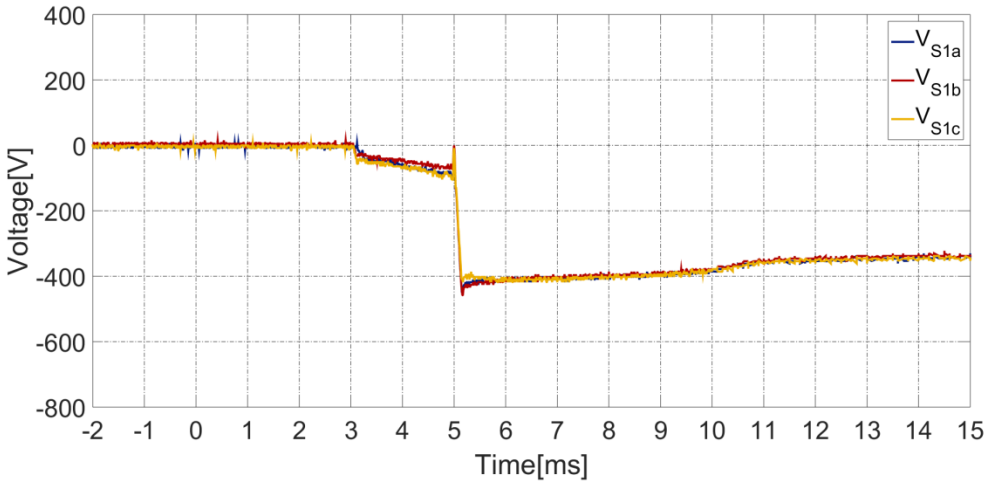

Figure 4.42 Voltages across the contactors in S1 of mechanical DC CB during fault clearing.

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4.8.8 HIGH IMPEDANCE FAULT $R_g = 7.5k\Omega, C_g = 50nF,$ S3 TRIGGERED $4.7ms$ AFTER S1

The high impedance fault test is carried out. The results are shown in Figure 4., Figure 4.39, and Figure 4.40. It can be seen that the CB can successfully open at current of around 65A. It is also seen that interruption happens when resonant current is injected. The arc voltage is quite high and close to DC voltage which implies that for this topology the interruption could occur eventually even without resonant current injection. This phenomenon is different from what would be expected in an HV vacuum interrupter employed in HV DC CBs.

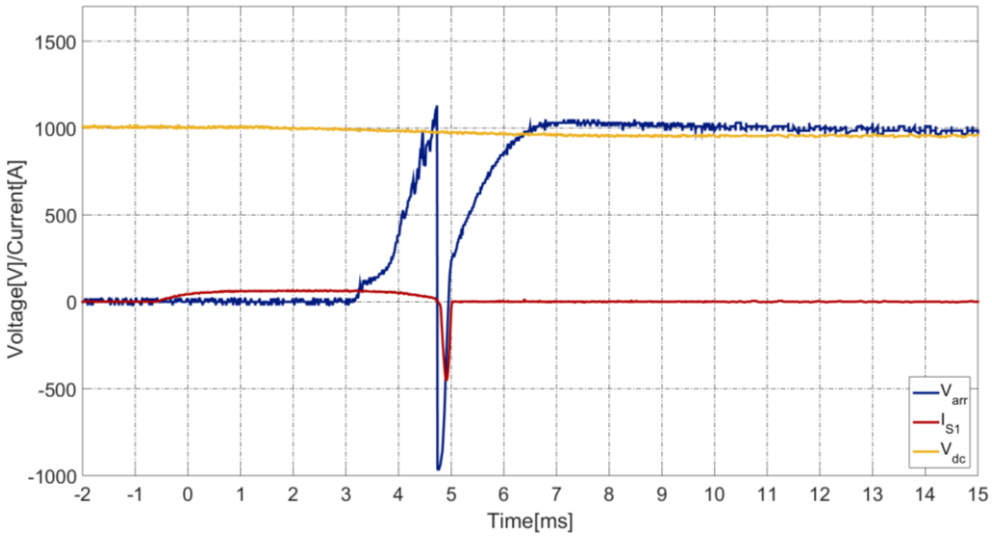

Figure 4.43 DC voltage, S1 current and arrester voltage during high impedance fault clearing.

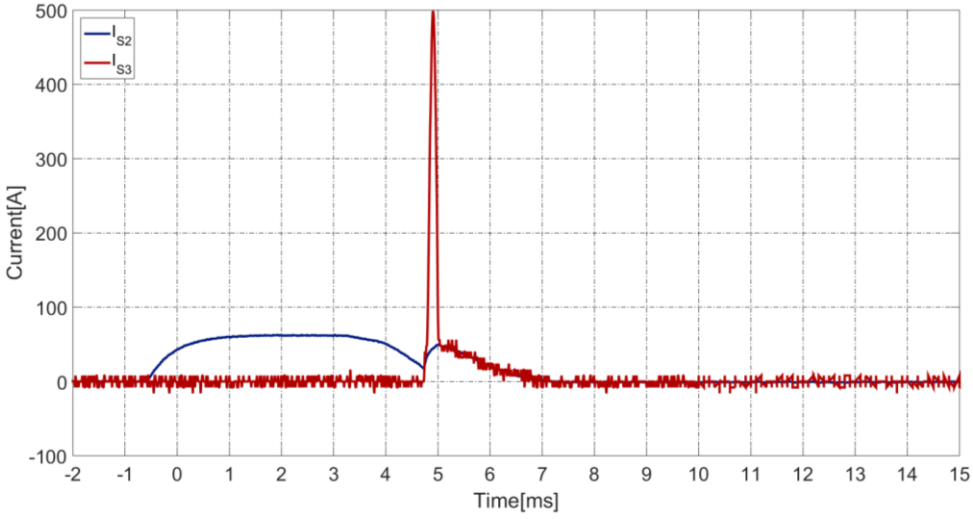

Figure 4.39 Residual switch (S2), and resonance switch (S3) current during high impedance fault clearing.

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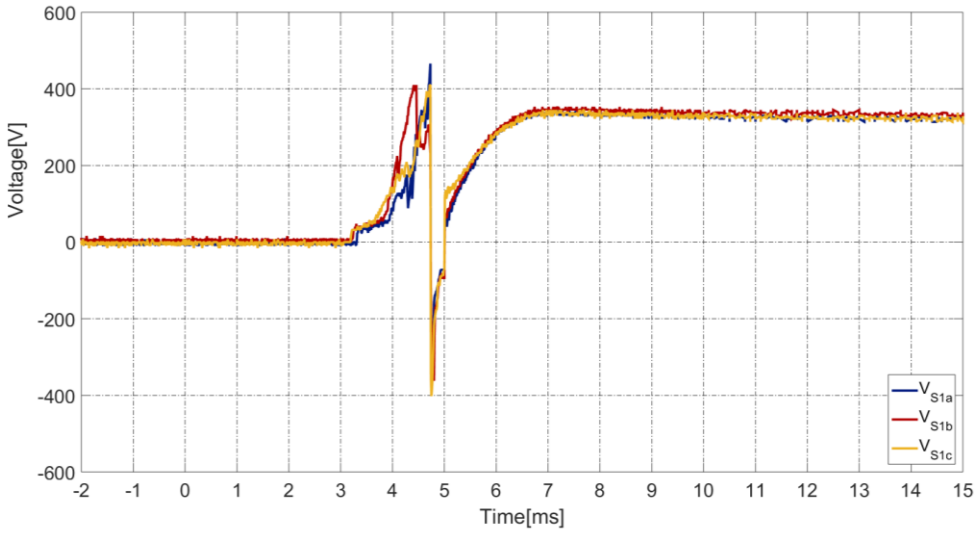

Figure 4.40 Voltages across the contactors in S1 of mechanical DC CB during high impedance fault clearing.

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5 CONCLUSION

A new DC chopper-based test circuit, for testing DC CB, is proposed that largely replicates all important stress conditions on the DC CB. The test circuit employs capacitive storage banks to avoid drawing high current pulse from the grid. The test circuit simulation and experimental results confirm that accurate stresses are applied on the DC CB test unit. The designed and fabricated test circuit is capable of supplying a pulse current of 1000A at 1000V.

A hybrid DC CB is designed, fabricated, and tested. The hardware includes a fast disconnector capable of operating in 2ms and blocking at least 1500V with 3mm gap. The experimental results show that the hybrid CB can break a fault current of 500A and the share of component stresses represent actual DCCB reasonably well. Further tests with low current and repeated operations show excellent results. A range of experimental results with fast disconnector are also presented including magnetic braking. The hybrid DCCB demonstrator is also tested for fault current limiting and new voltage control method while UFD contacts are moving.

A 1000V, 500A mechanical DC CB is designed and prototyped. The principal limitation of this demonstrator is that an air switch is sued instead of vacuum interrupter. It is concluded that there is a trade off in selecting resonant circuit components, and that the internal resistance plays an important role in damping of oscillating current. Various experimental tests are carried out on the CB. The results show that the mechanical CB is capable of breaking a fault current of 500A. Many tests with different time of current injection have been carried out and it was found that the best time for injecting the resonance current is 4.7ms after sending the command to the S1. The initial study of grading elements across 3 series-connected interrupters is also completed, although this topic will be analyzed in more depth in the forthcoming tasks.

Tests have also been carried out with negative rated fault current and successful interruption is demonstrated. Additionally, tests with high impedance faults demonstrated successful interruption of 65A current.

These demonstrators will be used for further failure mode studies in Task 6.6 and also for confirmation of analytical studies in various tasks in WP6.

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[10] Promotion Deliverable 6.2 "Develop system level model for mechanical DC CB" December 2016,

[11] Promotion Deliverable 6.9 "Standard DC CB model verification plan and RTDS models" December 2017,

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7 APPENDIX

7.1 PSCAD MODEL OF TEST CICRUIT

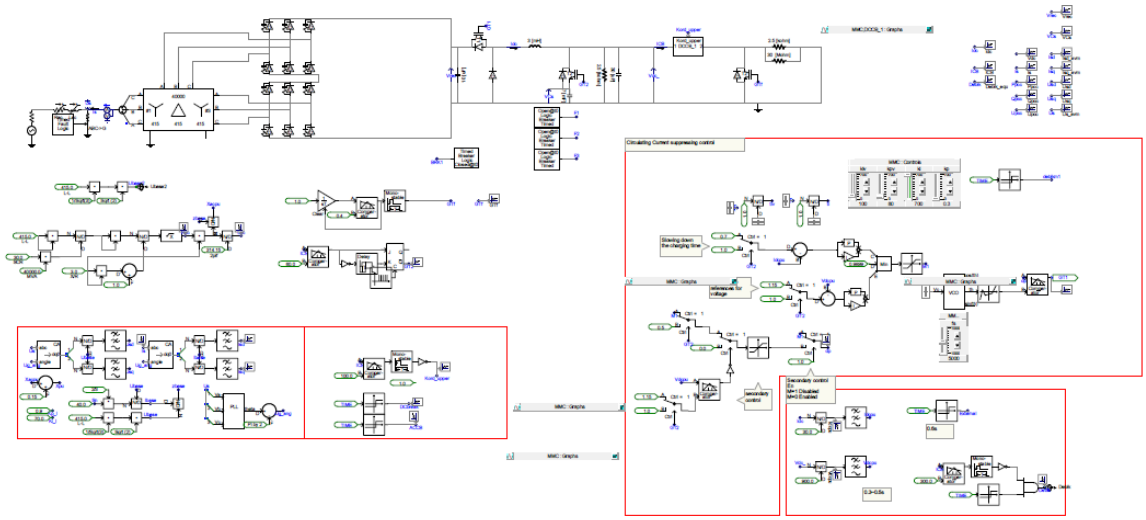

Figure 7.1 PSCAD model of the test circuit.

7.2 LIST OF COMPONENTS

Table V List of component used in the DC CB test circuit

COMPONENT	PEAK STRESS	SELECTED COMPONENT
T1, T2, D	1200V, and 100A	IGBT (T1, T2, and D) 1700V, 300A, SEMiX452GB176HDs SEMiX×2.
T_f	1200V, and 1000A	SKKT273/18E, 1800V, 273 A (9kA for 10ms).
Gate Driver		Board 2S SKYPER 32+SKYPER 32×2
Diode Bridge	1200V, and 100A	1600V, 160A, IXYS VUO160-16NO7, 3-phase Bridge Rectifier×2
Diode Bridge	1000V, and 100A	1000V, 50A single phase Bridge Rectifier×2
Diode	500V, and 50A	600V, 80A single diode×2
Capacitor bank	1200V, and 1000A	Cs, Film Capacitors 590uF 1200 Volts×12

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Inductor	1200V, and 1000A	3.5mH, 30A×1
Transformer	415V, 30kW	Three phase single primary winding and double secondary winding transformer. (415V, 30kW)
Rectifier capacitor	1200V	C_d, Film Capacitors 5uF 1500 Volts×2.
Dc capacitor	1200V	C_{dc} Film Capacitors 20uF 1200 Volts×2.
Load resistor	1200V	Resistors 2.2kΩ, 500W×3 Resistors 47Ω, 2kW×12
Arresters		EPCOS Arrestor 750Vrms EPCOS Arrestor 680Vrms×2
Fuse		Fuse 40A

Table VI List of component used in the control panel

- ON/OFF switch×1
- Push button switch×2
- Digital voltmeter(0-1200V) ×2
- Current meter×1
- LED×3
- 1kΩ Potentiometer×1
- resistor 100Ω ×1, 10kΩ×2, 1kΩ×1
- power supply 3.3V

Table VII List of component used in the voltage sensing card

- LEM LV 25-P ×1
- 22kΩ Resistors, 5W×6
- 120Ω Resistors, 0.5W×1
- Power supply +/-15V (isolated).

Table VIII List of component used in the current sensing card

- LEM LA 100-P/SP13 ×2
- LEM HTA 1000-S ×1
- 50Ω Resistors ×1, 100Ω Resistors ×1
- Isolated +/-15V power supply

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Table IX List of component used in the fault detection circuit

- 100Ω×4, 3kΩ×4, 1.5kΩ×4, 10kΩ×4.
- 5kΩ potentiometer×2.
- 15V power supply×1.
- 5V power supply×1.
- LM358N op-amp×1.
- FO Transmitter×4.
- FO driver×2.

Table X List of component used in the interface board INT1

- Buffer (CD4050BD) ×1
- FO driver (SN75451BD) ×3
- FO Transmitter (HFBR-1521ETZ) ×6
- FO Receiver (HFBR-2521ETZ) ×4
- 47uF Capacitor ×1
- 0.1uF Capacitor×4
- Resistor: 100Ω ×6, 10kΩ×4, 3.9kΩ×4
- Connector: 20pin×1, 2pin×1
- Power supply 5V

Table XI List of component used in the interface board INT2

- FO driver (SN75451BD) ×2
- FO Transmitter (HFBR-1521ETZ) ×2
- FO Receiver (HFBR-2521ETZ) ×4
- Mosfet (SI4174DY-T1-GE3)×4
- 47uF Capacitor ×4
- 0.1uF Capacitor×4
- Resistor: 100Ω ×2, 1kΩ ×4, 1.5kΩ ×2, 3kΩ ×2
- Connector: 2pin×2, 2pin×2
- Regulator (7805)×2
- Power supply 15V

Table XII List of component used in the test Hybrid DC CB

COMPONENT	PEAK STRESS	SELECTED COMPONENT

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T1	200V, 50A	600V, 400A IGBT SEMiX402GB066HDs × 1
T2	200V, 500A	600V, 400A IGBT SEMiX402GB066HDs × 4
S1	1500V, 50A	Ultra-Fast Disconnector × 1
S2	1000V, 500A	EV200HAANA as residual switch × 1
Ldc	1000V, 500A	3.5mH inductor × 1
T2 Arresters	200V, 500A	75vrms B40K75, energy max: 190J × 9
T2 Arresters	50V, 50A	50V V47ZA7P

Table XIII List of component used in the test Mechanical DC CB

Component	Data
S1	3 x Kilovac EV200HAANA
S2	Kilovac EV200HAANA
S3	2 x Thyristor 1600V, 70A VS-70TPS16PBF
C	60µF WIMA film capacitor
L	46µH,
Ldc	7mH
Rch	50kΩ
Rg	7.5 kΩ
Cg	50nF
Arresters	4x EPCOS B72260B0131K001 (170 Vdc)

7.3 900V CONTACTOR

The datasheet of the contactors used in S1 and S2 is shown below.

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KILOVAC EV200 Series Contactor With 1 Form X (SPST-NO) Contacts Rated 500+ Amps, 12-900 Vdc

Product Facts

- **Designed to be the smallest, lightest weight, lowest cost sealed contactor in the industry with its current rating (500+A carry, 2000A interrupt at 320VDC)**
- **Built-in coil economizer — only 1.7W hold power @ 12VDC and it limits back EMF to 0V. Models requiring external economizer also available**
- **Optional auxiliary contact for easy monitoring of power contact position**
- **Hermetically sealed — intrinsically safe, operates in explosive/harsh environments with no oxidation or contamination of coil or contacts, during long periods of non-operation**
- **Versatile coil/power connections**
- **UL Recognized for the U.S. and Canada (File E208033) All contact ratings & coil versions may not be UL Recognized**
- **CE marked for EC applications**
- **AIAG QS9000 designed, built and approved**
- **RoHS versions available**

EV200 Series Contactor (CZONKA Relay, Type III)

Coil Operating Voltage (Valid Over Temperature Range)			
Voltage (Will Operate)	9-36VDC	32-95VDC	48-95VDC
Voltage (Max.)	36VDC	95VDC	95VDC
Pickup (Close) Voltage Max.	9VDC	32VDC	48VDC
Hold Voltage (Min.)	7.5VDC	22VDC	34VDC
Dropout (Open) Voltage (Min.)	6VDC	18VDC	27VDC
Inrush Current (Max.)	3.8A	1.3A	0.7A
Holding Current (Avg.)	0.13A@12V, 0.07A@24V	0.03A@48V	0.02A@72V
Inrush Time (Max.)	130ms	130ms	130ms

Ordering Information

Typical Part Number ▶ **EV200 A A A N A**

Series:
EV200 = 500+ Amp, 12-900VDC Contactor

Contact Form:
A = Normally Open
H = Normally Open with NO Aux. Contacts
G = Normally Open with NC Aux. Contacts

Coil Voltage:
A = 9-36VDC (1 = requires external coil economizer)
D = 32-95VDC (2 = requires external coil economizer)
J = 48-95VDC (3 = requires external coil economizer)
R = 28VDC with Mechanical Economizer

Coil Wire Length:
A = 15.3 in (390 mm)

Coil Terminal Connector:
N = None
C = Molex Mini-fit Jr, 2 Skt, Female 18-24, P/N 39-01-2020 & 39-00-0060 +red is pin 1 (A length only)

Mounting & Power Terminals:
A = Bottom Mount & Male 10mm x M8 Terminals

Performance Data

Contact Arrangement, Power Contacts — 1 Form A (SPST-NO)
Rated Operating Voltage — 12 - 900 VDC
Continuous (Carry) Current, Typical — 500 A @ 85°C, 400 mcm conductors
Consult Factory for required conductors for higher (500+ A) currents
Make/Break Current at Various Voltages [1] — See graph next page
Break Current at 320VDC [1] — 2,000 A, 1 cycle [3]
Contact Resistance, Typ. (@200A) — 0.2 mohms
Load Life — See graph next page
Mechanical Life — 1 million cycles
Contact Arrangement, Auxiliary Contacts — 1 Form A (SPST-NO)
Aux. Contact Current, Max. — 2A @ 30VDC / 3A @ 125VAC
Aux. Contact Current, Min. — 100mA @ 8V
Aux. Contact Resistance, Max. — 0.417 ohms @ 30VDC / .150 ohms @ 125VAC
Operate Time @ 25°C — Close (includes bounce), Typ. — 15 ms Bounce (after close only), Max. — 7 ms Release (includes arcing), Max @ 2000A — 12 ms
Dielectric Withstanding Voltage — 2,200 Vrms @ sea level (leakage <1mA)
Insulation Resistance @ 500VDC — 100 megohms [2]
Shock, 11ms 1/2 Sine, Peak, Operating — 20 G
Vibration, Sine, 80-2000Hz., Peak — 20 G
Operating Ambient Temperature — -40°C to +85°C
Weight, Nominal — .95 lb. (.43 kg)

Notes:
[1] Main power contacts
[2] 50 at end of life
[3] Does not meet dielectric & IR after test, 1700 amp for unit with Aux. Contacts

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7.4 PCB LAYOUTS

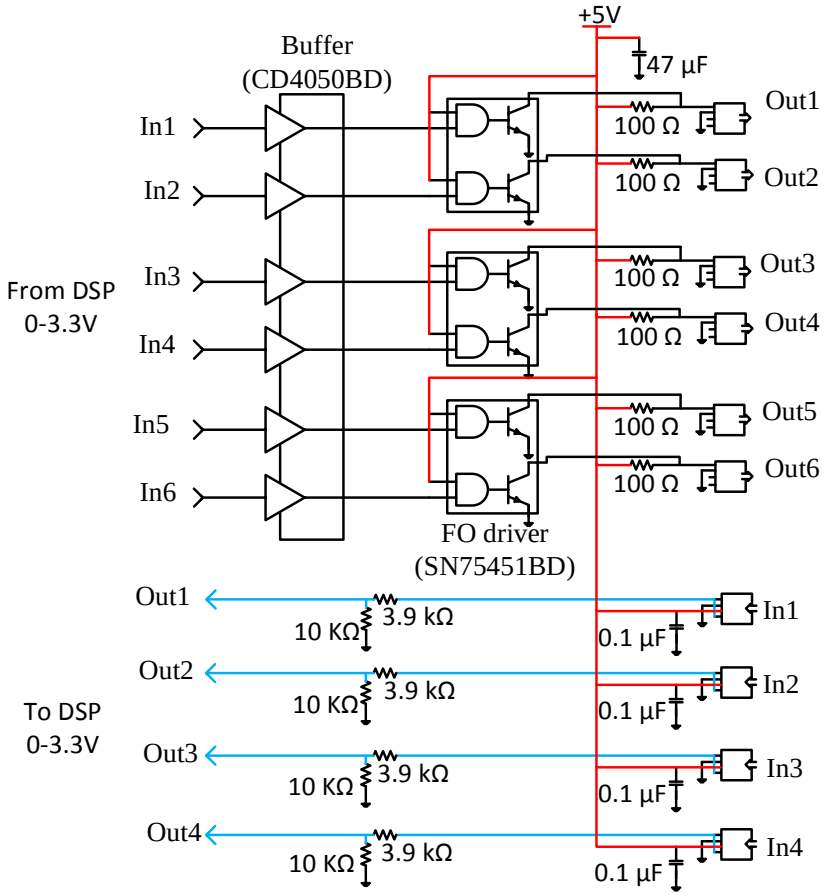

Figure 7.2 Circuit diagram of interface board1 (INT1).

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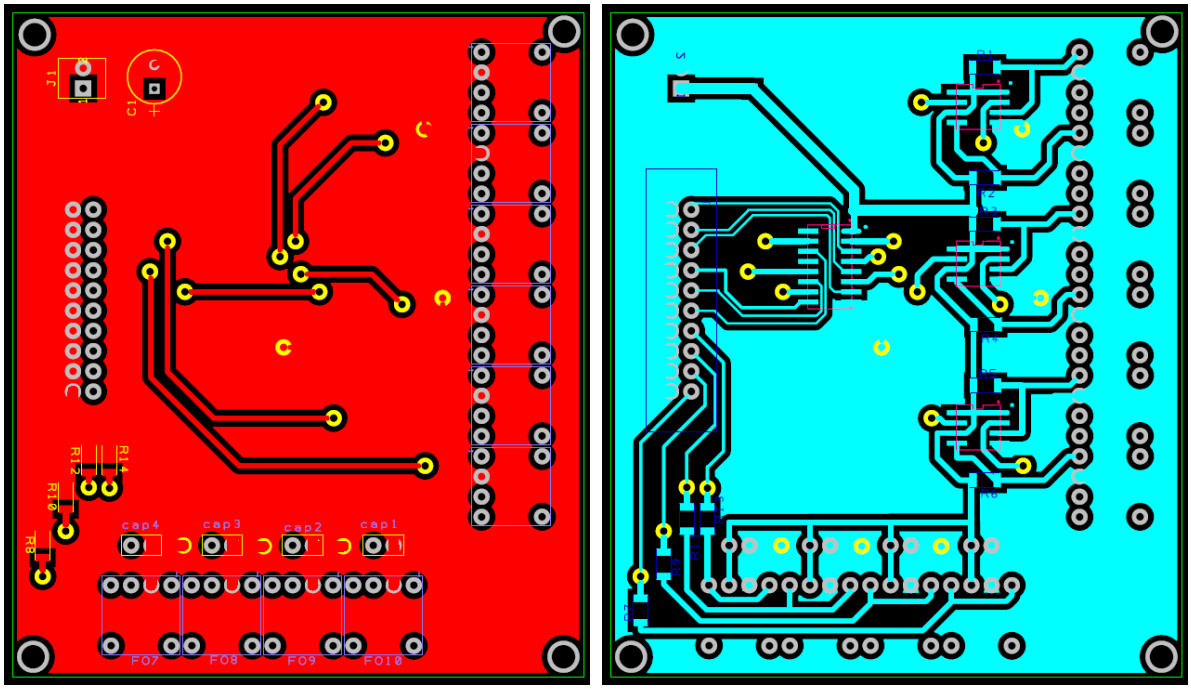

Figure 7.3 The PCB Layout of INT1. Top layout (Right), Bottom Layer (Left).

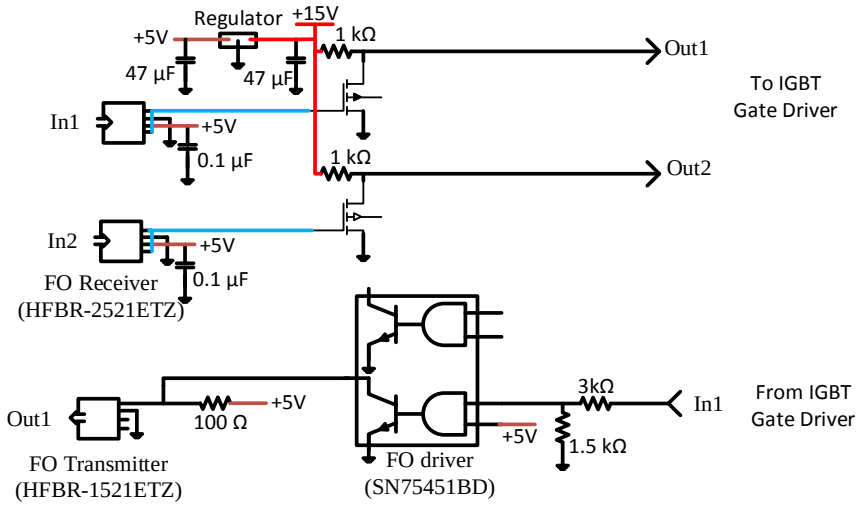

Figure 7.4 Circuit diagram of interface board1 (INT1).

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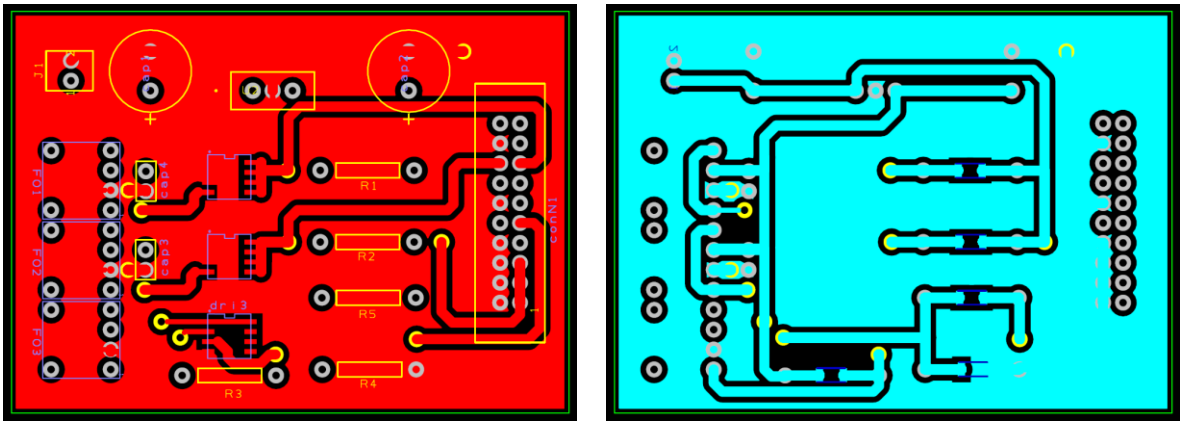

Figure 7.5 The PCB Layout of INT2. Top layout (Right), Bottom Layer (Left).

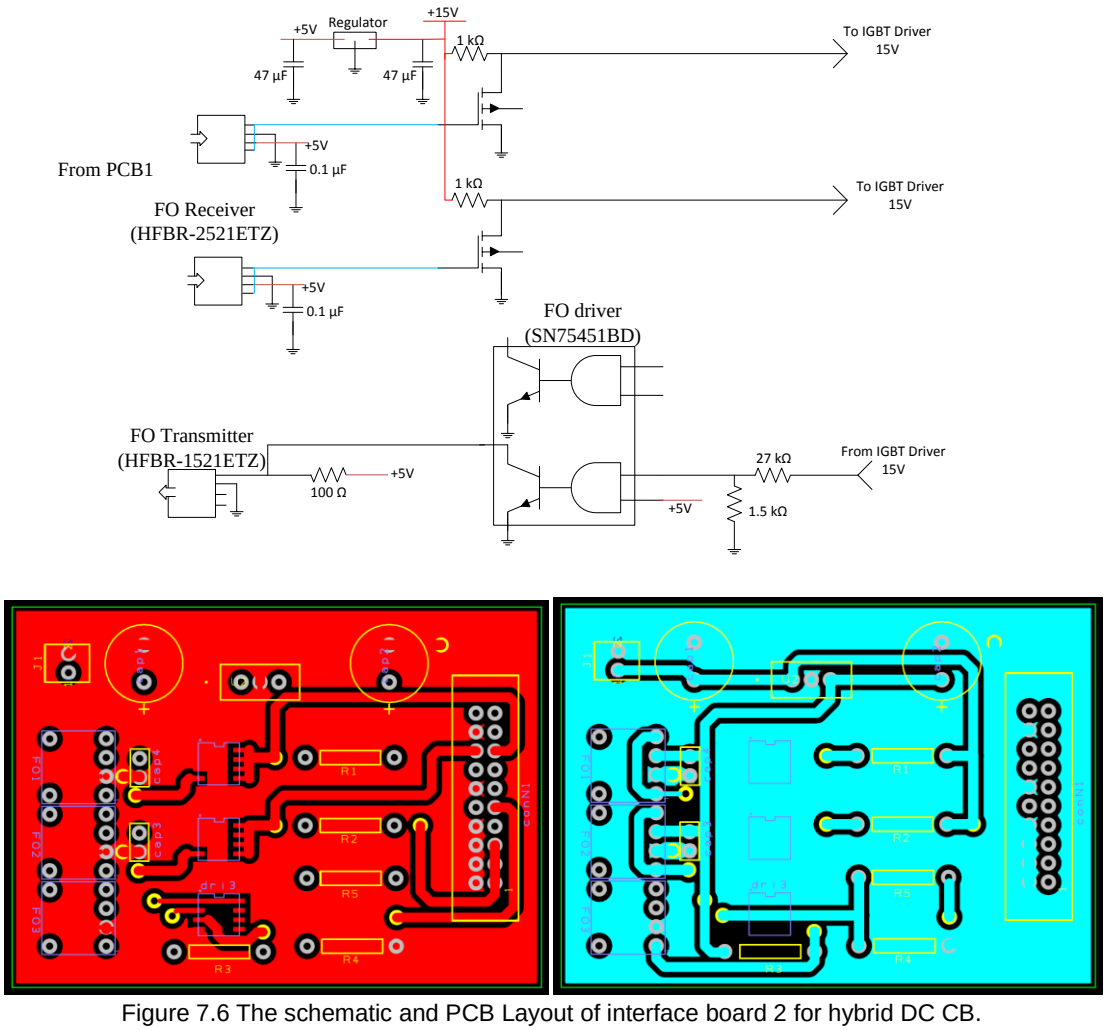

Figure 7.6 The schematic and PCB Layout of interface board 2 for hybrid DC CB.

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