PROJECT REPORT

PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

Deliverable 6.6 –Demonstrate DC CB failure modes on kw-size hardware models

PROMOTioN – Progress on Meshed HVDC Offshore Transmission Networks

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This result is part of a project that has received funding form the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

DOCUMENT INFO SHEET

Document Name:	Demonstrate DC CB failure modes on kw-size hardware models
Responsible partner:	University of Aberdeen
Work Package:	WP 6
Work Package leader:	Dragan Jovcic
Task:	6.6
Task leader:	

DISTRIBUTION LIST

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DOCUMENT HISTORY

Version	Date	Main modification	Author
1.0			
2.0			

WP Number	WP Title	Person months	Start month	End month
6	HVDC circuit breaker performance characterization	178	1	48

Deliverable Number	Deliverable Title	Type	Dissemination level	Due Date
6.6	Demonstrate DC CB failure modes on kw-size hardware models	Report	Public	M48

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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

LIST OF CONTRIBUTORS

Work Package and deliverable involve a large number of partners and contributors. The names of the partners, who contributed to the present deliverable, are presented in the following table.

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CONTENT

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SUMMARY

This report presents the findings of the failure mode study on two DC Circuit Breaker topologies: hybrid breaker and mechanical breaker.

The failure modes are analysed using hardware DC CB demonstrators in Aberdeen laboratory which have been developed in previous tasks. Also the study is complemented by literature review and PSCAD simulation both: using models for low power 5kV units and full scale 320kV units.

The failure of all major internal components in hybrid DC CB has been studied including: ultrafast disconnector, load commutation switch with parallel energy absorber, main breaker, energy absorber and residual current breaker. A model for air-based disconnector in arcing (failure) mode is developed and it was concluded that accuracy is good by comparing with the experimental results on laboratory 5kV hardware. The model for SF_6 320kV disconnector in arcing mode is also developed and PSCAD simulation confirmed expected responses for various modes including transitions between modes. A comprehensive experimental study of energy absorber failure has been conducted on metal oxide varistors rated approximately 75V RMS 190J. The experimental results confirmed that arresters are expected to fail in short circuit (or low resistance state). Further analysis at the level of energy absorber indicated that cascaded failure is feasible and likely. It was demonstrated that a single arrester failure (in a 2x2 matrix of arresters) leads to overload of the other arresters in the same column and eventually whole column fails. A proposal is made for new method of interconnecting arresters between rows in order to better spread current and prevent cascaded failure in case of a single unit failure. The testing with the arrester across load commutation switch demonstrated that it would fail in short circuit and that such failure would not be damaging for the LCS. The analysis of auxiliary power failure concluded that LCS arrester would take full load current in such case. As the result DC CB would respond like a resistor with around 9-10kV voltage drop. The case of one (80kV) module failure in a 320kV breaker is also evaluated. It is demonstrated that fault current would be interrupted in much longer time and the residual current would be large, probably beyond the ability of residual breakers.

The failure of all major components of the mechanical DC CB has also been studied. The hardware testing demonstrated that timing of activation of the injection circuit has significant impact on the success of DC current interruption. Too early current injection led to restrikes and failed interruption because contacts did not adequately sperate at the instant of current injection. Too late current injection was demonstrated to deteriorate interruption (multiple zero crossings) because of prolonged arcing which resulted in thermal-based re-striking. The study of timing inaccuracies between the series connected vacuum interrupters demonstrated that interrupters that open firstly would have most significant voltage stress. The auxiliary power failure in mechanical DC CB would not change state of the breaker.

The report also presents a new design of DC CB test circuit and ultrafast disconnector which have now been upgraded to 5kV.

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ABBREVIATIONS

Abbreviation	Explanation
AC	Alternating Current
CB	Circuit Breaker
DC	Direct Current
DC CB	Direct Current Circuit Breaker
DSP	Digital Signal Processor
EA	Energy Absorber
HDCCB	Hybrid Direct Current Circuit Breaker
HVDC	High Voltage Direct Current
IC	Injection Circuit
IGBT	Insulated Gate Bipolar Transistor
LCS	Load Commutation Switch
MB	Main Breaker
RCB	Residual Current Breaker
SA	Surge Arrester
UFD	Ultrafast disconnector
VI	Vacuum Interrupter
VSC	Voltage Sourced Converter
TIV	Transient Interruption Voltage
ITIV	Initial Transient Interruption Voltage
WP	Work Package

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1 INTRODUCTION

1.1 BACKGROUND

The use of high-voltage direct current (HVDC) transmission has been increasing because of many changes in the power industry like the use of remote renewable sources, increasing the need for interconnections and increasing the use of cable systems [1]. There have been significant advances in HVDC technologies which have increased performance but reduced losses, costs and harmonics. Presently DC transmission networks are considered feasible and the first grids are being built [2].

HVDC circuit breakers (DC CB) have been recognized as a critical component in the DC power networks. They have been developed to commercial products recently and few have been installed [3]-[8]. It is expected that DCCBs will be ubiquitous in future DC grids and therefore their significance for the future transmission systems should not be underestimated.

In the previous tasks in WP6 of the project Promotion various aspects of DC CBs have been analysed:

- In [9], (D6.1) system level model for hybrid DCCB has been developed,
- In [10], (D6.2) system level model for mechanical DCCB has been developed,
- In [11], (D6.3) detailed component level model for hybrid DCCB has been developed,
- In [12], (D6.4) detailed component level model for mechanical DCCB has bene developed,
- In [13], (D6.5) scaled hardware DC CB demonstrators for hybrid and mechanical DC CBs have been developed,
- In [14], (D6.9) standard DC CB models and testing plans are presented.

This deliverable (task 6.6) will continue the above work and will primarily utilise the scaled hardware demonstrators from [13] to perform further analysis of failure modes. The goal is to increase understanding of internal failures in hybrid and mechanical DC CBs and their impact at the system level. All the internal failures should be addressed but those most likely and important will be specially examined.

Concurrently within WP6 the following studies will also have impact on the present task:

- Promotion EU project, WP6, Deliverable 6.7 “Analyse hybrid DCCB integration in EHV DC grid” December 2019 [15],
- Promotion EU project, WP6, Deliverable 6.8 “Develop roadmap for SCiBreak DC CB scaling to EHV DC voltage” December 2019 [16]
- Promotion EU project, WP6, Deliverable 6.10 “Develop roadmap for mechanical DC CB scaling to EHV DC voltage” December 2019 [17],

This task will provide technical analysis of internal failures within DC Circuit breakers which will provide basis for further DC CB reliability analysis, cost analysis and study of system impact which is performed in Task 4.7 [18].

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The task 6.6 is also closely connected and complementary to the task 10.4 [19], which performs limited-scope failure study on full-scale mechanical DC Circuit Breaker. In this context, task 6.6 has much wider scope and greater depth but accuracy may not be as high when compared with task 10.4.

Not many references exist on the failure mode study of DC Circuit Breakers at system level. Commonly failure mode and reliability studies are based on operating experience and reliable references are available for many high voltage components [20]. In case of DCCBs only very minimal; operating experience exists. Some recent work attempts to harmonise studies across various DCCB topologies [21].

However all DCCBs are composed of a number of components which have been used in other applications for many years. Therefore the reported experience with internal components will be examined and used to direct the study in this project.

1.2 MOTIVATION

It is critically important for DC grid developers and operators to fully understand behaviour of DC Circuit Breakers including failure modes. The protection system designers also need to be aware of the expected performance if DCCBs fail to operate properly [22][23].

DC CB in both hybrid and mechanical design is a complex system, significantly more complex than many traditional power system protection components. In case of hybrid DCCB, it is comprised of various subcomponents such as semiconductor-based main breaker (MB) and load commutation switch (LCS), surge arresters, snubber circuit, cooling system and auxiliary power sources, as well as energy absorption (EA) branch, ultra-fast disconnector (UFD) including Thomson coils, and bi-stable spring, and residual current breaker (RCB). Mechanical DCCB includes the interrupters comprising of operating drive mechanism and control section as well as injection circuits along with EA and RCB.

Consequently, understanding the interaction between the failure of individual DCCB components and the system level impact if high importance.

The study will be based on tests using scaled DC CB demonstrators (500 A, 0.9 kV) developed in [13] where possible. It is understood however that because high voltage effects do not scale linearly, and different quenching mediums are used, these demonstrators cannot ideally represent all properties and failures of full scale DCCBs. The study will therefore be supplemented by simulation on PSCAD models from [14],[9],[10], using both low power and full scale DCCB parameters.

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2 FAILURE MODE ANALYSIS OF HYBRID DC CB

2.1 INTRODUCTION

Hybrid DCCB, with topology shown in Figure 2.1, incorporates several novel components under different electrical and mechanical stresses. During the fault current breaking operation, the peak current stress on the DCCB is expected to be up to 19 kA or even more while the voltage stress would be 1.5 times the nominal voltage [3]. Depending on the grid topology, cable length and the size of inductive di/dt limiters, a DCCB may absorb tens of megajoules of energy in one opening operation [21]. An improper specification, or pre-mature aging, or improper operation of components of DCCB may occasionally cause a failure of some DCCB components. It is understood that a hybrid DCCB will utilize self-protection mechanism to prevent component overload [14], however, this mechanism may not be able to safeguard the breaker against all possible failures, the environmental influences and ageing. In the case of a breaker failure, backup protection [23] will need to clear the fault by opening the DCCBs on adjacent cables, and possibly also converter AC breakers.

In this regard, this section is devoted to investigating the impact of individual component failure on the system-level performance of a hybrid DCCB. The causes and effects of a failure of five distinct DCCB components as shown in Figure 2.1, are explored as follows:

1. Load commutation switch (LCS) – electronic switch (including: IGBT stack, cooling system, snubber circuit, control section)
2. Ultrafast disconnector (UFD) – mechanical switch (including, Thomson coil, bi-stable spring, drive section)
3. Main breaker valve (MB) – electronic switch (including IGBT stack, cooling system, and control section)
4. Energy absorber (EA) – bank of surge arresters (including surge arresters and connections)
5. Residual current breaker (RCB) – mechanical switch (including drive mechanism, control section, live-part)

A very detailed study of load commutation switch design and performance has been reported [24], although failures are not addressed. A low-voltage version of SF6 disconnector has been utilised as a load transfer switch in both AC and DC applications and various studies have been reported [25][26]. Some failure (arcing) tests and models have also been performed in these references. The IGBT semiconductor is the main building block of main valve and load commutation switch and numerous failure studies have been reported [27][28]. The performance, aging and failure of surge arrester which are key components in DC CB and energy absorber branch have been addressed in [29] -[32].

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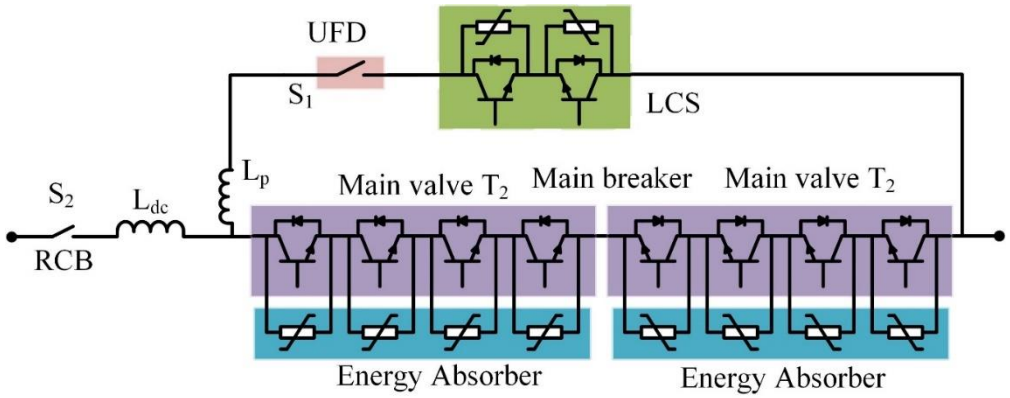

Figure 2.1 The hybrid DCCB topology.

For the purpose of this study, a failure mode is considered a function or state that falls outside the component's functional requirements. Hybrid DC CBs as a switching component needs to provide two final states, i.e. open and close. While In the close state of hybrid DCCBs, the RCB, UFD and LCS are in the close-state, in the open state, the RCB, UFD, LCS and MB are in the open-state.

The improper functioning in DC CB are as follows [20]:

- Fail open (FO) : Open without command
- Fail close (FC): Close without command
- Fail while opening (FWO): Does not open on command
- Fail while closing (FWC): Does not close on command

The definitions above can apply both to the breaker as a whole and to individual components. The open and close state define whether the component is able to conduct the current (closed circuit) or not able to conduct (open circuit). The origin of these failure modes could for example be the operating mechanism of the UFD like a failure in the Thomson coil driver, broken rod, malfunction in RCB, energy absorbers or cascading failures in DCCBs, e.g. failure in a small unit (which does not imply DC CB failure) subsequently causing failure of a module or leading to failure of DCCB.

The fault tree analysis (FTA) has been used in D6.3 [11] as a top-down, deductive failure analysis approach to clarify undesired states of a hybrid DCCB using Boolean logic to combine a series of lower-level events. This chapter expands the study and demonstrates the failures using simulation and small-scale hardware. The impact on the DC CB as a whole is examined first (high-level failure modes) whereas the failure modes of individual components are studied in later sections.

2.2 FAILURE TREE ANALYSIS

2.2.1 DCCB FAILURES IN OPEN STATE

In a fully functional breaker, all the electronic and mechanical switches mentioned in section 2.1 are open when the breaker is open, and the basic failure tree diagram is shown in [11]. Figure 2.2 shows the internal voltage

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stresses (with respect to ground) in a healthy hybrid DC CB in open state. These voltages are also important for safety while in maintenance. Because the rest of the breaker is fully isolated by the RCB, no current flows through any component and hence there are no internal voltage drops. This demonstrates that there are no undefined voltages anywhere in the breaker.

Since the RCB provides full high-voltage insulation in this state, it can be observed that a FC failure of the breaker is possible only if the RCB and at least one more component fails. FC failure of the LCS is theoretically possible due to control malfunction, IGBT breakdown or surge arrester failure. However, since the LCS is isolated by both the RCB and UFD, the DCCB remains an open circuit. FC of UFD and MB could also result from control malfunction or overvoltage, but this similarly does not influence state of the breaker. The same conclusion is reached for the EA failure in either the open or closed state, which is analysed in more depth in Section 2.6. In general, the energy absorber failure is the most serious fault and it is assumed that the back-up protection would reliably and timely detect it. Internal DC CB fault detection mechanism [33] could speed up the detection process if it is able to communicate its failure to adjacent DC CBs [34].

The RCB can become erroneously closed due to control malfunction, operating mechanism or overvoltage-induced dielectric breakdown. However, since all the other switches of the DCCB are open (UFD, LCS and MB), EA would be inserted in the circuit and the line remains disconnected. While this does not impact the power flow of the DC grid, leakage current would appear through the EA and energise the line which is not expected to be energized. Moreover, prolonged flow of leakage current could overload the EA and facilitate its eventual failure, resulting in the breaker becoming a closed circuit. This case should be considered by back-up protection designers.

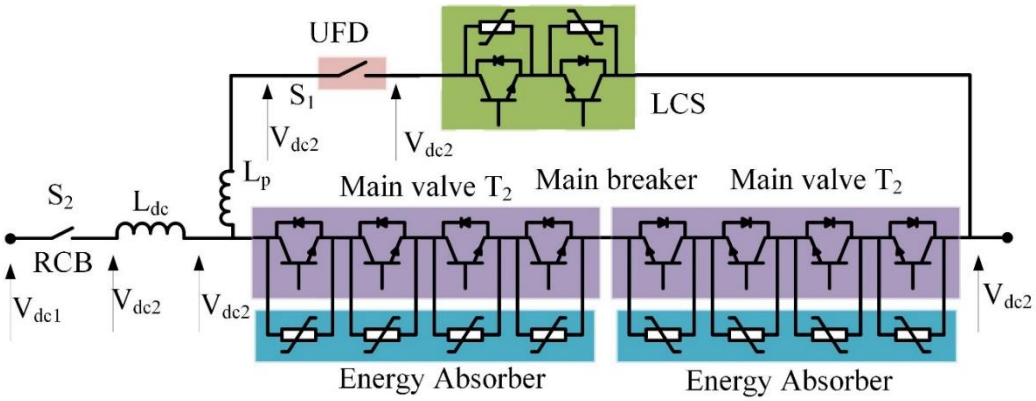

Figure 2.2 Voltage stress on the hybrid DC CB in the open state.

2.2.2 DCCB FAILURE IN CLOSED STATE

In a closed hybrid DCCB, all the mechanical and electronic switches are closed. RCB, UFD and LCS carry the load current while the current through the MB and EA is negligible. The failures of the LCS surge arrester or individual IGBTs have no system-level impact on the DCCB since both result in a closed circuit. FO of the LCS's

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arrester has no impact since this element does not conduct while the LCS is closed. However as discussed, it is assumed that arrester failure is timely detected by back-up protection.

The failure of the whole LCS valve might be feasible, perhaps because of a control malfunction or IGBT self-protection, for example if the cooling system fails. In that case the current would commutate into the MB and self-protection would open the MB. It is assumed that the MB cannot conduct the load current since it is cooled by natural convection. The FO failure of the LCS could therefore cause the FO of the whole breaker. However, the self-protection mechanism of MB in commercial DC CBs is not entirely clear, and if activated solely on valve temperature and overcurrent as assumed in [11] then the MB could be conducting limited load current. It is acknowledged that opening the MB during normal operation leads to a theoretical 2.5 pu voltage on the source side of the UFD. This case has been simulated in [13] and further study is shown in Section 2.9.

FO failure of the MB (control malfunction as a n example) would not have an impact on the DCCB performance since the main valve does not conduct (or conducts very low current) when the breaker is closed. However, if this failure is followed by failures in UFD or LCS, a complete DCCB failure happens.

The EA failure in either the closed or open circuit has no impact since this element is also bypassed by the low-resistance normal current branch. The influence of the FO of the UFD is not high due to its very low current chopping limit. It is noted that if the UFD tries to open resulting from control malfunction, the arc occurs across the UFD and consequently it could be considered as a close state. Similar reasoning applies to the RCB. However, unlike the UFD, the RCB may be able to break very low load currents (hundreds of Ampere). In such cases, the breaker would become an open circuit and the power flow is disrupted.

The auxiliary power supply failure is analysed separately in Section 2.8, and it applies equally to failure in closed state or failure while opening.

2.2.3 DCCB FAILURE WHILE OPENING

It is assumed that some form of backup protection will be installed in virtually all DC grids [22] [23]. Backup protection is expected to operate sufficiently fast if the primary protection fails in order to prevent thermal destruction of the DC grid components. LCS is the first component in a normal operating sequence to open upon the DCCB receiving the trip command. The LCS may fail to open because of control malfunction, or because it previously failed in a short circuit. The opening sequence cannot continue and DCCB remains closed.

If the LCS opens successfully, the current is commutated into the MB. The control system waits for the confirmation that the UFD is fully open before turning the MB off [9]. If the UFD fails to fully open, the current continues to flow through the MB. In such case, a signal would be sent to back-up protection to operate or, otherwise, the MB would open on self-protection. Therefore, it could result in LCS arrester overload resulting in short circuit and DC CB remains closed.

Successful opening of the UFD should be followed by the opening of the MB. The self- and driver-level protection ensure MB opening even if the main DC CB controller fails to send an opening signal for some reason. The FO

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of the whole MB is highly unlikely due to its modular structure and integrated driver-level protection circuitry. However, even if the MB fails to open for the sake of the argument, the current continues to flow through the main branch and a signal is sent to back-up protection to interrupt the current.

If the MB opens as expected, the current commutates into the EA which dissipates the fault energy and creates a defined overvoltage to suppress the fault current. In the case of a single (or multiple) surge arrester failure, the breaker may still be able to operate properly but this greatly depends on the design of the surge arrester bank. Firm conclusions can only be made with detailed knowledge of the design of a particular DCCB as discussed further in Section 2.6. On the other hand, if a fast-cascaded failure occurs and the EA becomes a low-resistance path, no counter-voltage is provided, and the fault current continues increasing until the fault is cleared by backup protection. The DCCB consequently remains closed. It is considered practically impossible that the EA would fail in an open circuit since ruptured arresters would arc and remain a closed circuit until the fault is cleared. This is convenient since (potentially very large) fault energy is always dissipated inside the DCCB, even in the case of component failures. In practical terms however, an arrester failure is almost always catastrophic and back-up protection must be immediately activated to prevent further failures and a system impact.

The final step in the DCCB opening sequence is opening the RCB after the line current decreases to the level of arrester leakage current. The failure of the RCB to open will not change the state of the DCCB on its own because the EA is inserted in the circuit and the current flow through the breaker is very low. However, leaving the EA exposed to leakage current for a prolonged period may lead to overheating of the surge arrester bank and cause cascaded arrester failure.

2.3 FAILURE OF LOAD COMMUTATION SWITCH

The LCS is an essential part of the hybrid DDCB concept to achieve a low-loss conducting path for the load current, and it includes a matrix of semiconductor switches [24]. Any design of LCS needs to fulfil key requirements [24]: low conduction losses, minimal voltage stress and high reliability. Additional features such as bi-directional current interruption, simple mechanical structure and several switching actions of LCS in a short period of time in case of reclosure, may also be required. The LCS is typically implemented as a 3x3 IGBT matrix with a surge arrester in parallel [24] but other configurations such as 2x2 or 3x4 are also feasible. This matrix form of modules provides a reliable LCS design which can handle internal fault cases on individual semiconductors with no interruption of operation [24]. The failure of electronic switches (IGBTs) is well understood and documented [25][28]. The failure modes could be divided into open-circuit (unlikely) and short-circuit.

The main origin of the open-circuit failure (FO) mode are bond wire lift-off and die-attach failures, both promoted mainly by power dissipation and thermo-mechanically induced stress. This failure mode could also result from the absence of a gate drive signal which may be caused by the component damage inside the driver, the disconnection between the driver board and the IGBTs or an auxiliary power failure. To ensure integrity of the high-voltage valves in HVDC applications, an open circuit failure is converted to a short circuit through external means (a mechanical wire bond or a fast switch). The same principles can be applied to the LCS design so that the failure of a single (or multiple) IGBT has no impact on the system-level performance of the device. However,

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because the LCS contains a considerably lower number of series-connected components than conventional high-voltage IGBT valves, the impact of a single-component failure on the voltage rating of the switch is very significant. This needs to be carefully taken into account to prevent LCS overvoltage and ensure integrity and high reliability of the switch.

IGBT short circuit during turn-on can result from high gate-voltage and external failures. Failure during on-state may be caused by static latch-up or the fast increase of intrinsic temperature resulting from second breakdown, as well as by energy shocks. In fact, excessive electric fields or temperatures lead to the failure of IGBTs in a closed circuit. Failure during turn-off can be caused by dynamic latch-up and high voltage breakdown. Failure during off-state may be caused by the thermal runaway phenomenon [28]. Noteworthy is that with series-connected IGBTs, proper voltage sharing is ensured using RC snubbers and grading resistors. Both components usually fail in a closed circuit which bypasses the IGBT. However, in the case of an open-circuit failure of the voltage balancing components, the IGBT would most likely suffer a dielectric breakdown and fail in a closed circuit. Therefore, at a system-level, only a simultaneous failure of all the IGBT modules within the same row would result in an LCS short circuit. This is not likely to occur because all the switches will have local (hard-wired, driver-level) self-protection which trips them if excessive current is detected. Overvoltage may cause simultaneous failure of multiple IGBTs but the LCS surge arrester would need to previously fail in an open circuit. The investigation in section 2.6.3 shows that this is virtually impossible within a single DC CB opening.

2.4 FAILURE OF ULTRAFAST DISCONNECTOR

Ultra-fast disconnector (UFD) is a crucial component in a hybrid DCCB which determines the opening speed. They should carry high nominal current within negligible loss and provide full voltage isolation in very short time, i.e. 2 ms [35]. UFD can open only under very small current, i.e. 1 A is specified in [35], which is ensured by proper operation of other components such as the LCS in a hybrid DC CB, and normally UFD is modelled as an ideal switch. However, in order to understand the failure modes of DC CBs it is necessary to model the responses of a failed UFD, and to identify the UFD stresses when other units fail. It is also known that the presence of internal parasitic components in DCCB imply that the UFD current will not be zero during opening [9][24].

FC, FO and FWO could result from the arc that forms between UFD contacts [25][26]. Since arcing is a common phenomenon in failure mechanism, a special attention will be devoted to modelling arc of the UFD. The electric arc is formed between UFD's contacts if the

1. UFD opens under current higher than chopping value (typically very small),
2. Electric field between UFD's contacts exceeds the dielectric strength of the insulating medium, causing a dielectric breakdown

The occurrence of the arc during the operation of the UFD needs to be evaluated from both system and component level. From system-level viewpoint, the arc keeps UFD in closed state despite its contacts being separated, it leads to exposure of UFD's contacts to very high thermal stress, which can only be sustained for short period of time.

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The first criterion for arc formation is satisfied during FO and FWO failure modes. FO mode can occur for many reasons, as an example if the UFD is erroneously given an opening signal (control malfunction) or if the Thomson coil driver thyristor fails in short circuit, causing unwanted movement of one of the rods. FWO mode occurs if the UFD is triggered prior to full commutation of the current into the main branch, for example due to the current sensor failure in the auxiliary branch.

The second criterion for arc formation may occur in FC and FWO failure modes. An overvoltage appearing across the contacts of the UFD could result in a dielectric breakdown, forcing the switch to conduct when it is meant to be open. The UFD is particularly prone to this failure mode if one of the opening Thomson coils fails since the contact distance would reduce to half. There are multiple other possible causes of such failure like: issues with bistable springs, friction or component aging.

Two UFD arcing models will be developed: the first for the 5 kV air-insulated UFD and the second for SF6 insulated 320 kV UFD. The tests on the air-insulated UFD have been performed on the 900V, 500A test circuit described in [13]. However, the UFD prototype is suitable for application in 5 kV systems based on the contact separation distance and opening speed. The behaviour of the full-scale, SF6-insulated UFD model is demonstrated in PSCAD. Detailed parameters of both devices are given in Table 6.1 in the appendix.

2.4.1 5 KV UFD ARC MODEL

Although the phenomenon and causes of electric arcs are well known, the modelling of electric arcs has remained a very challenging topic given the stochastic nature of the process. In more than a century of research on free-burning arcs in open air, numerous arc models have been developed. However, all these models are based on empirical data rather than theory, leading to inconsistencies between them. Moreover, given the chaotic, fast-changing nature of electric arcs, even the derived formulae for estimating arc voltage and resistance can produce substantially different results from those obtained from experimental measurements. While basic tendencies of electric arcs to change with arc current and gap distance are known, modelling of electric arcs is primarily done by adjusting formulae to match experimental data. Therefore, the suitability and accuracy of any arc model will greatly depend on the application at hand. Ultimately, the best approach is to use existing arc models as a starting point and tune them to suit the given application.

This section aims to accurately represent the arc model of the UFD referred also as the behaviour outside of the safe operating area (SOA). The SOA could be defined based on the chopping current (I_{chop}) and maximum withstand voltage V_{max}, i.e. $|I_{UFD}| \leq I_{chop}$ and $|V_{UFD}| \leq V_{max}$. While the UFD can enter open state and remain opened within the SOA, the opening under current larger than I_{chop} or stressing the contacts with voltage higher than V_{max} ignites an arc between the contacts. The arc creates a conducting plasma channel in the gaseous insulating medium and the UFD remains a closed circuit with resistance R_{arc} despite its contacts being physically separated. I_{chop} is dependent on the arc quenching medium and contacts material. Therefore, in the specific design of the UFD, it could be considered as a constant parameter. This value is typically small, e.g. I_{chop}=1 A in SF_6 [35], while in a hypothetical air UFD I_{chop}= 0.5 A. The value for chopping current is adopted based on initial

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experiments and it is not studied analytically. V_{max} is solely dependent on the dielectric conditions and is represented as:

$$\boldsymbol{V_{max} = z_g E_d n_{bp}} \quad (1)$$

$$z_g = \begin{cases} 2z - z_{ovl} z \geq \frac{z_{ovl}}{2} \\ 0 z < \frac{z_{ovl}}{2} \end{cases} \quad (2)$$

where, z_{ovl} is the overlap of the contacts in closed state, z_g is the gap distance, E_d is the dielectric strength of the insulating medium and n_{bp} is the number of breaking points used to provide the required insulation-distance for TIV within a compact design. As an example UFD design in [35] uses 4 breaking points (parallel contacts attached to the same rod) to facilitate shorter travel distance for the main rod and therefore reduced opening time.

The implementation of the electric arc in the UFD model is shown in Figure 2.3. S_1 is open if the UFD's contacts are separated ($z_g > 0$) and there is no arcing, otherwise it is closed. The arc is active (*Arcing*=1) if the contacts are separated and $|I_{UFD}| > I_{chop}$ or $|V_{UFD}| > V_{max}$. The theoretical arc resistance R_{arc0} could be continuously determined from the current magnitude and gap distance. The actual arc resistance is obtained by multiplying R_{arc0} with the *Arcing* signal. By setting *Arcing* to 1, resistor R_{arc} obtains a non-zero value which changes according to the grid conditions.

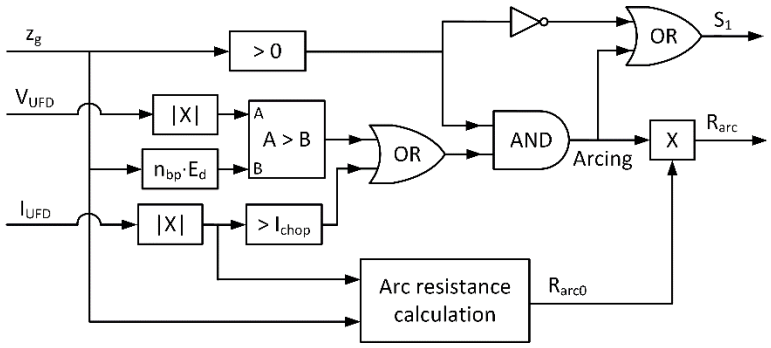

Figure 2.3 UFD arc model structure

The calculations for R_{arc0} is dependent on the type of the insulating medium. For an air-insulated UFD (5kV lab UFD), R_{arc0} is determined based on Paukert's arc model, using compilation of arc voltage measurements reported in [36].

$$\boldsymbol{V_{arc} = A\, I_{arc}^{B}} \quad (3)$$

where I_{arc} is the arc current; A and B are empirically determined constants for an air-gap distance and current-range. The need for separate Paukert's coefficients at high and low currents is related to the phenomenon that the arc voltage increases with current in the high current range but decreases with the current in the low current range (negative resistance) [37] The transition current at which this occurs in the Paukert's model is assumed as I_t =100 A [36].

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In its original form, Paukert's arc model is not suitable since both the gap distance and current magnitude change dynamically in the UFD operating conditions. It is therefore necessary for A and B to change as well. In order to ensure smooth transition between various Paukert's coefficients, an interpolated Paukert's model is proposed.

The Paukert's coefficients A_1, B_1, A_2 and B_2, defined at the air gap distances of z_{g1} and z_{g2}, respectively and belonging to the same current range, are used to determine the interpolated Paukert's coefficients as follows:

$$\boldsymbol{A_{12} = A_1 + \frac{A_2 - A_1}{z_{g2} - z_{g1}}(z_g - z_{g1})} \tag{4}$$

$$B_{12} = B_1 + \frac{B_2 - B_1}{z_{g2} - z_{g1}}(z_g - z_{g1}) \tag{5}$$

This interpolation makes A_{12} and B_{12} continuous smooth functions of z_g so that (3) covers a wide range of UFD air-gap distances. The coefficients A_1, B_1, A_2 and B_2 are defined separately for currents above and below the transition current I_t. In order to combine two operating ranges into one smooth function, transition function $O(I_{arc})$ is defined as follows:

$$\boldsymbol{O(I_{arc}) = exp\left[-\left(\frac{I_{arc}}{I_t}\right)^2\right]} \tag{6}$$

The finalized interpolated Paukert's model is given as

$$\boldsymbol{V_{arc} = [1 - O(I_{arc})]\, A_H I_{arc}^{B_H} + O(I_{arc})\, A_L I_{arc}^{B_L}} \tag{7}$$

where A_H, B_H, for high current ($I_{arc} > I_t$) and A_L, B_L for low current ($I_{arc} < I_t$) are interpolated coefficients A_{12} and B_{12}. When the current is low, $O(I_{arc}) \approx 1$ so $V_{arc} \approx A_L I_{arc}^{B_L}$. Conversely, when current is high, $O(I_{arc}) \approx 0$ so $V_{arc} \approx A_H I_{arc}^{B_H}$. The pre-calculated arc resistance is obtained by dividing (7) with I_{arc}:

$$\boldsymbol{R_{arc0} = [1 - O(I_{arc})]\, A_H I_{arc}^{B_H - 1} + O(I_{arc})\, A_L I_{arc}^{B_L - 1}} \tag{8}$$

Transforming the arc model from the voltage (7) to the resistance in (8) is advantageous because the resistance, unlike voltage, is independent of current direction. The validation of the air arc model has been performed on the 5kV UFD prototype (presented in the Appendix). The arc model parameters are obtained from [36] and summarized in Table 2.1. Figure 2.4 shows the experimental results with two test cases, i.e. opening at current of 200 A (high) and opening at current of 2.5 A (low). The arc voltages are calculated using (7), based on the position sensor (Figure 2.4 a) and current (Figure 2.4 b and c) measurements. These comparisons show a very good accuracy which validates the proposed air arc model. Figure 2.5 shows the photograph of the UFD and the contacts after the arcing test.

Table 2.1 Electric arc parameters in air for a 5kV UFD

Current	Gap distance	A	B
< 100 A	1 mm	36.32	-0.124

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	5 mm	71.39	-0.186
> 100 A	1 mm	13.04	0.098
	5 mm	14.13	0.211

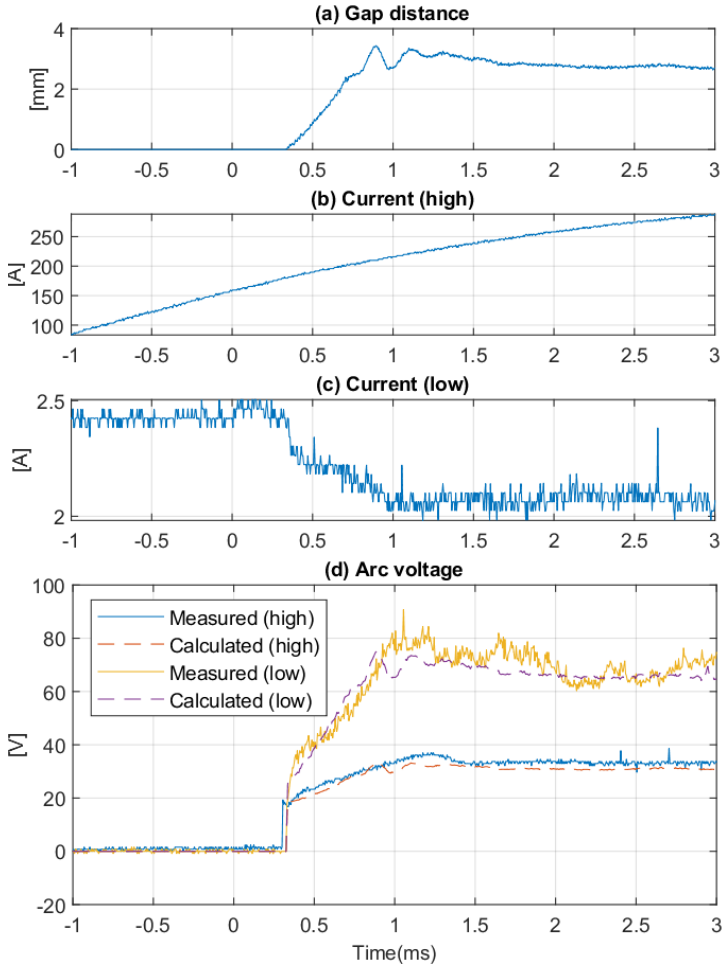

Figure 2.4 UFD air-arc model verification against measurements on 5 kV UFD

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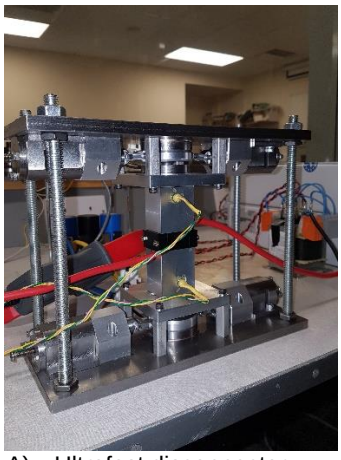
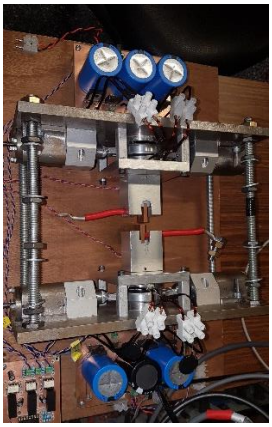


A) Ultrafast disconnector



B) UFD with open contacts

C) UFD contacts after arcing test

Figure 2.5 UFD and contacts after arcing test.

2.4.2 320 KV UFD ARC MODEL

For high-voltage applications, the UFD contacts are surrounded by sulphur-hexafluoride (SF_6) rather than air [35]. The high dielectric strength of SF_6 leads to a smaller distance between contacts and shorter operating time [38]. Despite its widespread use in the electric power industry, the reported knowledge about SF_6 arc modelling is limited, contrary to the arcs in air where comprehensive experimental data is publicly available [36][37].

The structure used here is similar to that used for 5 kV as shown in Figure 2.3. However, the behaviour of the arc voltage and the resistance model in SF_6 is different. No SF_6 UFD is available for testing however some researchers have reported test results for SF_6 load transfer switch in literature [39][25], which will be used for verification.

A study on SF_6 arcs in DC disconnectors (in the function of a load transfer switch) concluded that the arc voltage at a fixed-gap is generally independent of the current magnitude [39][25][26]. The same conclusion has also been reached in earlier studies on SF_6 arcs [37]. It is assumed that the behavior of SF_6 arcs in conventional disconnectors is similar to the behavior of arcs in UFDs, and the structure of the arc model from [39][25][26] is adopted.

Considering the data presented in [25][26], it is evident that SF_6 arc voltage V_{arc} greatly depends on the gap distance z_g, and an analytical expression is derived as:

$$\boldsymbol{V_{arc} = 14.3 + 12.33 \cdot z_g^{0.64}\ [V]} \tag{9}$$

where z_g is given in mm. By dividing (9) with the arc current I_{arc}, the expression for SF_6 arc resistance is obtained as follows:

$$\boldsymbol{R_{arc0} = \left(14.3 + 12.33 \cdot z_g^{0.64}\right) \cdot I_{arc}^{-1}} \tag{10}$$

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The PSCAD test system for evaluation of the high voltage arc model based on (10) is developed and shown in Figure 2.6. It consists of two variable DC voltage sources V_1 and V_2 with series RL impedance. V_1 and V_2 represent two DC terminals in a VSC-based DC grid while the RL impedance represents a DC cable with a terminating inductor. In practice, the two DC voltages at cable ends can take a wide range of dynamically changing values, depending on the type of VSC converters, type of faults, and the protection system employed.

The key aspects that need to be verified are entering and exiting the arcing mode, as well as the value of the arc resistance. Two test cases from Table 2.2 are performed to evaluate the behaviour of the arc model,

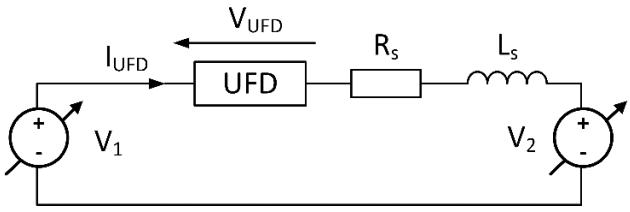

Figure 2.6 UFD test system

Table 2.2 Test system parameters for a 320kV UFD arc model

Parameter	Symbol	Test 1	Test 2
Series inductance	L_s	0 mH	100 mH
Series resistance	R_s	1 Ω	1 Ω
UFD chopping current	I_{chop}	1 A	1 A

The results of Test 1, simulating spurious opening under load current, are shown in Figure 2.7. V_1 and V_2 are kept constant throughout the test as indicated, while the series inductance is set to zero to speed up the current transient. The UFD opening command is given at 20 ms while the contact separation starts around 21.1 ms. The model enters arcing mode and the arc voltage increases with the increase of the gap and reaches 158 V at full separation. As the arc resistance increases, the current through the UFD decreases from 2 to 1.85 kA. Without corrective action from the control system (a change in source voltages), it is visible that the arcing in the UFD can cause a substantial change in the steady-state load current because the voltage difference between the terminals is typically low. However, the rate of change of current in the actual system may be much lower because of the cable and DC CB inductances. The arc resistance is shown to correctly adjust to provide the arc voltage defined in (**9**) based on the arc current and contact separation distance. The model is also shown to accurately enter the arcing mode due to opening under high current.

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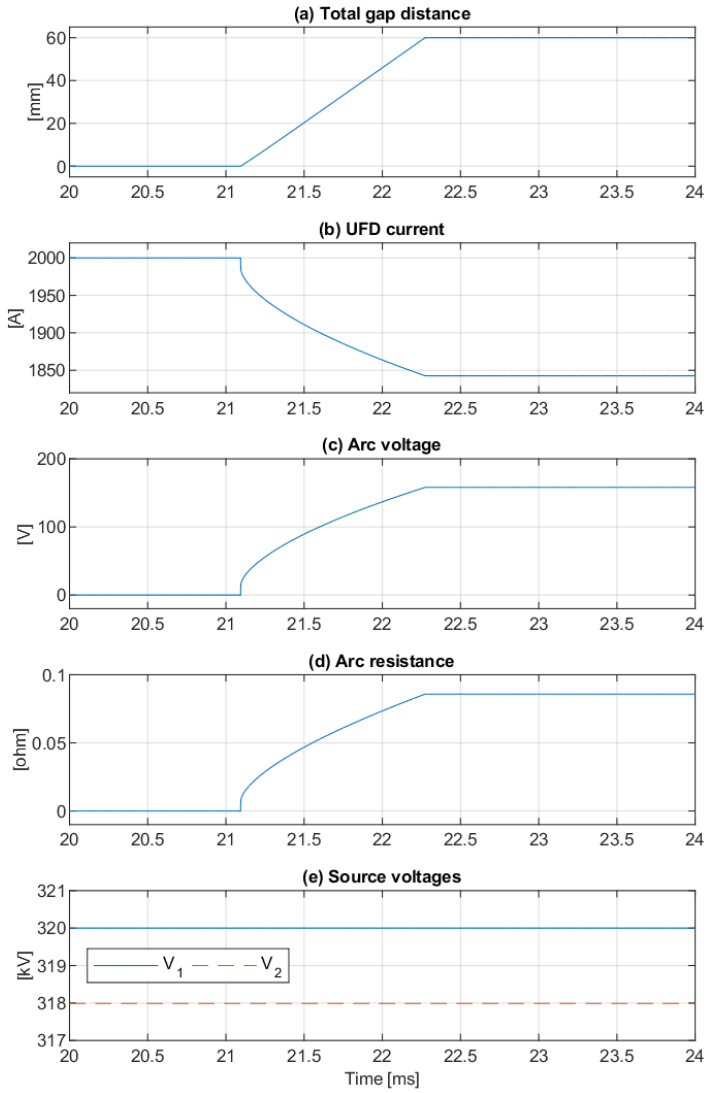

Figure 2.7 Simulation of attempted 320 kV UFD opening under load current.

The results of Test 2, shown in Figure 2.8, demonstrate: 1) entering arc mode on high current, 2) exiting the arc mode on low current and 3) re-entering the arc mode on overvoltage (dielectric breakdown).

A DC fault condition with negative pre-fault current of -2 kA is assumed at 21 ms. At 21.1 ms, the UFD's contacts separate but, because $I_{UFD} > I_{chop}$, an arc is ignited between the contacts. The current is increasing at 3.2 kA/ms. At 21.63 ms, I_{UFD} falls below I_{chop} and the arc is temporarily extinguished, as seen by the spike in UFD voltage. However, at this point the contacts have not separated sufficiently to provide blocking voltage to satisfy $V_{UFD} > V_{max}$ and a restrike occurs. The arc is reignited and the arc voltage continues to rise until full contact separation. Figure 2.8 shows the total source voltage ($V_1 - V_2$), as well as the UFD's actual voltage (V_{UFD}) and the maximum blocking voltage (V_{max}).

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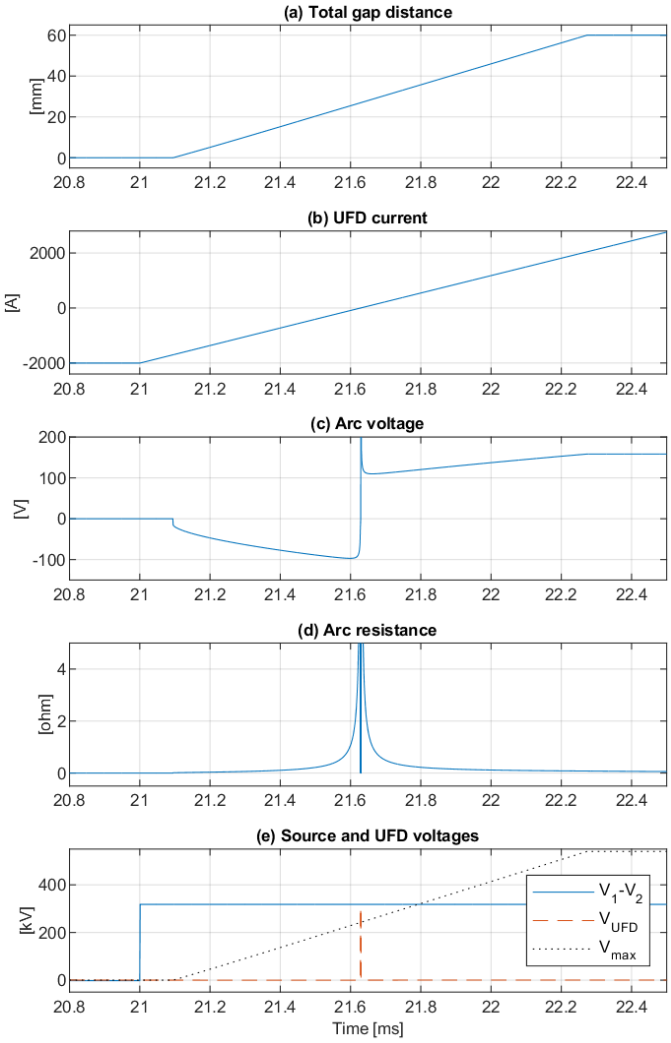

Figure 2.8 Simulation of SF_6 UFD model entering and exiting failure mode

In order to assess the model's wider applicability, the differences between the lab-scale and full scale of UFDs are listed as follows:

- The operating mechanism in both cases are identical based on Thomson coil. However, the size of mechanism, coil turn number, contact weight, the required electromagnetic force, and the parameters related to the bi-stable spring parameter are different.

- In case of full scale UFD, the number of breaking points is higher and this might introduce some non-linearities in the equation for dielectric strength between contacts.

- The use of SF6 as insulator may introduce some difference in the arc voltage profile. While this voltage is dependent on the distance between the contacts in both cases, it is minimally dependent on the current level, and this dependence is smaller in the SF6 arc quenching medium.

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2.5 FAILURE OF THE MAIN BREAKER

As it is studied in [9], once the LCS is switched off, the current is commutated to the MB path and the UFD could subsequently isolate the LCS. At this time the MB can interrupt the fault current and commute the current into the energy absorber. Subsequently, the fault energy will be absorbed and the current reduces [24].

In order to evaluate the failure of the MB, an understanding of its components is necessary. The valve in the MB module of a hybrid DCCB will be similar to one (of 6) valves in the first generation of 2-level VSC HVDC converters [9]. It consists of a string of series connected IGBTs of the press-pack design. These valves operate at around 1kHz switching frequency in the VSC HVDC converter. Also, the switching transients are optimised for low losses which means they are very fast. Inside the DCCB, there is normally requirement for a single turn off operation although operators may specify multiple O-C cycles. The fault current limiting is also possible for a short time [9]. The turn off transient need not be particularly fast and turn off loss is of no relevance. The stress conditions inside a DCCB are therefore lower than in the VSC converter. Nevertheless the peak interrupting current is higher than it would be the case in a VSC converter, which is achieved by operating DCCB valve from cold state [11]. In case of a bidirectional hybrid DCCB, two valves are required which are connected in series in the opposite directions.

To ensure equal voltage sharing in the open state, grading resistors may be employed across each semiconductor [9]. In comparison with other technologies, press-pack IGBT devices are a more appropriate choice, since they can provide the highest current ratings and lowest parasitic inductances. Their use of established pressure-contact technology fulfils high-reliability and an inherent short-circuit failure mode, due to the absence of wire bonds. Moreover, 40-year design lifetimes are expected for these switches [40] [41]. During the turn-off transient, voltage sharing on IGBTs is normally achieved using active gating [43]. This method relies on a driver-based voltage feedback loop which adjusts the transistor base voltage in response to any deviation from the expected values.

The failures of MB will be investigated using two approaches, i.e. a unit failure, and whole valve failure.

2.5.1 UNIT FAILURE IN MAIN BREAKER

As discussed in the section 2.3, the most commonly expected failure type is a short circuit fault of single IGBT. In order to avoid the impact of single unit short-circuit failure on the performance of the systems, some redundant IGBTs are normally employed in each valve. Redundancy is considered in the MB valves to improve the reliability of the valve, and failed modules need to be short circuited for a long time until replaced [42]. In fact, short-circuit failure mode is a required feature for these devices. In IGBT failure, the device should fail to short-circuit, as any unscheduled interruption of its operation is unacceptable. The reason lies in fact that IGBT fail open leads not only to current interruption, but also presents a risk of uncontrolled explosion caused by snubber rupture, both of which are unacceptable. Furthermore, this failure could result in an internal arcing between open contacts, leading to arc generation and pressure build-up within the device, which may lead to explosion. Figure 2.9 shows the outcome of such an explosion in a wire-bond module. If failure to a short circuit mode is not guaranteed by the IGBT design, alternative external bypass circuitry is required, adding cost, mass, size and complexity to the system [40] [42] [43].

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Figure 2.9 An IGBT module ruptured resulting from open-circuit failure [40].

2.5.2 WHOLE BRANCH FAILURE

Because of the use of an air-cooling system rather than water cooling, the IGBTs used in the MB cannot tolerate a high level of current for a long time. Therefore, valve overcurrent and temperature protection will play an important role. All semiconductors in a valve will be protected through driver level protection. This is a similar mechanism and the same circuit used for voltage balancing with active gating [43] [44]. The method is very fast and has negligible impact on the switching losses.

The MB branch may consist of multiple valve modules, which depends on the rated-voltage and required redundancy. The rating of breaking modules in commercial DCCBs has been 80kV [6]. Redundancy at breaking module level would be extremely expensive and perhaps unnecessary. A hybrid breaker with 3 (out of 4) healthy modules is still able to provide 320 kV blocking voltage but this can have an adverse effect on the energy absorbers, as discussed in section 2.6.

2.6 FAILURE OF ENERGY ABSORBER

The arrester banks are employed to build energy absorbers which provide energy dissipation and suppress the current [3]. A generic energy absorber consists of Ns series units which form a single arrester column and Np parallel columns. This structure, shown in Figure 2.10, is used to achieve the desired voltage, current and energy rating of the energy absorber. More precisely, their main functions are comprised of absorbing the magnetic energy stored in system's inductances (di/dt limiting inductors, arm inductors, line/cable inductance…) and providing counter-voltage to the sources feeding the fault in order to reduce fault current below the residual current level and facilitate opening of the residual current breaker (RCB). Surge arrester failure can be catastrophic for the DCCB (and the whole power system), rendering it unable to break fault current or causing destructive overvoltages and widespread hardware damage to other DCCB components.

The arrester behaves like a non-linear resistor with two operating regions, i.e. non-saturation and saturation. While the latter occurs at low voltage or current and it behaves like open circuit as a large resistor for this non-conductive region, the former occurs under high-current or voltage in which the arrester behaves like a small resistor.

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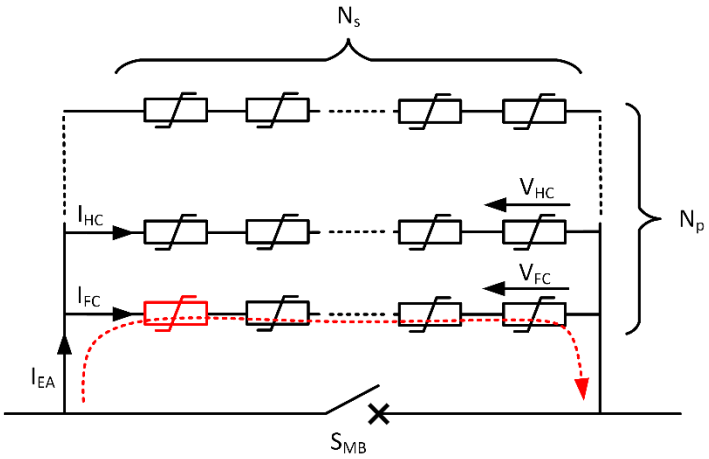

Figure 2.10 Energy absorber implemented as a bank of surge arresters.

The failure of surge arresters is well understood in common AC applications [29][30]. While the main origins of failures are environmental effects such as moisture ingress, contamination and ageing, the electrical and thermal stresses account for the rest. Surge arresters are usually degraded in a positive-feedback loop where the deterioration of the V-I characteristic occurs in the high-resistance region. It results in an increase of leakage current which, in turn, accelerates the ageing and further deterioration of the surge arrester. Once the thermal stability of the surge arrester is compromised, the resulting thermal runaway causes a dielectric breakdown in the arrester which flashes over and fails in a closed circuit. In DCCB applications, the absorbed arrester energy is much higher than in transient overvoltage protection applications in AC systems. Therefore, the energy absorber is typically constructed with many parallel columns, as shown in Figure 2.10.

The manufacturers will match the arresters in the energy absorber [3]. Nevertheless, as the characteristics of all arresters are not identical and the link connection amongst them could be imperfect, it is possible that one branch takes more current, and consequently suffers more thermal stress resulting in accelerated-aging [31]. The tests in WP10 reported that the DCCB energy absorber of 72 arresters can have over 30% difference in current stress between individual arresters [31], although it is noted that these arresters have not been matched.

The bank of arresters should be dimensioned and designed in such a way that the failure of a single (or multiple) arrester would not lead to failure of the entire energy absorber. In an extreme case of multiple simultaneous failures, the corresponding branch would draw excessive current, potentially leading to a cascaded failure of the other arresters in the same branch. As the pressure builds up inside the arresters, they can rupture and physically separate into multiple parts [29][30]. A failed arrester remains a closed circuit even when ruptured, because the current passing through it ignites an arc between the debris. In DC systems, the arc persists until backup protection clears the fault since there is no natural current zero crossing. In order to investigate the impact assessment of the arrester failures on the DCCB some experiments have been conducted in the DC laboratory as explained in the following section. In addition, some design and failure investigations have been provided in the last section.

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In WP10, tests have been performed on a bank of full-size arresters [31] and very interesting results have been obtained related to stress sharing. The study in this report will complement WP10 study, since it will be concerned with destructive testing of individual arresters and whole branch, but also the aim is to proposed new topologies that could ensure better reliability of absorber banks.

2.6.1 COMPONENT-LEVEL FAILURE OF SURGE ARRESTERS

In order to gain understanding of surge arrester's behaviour prior to and following the failure some tests have been conducted, as shown in Figure 2.11. A controllable voltage source (1000 V, 500 A) is used to apply the voltage across a single arrester Voltage (and current) is increased until the arrester fails (in short circuit). In addition, numerous V-I data points are captured to obtain the V-I characteristic. After the failure, the test is repeated at lower voltage to evaluate the V-I profile of a failed-SA. The arrester under test is EPCOS Metal Oxide Voltage Arrester, 75vrms B40K75, energy max: 190J. This arrester, shown in Figure 2.12 has the lowest voltage rating of the MOV type. While the material used in this arrester is representative of the those used in high-power arresters, the analysis in this section is predominantly qualitative due to differences in arrester construction.

Figure 2.13 presents the test results. As it can be seen, the healthy arrester has variable resistance between 100 Ω and 20 kΩ in the observed-range. However, the failed-arrester indicates a constant resistance of around 2 Ω.

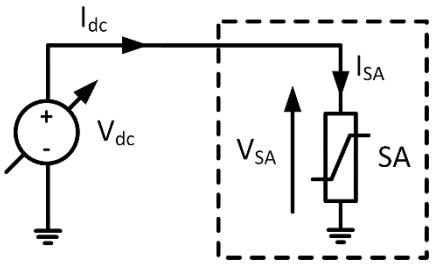

Figure 2.11 The test set-up for V-I characteristics of arrester.

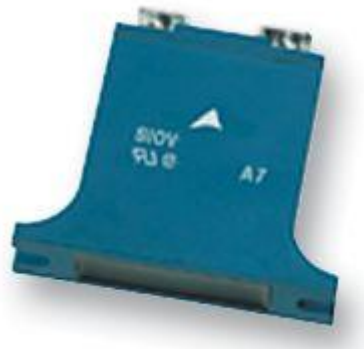

Figure 2.12 EPCOS Metal Oxide Voltage Arrester, 75vrms B40K75.

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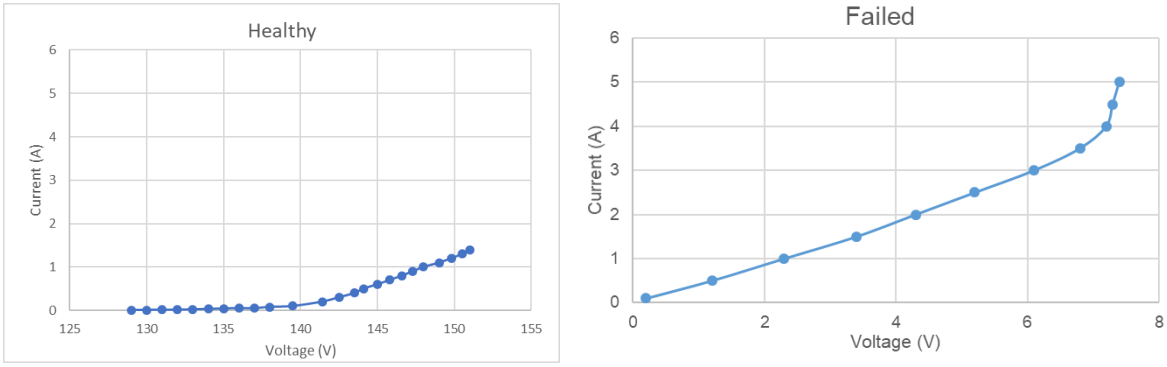

(a) (b)

Figure 2.13 The test results of V-I charachrestics a) healthy b) failure.

2.6.2 FAILURE OF ARRESTER BANK

A test set-up including 2×2 matrix connection of the SAs as shown in Figure 2.14 has been established to assess the impact of component failures in the surge arrester branch on the system-level performance of DCCB. The voltage and energy rating of the arresters ((EPCOS Metal Oxide Voltage Arrester, 75vrms B40K75, energy max: 190J) is much lower than it would be required in normally designed DCCB (as tested in [13]). This is purposely implemented in order to invoke arrester failure.

A capacitor bank from the DCCB test circuit is used to provide fault energy, which leads to a reducing voltage profile. The remaining test circuit and DCCB are described in [13]. As a safety precaution, a shunt arrester is added to protect the main breaker if arrester rupture causes an open circuit of the main arrester bank. The tests have been conducted into three scenarios, i.e. successful interruption, an arrester failure and full branch failure. A fault is applied, and the main breaker opens around t=1.8 ms. Variables shown are the source current and voltage (I_{dc}, V_{dc}), main breaker current and voltage (I_{T2}, V_{T2}) and individual arrester currents and voltages (I_{SAx}, V_{SAx}).

Figure 2.15 indicates the result of a successful breaking test. As it can be seen, once the main breaker opens at 1.8 ms, the current commutates into the two parallel arrester branches. The arrester voltages go to saturation state which in this case is quite low at around 380V. Subsequently, the current is decreased when the system voltage drops below the residual voltage of arrester and finally the RCB interrupts the leakage current. The figure also illustrates that there is notable difference between the currents in two otherwise identical arrester branches.

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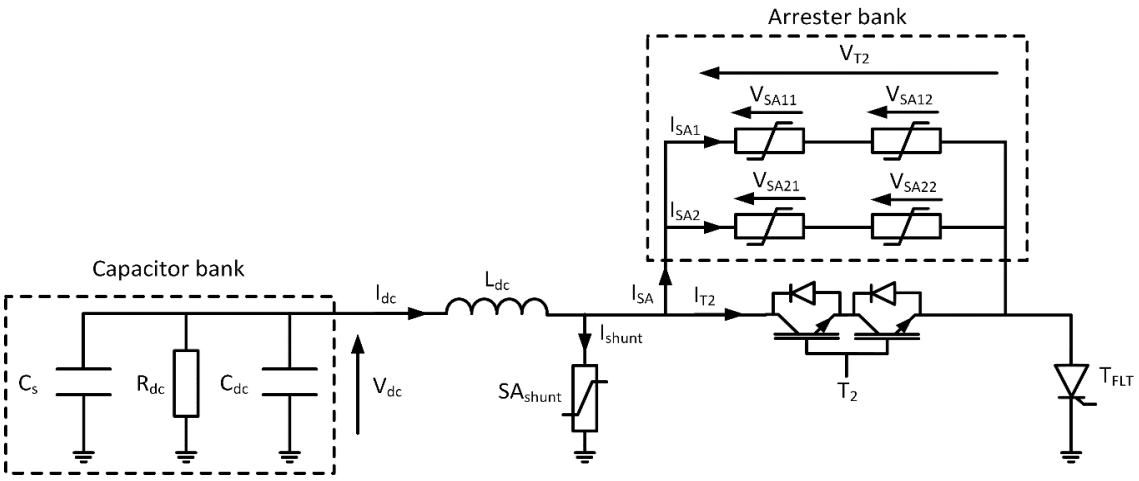

Figure 2.14 Test set-up for the main arrester bank failure.

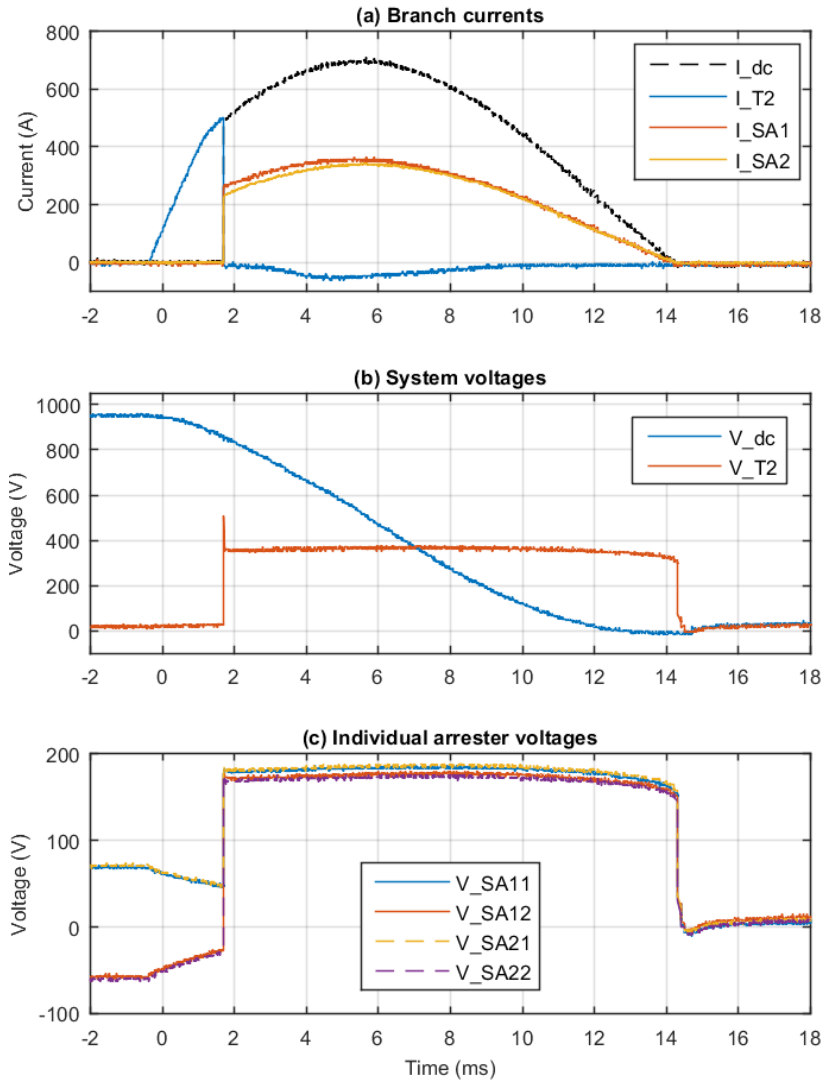

Figure 2.15 Successful current breaking operation.

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It was not possible to fail an arrester in this topology. A single arrester failure was achieved by using a single arrester instead of the 2x2 matrix which resulted in eventual arrester overload. The investigation is then carried out to evaluate if cascaded failure would be possible.

The failed arrester is inserted in the original 2x2 bank and the same test as in previous figure is repeated. The test is demonstrated in Figure 2.16. In the initial period when arresters are inserted (2-3.5ms) the branch with faulted arrester takes larger current. This leads to further overload of the remaining healthy arrester in this branch. This second arrester also fails (at 3.5 ms), and that branch then takes full the DC current. A change in the arrester voltage characteristic is apparent before and after this cascaded failure of a 2x2 surge arrester matrix.

This is important test since it demonstrates a possible cascaded failure of energy absorber. It is noted that the stress required for second arrester failure is significantly lower than that required for failing the first arrester (second arrester fails in 2x2 bank).

Note that there are small inaccuracies in these measurements caused by the magnetic interference between inductors and current probes. This is seen in the small negative T2 current as an example.

Figure 2.17 shows the PSCAD simulation of the DCCB opening with one failed arrester. It is seen that PSCAD model simply shows that failed branch takes full current and then, when voltage increase, the second arrester branch takes some current. This response is a result of overly simplified and inaccurate arrester models in PSCAD (10-point V-I curve) and warns that caution is required when simulating arrester banks.

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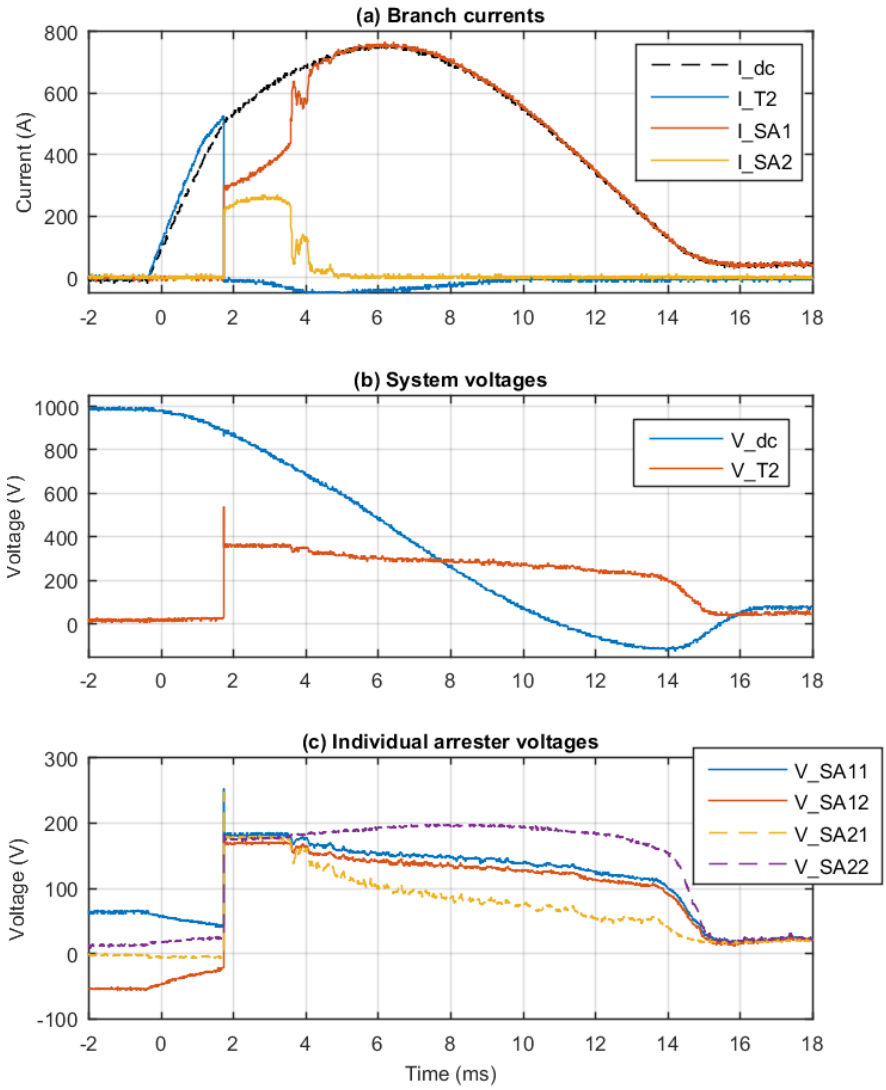

Figure 2.16 Demonstration of cascaded arrester bank failure during breaker opening.

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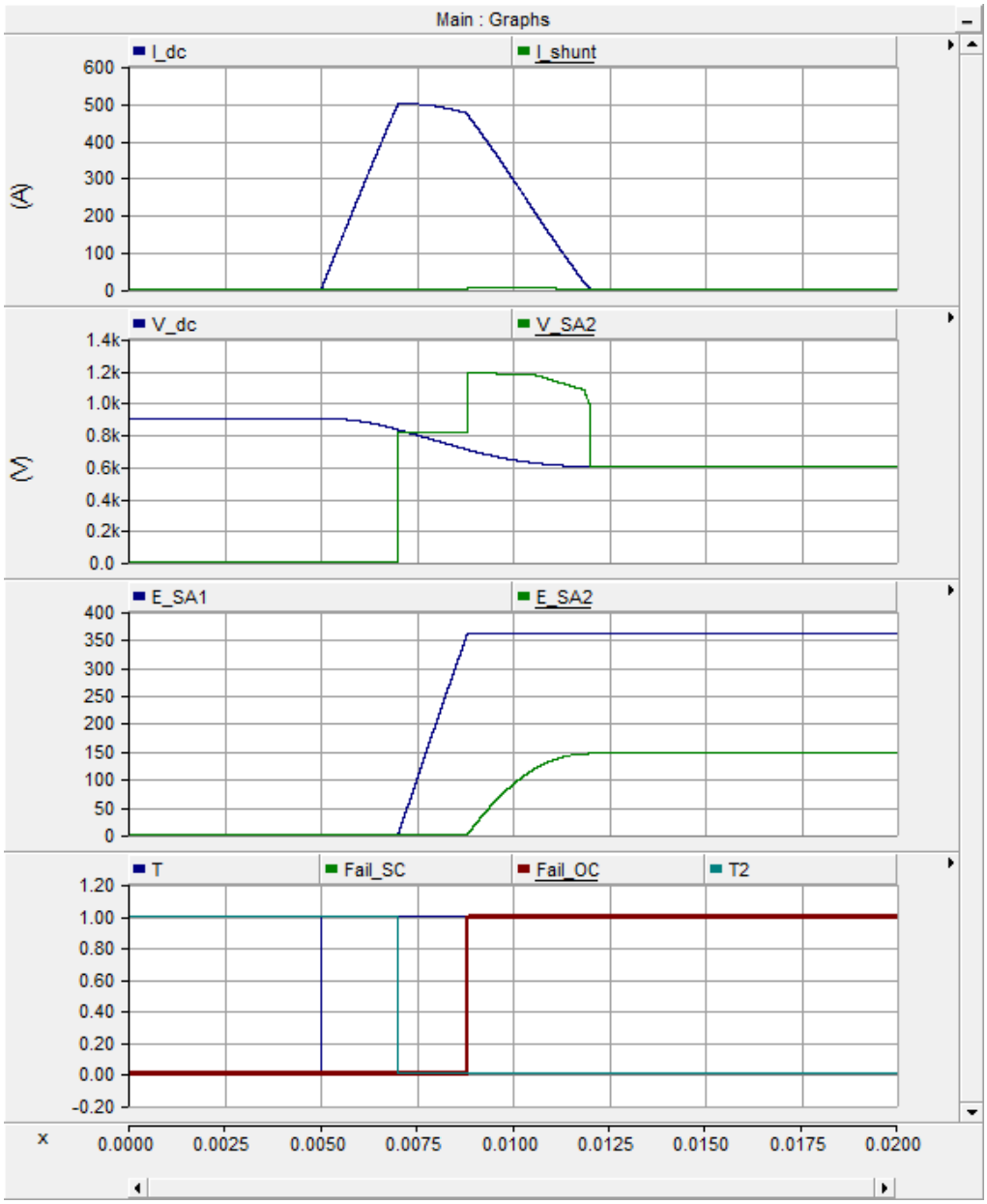

Figure 2.17 PSCAD model simulation of DCCB opening with one failed arrester.

In the last test, as shown in Figure 2.18, the test is repeated with failed arrester branch, that would represent undetected arrester failure. It is seen that the failed branch takes full current while current in the second branch is practically zero. The arrester counter voltage is less than ½ of the value for healthy arresters. The arrester bank (with 2 failed arresters) is shown in Figure 2.19.

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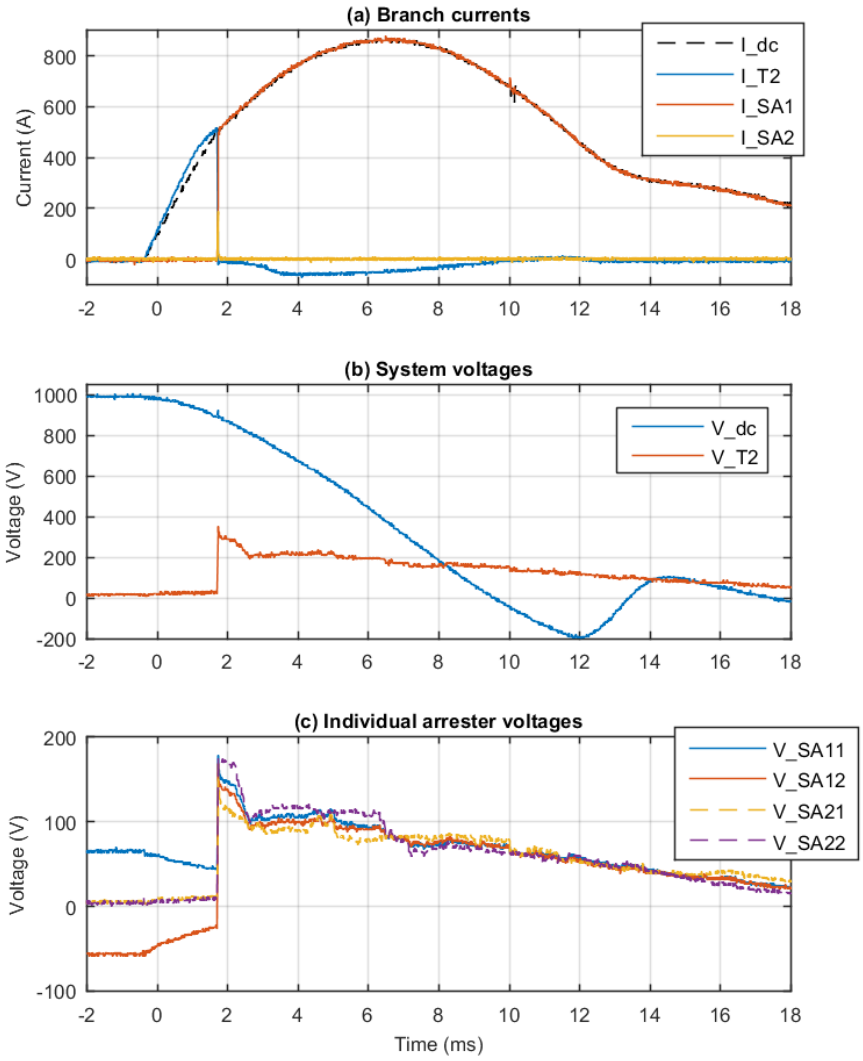
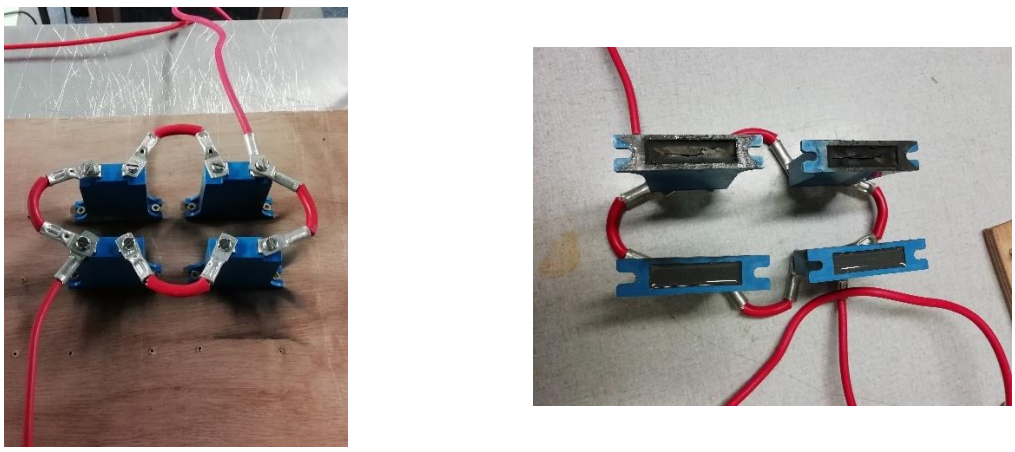


Figure 2.18 DCCB opening with failed arrester bank.



(a) (b)

Figure 2.19 Arrester bank with 2 failed arresters, (a): Top view, (b): Bottom view

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2.6.3 FAILURE OF LCS ARRESTER

The failure of LCS arresters can be caused if UFD fails to open. In order to experimentally demonstrate LCS arrester failure the test set-up has been established as shown in Figure 2.20. Accordingly, the UFD is replaced by a short circuit, simulating the case where a malfunction keeps the UFD closed while T1 opens normally during the opening operation. In these tests, the voltage rating of main arrester bank (SA2) is much higher than the voltage rating of T1 (600V) and its arrester (SA1). The arrester across T1 is much smaller and of different construction (B72220S0600K101 - TVS Varistor, MOV, 60 V, 85 V, Standard Series, 165 V, Disc 20mm). The same fault condition as in the previous section is applied and T2 turns off 2 ms after T1.

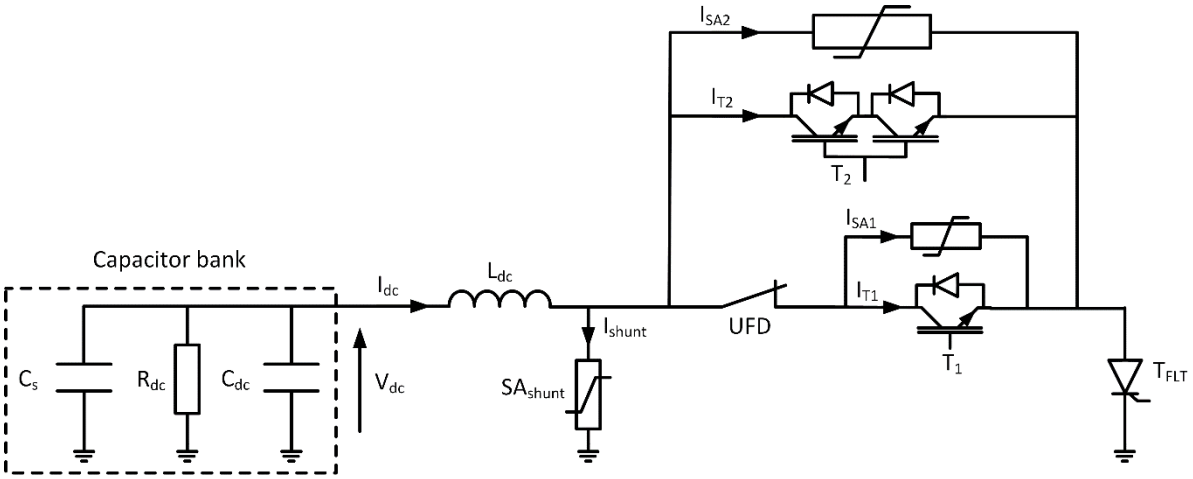

Figure 2.20 Test set-up for the evalution of LCS arrester failure (impact of UFD failure on arresters).

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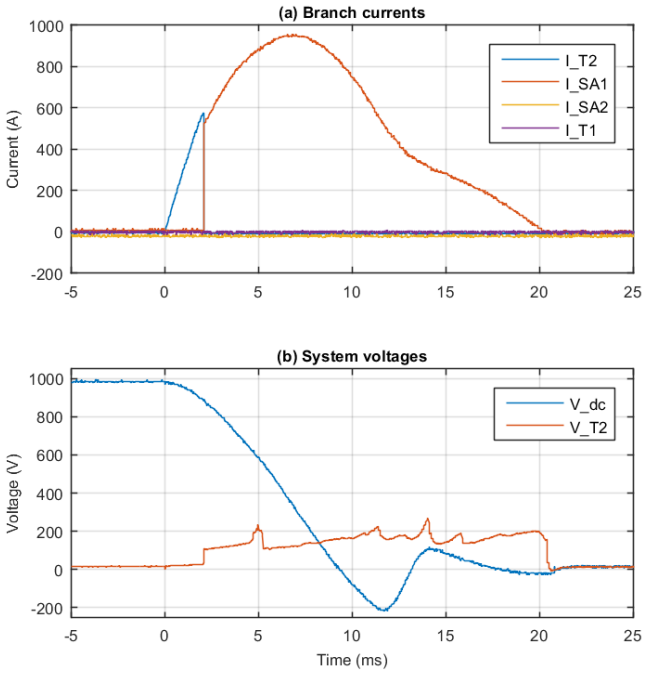
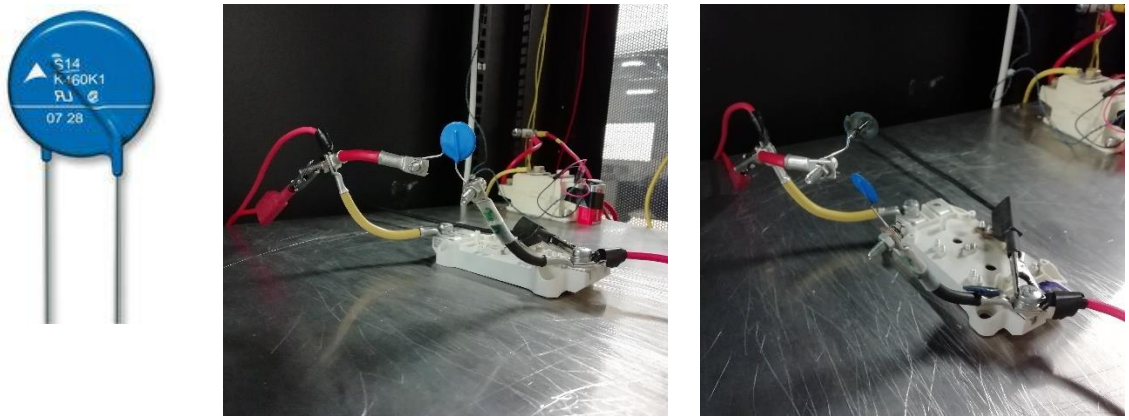


Figure 2.21 Test results for failure in UFD and LCS arrester

As it can be seen, once the T2 has been opened, T1 arrester takes full line current because of its low voltage rating and consequently, the arrester overloads and ruptures. Importantly, an arc ignites between the arrester's ruptured contacts which maintains low voltage across T1. In fact, the breaker remains a closed circuit and T1 did not fail in this test. Figure 2.22 shows the photographs of LCS and the arrester bank.

This test illustrates the importance of internal interlocking inside DCCB and status indication. A timely indication that UFD did not open would signify that DC CB is faulty and if such signal is sent to protection relay a backup protection should clear the fault before LCS arrester damage occurs.



(a) LCS arrester (b) LCS with arrester before failure (b) LCS with arrester after failure

Figure 2.22 LCS (Thyristor T1) and parallel arrester

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2.6.4 DESIGN OF EA BANK AND FAILURE EVALUATION FOR 320 KV DCCB

This section employs a PSCAD model of 320kV DC CB arrester bank and attempts to evaluate failure modes and to recommend design approaches for increased reliability. As it has been shown in Figure 2.10, it is assumed that the EA is implemented as a surge arrester (SA) bank with N_p parallel-connected columns, each column consisting of N_s series-connected individual SA units. It is assumed that SAs will normally fail in low-resistance state [32]. Consequently, failure of one unit leads to a decrease in the voltage of the corresponding column, and the column I-V curve shifts down. In fact, a small difference in the column's voltage could result in an immense difference in the current through that column owing to the low-slope I-V characteristic of SAs as it has been experimentally demonstrated in the previous section. This has also been explained as the important factor in building energy absorbers in [3]. To be more specific, Figure 2.23 compares two typical SA's I-V characteristics with the characteristic corresponding to 100% of the rated-voltage U_r and 90% of U_r. In case of parallel connection of these arresters and the applied-voltage of 1.8 p.u., the arrester with the 100% Ur and 90% Ur draw 35 A and 2000 A, respectively, i.e. a difference of 5700%.

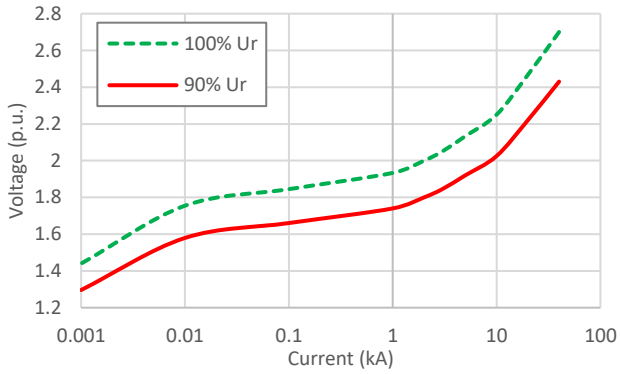

Figure 2.23 SA's I-V characteristic at normal and reduced voltage rating

This leads to the conclusion that failure of a single unit means that the corresponding column draws most of the EA current. With reference to Figure 2.10, this can be written as

$$\boldsymbol{I_{HC} \ll I_{FC} \approx I_{EA}} \tag{11}$$

I_{HC} stands for the current in the healthy column, while I_{FC} refers to the current in the column with a single unit failure. From (11), it is evident that a single-unit failure may lead to overloading of the healthy arresters in the same column. Therefore, there is possibility for a cascaded failure in which case the whole column becomes damaged and the breaker module short-circuited.

The input parameters (requirements) for the EA bank are shown in Table 2.3, which is used as the input to select suitable arresters and the number of parallel branches N_p which yields the desired TIV and prevent thermal overload of the arresters. The grid overvoltage coefficient (K_{OV}) is taken as 5%, which is the ratio between the maximum permissible DC voltage under normal grid operating conditions and the rated voltage level [45]. The peak TIV coefficient (K_{TIV}) is the ratio between the maximum DCCB voltage during the current interruption process and the nominal grid voltage, measured at the DCCB's rated short-circuit breaking current I_{pk}.

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Table 2.3 Input parameters for the EA design

Parameter	Symbol	Value
Rated voltage	V_{dcN}	320 kV
Rated short-circuit breaking current	I_{pk}	16 kA
Series DCCB inductance	L_{dc}	100 mH
Grid overvoltage coefficient	K_{OV}	1.05
Peak TIV coefficient	K_{TIV}	1.5
Number of breaker modules	N_m	4

The arresters are considered overloaded once the charge transferred during a single breaking operation exceeds their repetitive charge transfer rating Q_{rs} limitation. This criterion is more convenient as it is independent on the DCCB voltage rating and N_s. Moreover, Q_{rs} is a constant parameter for all the SAs within the same product series while the SA energy rating changes with U_r [32].

Referring to the Figure 2.10, the transferred SA charge is defined as

$$\boldsymbol{Q_j = \int_0^{T_s} I_j \, dt} \tag{12}$$

where j denotes the subscript of the branch or bank current, in this case FC, HC or EA. The main breaker opening occurs at $t = 0$ while T_s stands for the end of the fault current suppression period (when the residual current level is reached).

The rated TIV of the whole DCCB is calculated according to (13). Subsequently, assuming a firm DC bus voltage and flat EA current-voltage characteristic during the fault current suppression period, the L_{dc} current slope and the time to current zero from I_{pk} are obtained as (14) and (15), respectively. It is noted that firm DC voltage assumption is the worst case, while in practice voltage will drop somewhat leading to lower energy. The charge transferred through the EA between the main breaker opening ($t = 0$) and the current zero can be approximated as in (16)

$$\boldsymbol{V_{pk} = K_{TIV} \cdot V_{dcN}} \tag{13}$$

$$\frac{dI_{dc}}{dt} = \frac{V_{dcN} \cdot (K_{OV} - K_{TIV})}{L_{dc}} \tag{14}$$

$$T_0 = \frac{I_{pk} \cdot L_{dc}}{V_{dcN} \cdot (K_{TIV} - K_{OV})} \tag{15}$$

$$Q_{pk} = \frac{I_{pk} T_0}{2} = \frac{I_{pk}^2 \cdot L_{dc}}{2V_{dcN} \cdot (K_{TIV} - K_{OV})} \tag{16}$$

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For the given input parameters, Q_{pk} is calculated as 89 C. The rated TIV of a single breaker module is as follows:

$$\boldsymbol{V_{pkm} = \frac{K_{TIV} \cdot V_{dcN}}{N_m}} \tag{17}$$

where, N_m is the number of breaker modules. An arrester unit capable of providing V_{pkm} at I_{pk} is selected as PEXLIM P-Z with U_r of 54 kV [46][47]. It is noted that manufacturers may adopt specific purpose-built arresters which are not yet available on the market. The rated charge of this arrester is Q_{rs}=3.2 C while the I-V characteristic is shown in Figure 2.23 (100% U_r). The required number of parallel-connected arrester columns is calculated via (18) to be $N_p = 42$ considering a 50% margin to account for the uneven current distribution in the arrester bank and additional inductances in a DC system (MMC's arm inductors, cable inductances etc.).

$$\boldsymbol{N_p = \frac{1.5 \cdot Q_{pk}}{Q_{rs}}} \tag{18}$$

As the EA design is an iterative process since any change in N_p changes the non-linear voltage characteristic of the arrester bank, the values of $U_r = 54\ kV$ and $N_p = 42$ are considered as the starting point for the parameter optimization. The final EA design is obtained through iterative PSCAD simulations, with the final parameters shown in Table 2.4. It is worth noting that Q_{rs} is identical for the whole arrester column as for an individual arrester unit, and that Q_{rst} is identical for the whole DCCB as for a single breaking module.

To verify the EA design, four breaker modules with EA parameters from Table 2.4 are subject to a breaking with $V_{dc} = 336kV$ (1.05 p.u.) while $I_{th} = I_{pk} = 16$ kA. Table 2.5 compares the extracted performance indicators, given for the whole DCCB as well as a single module. Except for the peak TIV, the values of the remaining indicators are taken at the instance where dI_{dc}/dt becomes equal to -1 A/ms, signaling the end of the fault current suppression period. The peak TIV of the breaker is reasonably close to the 1.5 p.u. target while the absorbed charge per column, factoring in a 50% margin, is less than Q_{rs}.

Table 2.4 Final EA parameters for a single DCCB module

Parameter	Symbol	Value
Rated column voltage (per module)	U_r	66 kV
Number of parallel columns	N_p	40
Repetitive charge transfer rating (per column)	Q_{rs}	3.2 C
Repetitive charge transfer rating (total)	Q_{rst}	128 C

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Table 2.5 Main characteristics of test energy absorber

Performance indicator	Whole DCCB	Single module
Peak TIV	494.44 kV (1.55 p.u.)	123.6 kV (0.39 p.u.)
Absorbed charge per column	2.08 C	2.08 C
Absorbed charge per column (with 50% margin)	3.12 C	3.12 C
Total absorbed charge	83.17 C	83.17 C
Total absorbed energy	40.66 MJ	10.2 MJ
Fault current suppression time	11 ms	11 ms
Residual current level	35.4 A	35.4 A

In order to evaluate reliability of EA with single unit failure, the following circuit shown in Figure 2.24 has been simulated in PSCAD. This system is comprised of a strong DC bus with the added DCCB and line inductances, and four ideal series-connected DCCB modules (N_m=4) which are simultaneously operated when the line current exceeds a predefined threshold I_{th}. Each SA bank consists of $N_s \times N_p$ individual SAs, as shown in Figure 2.10. Increasing the number of series-connected units leads to a more uniform current distribution within the EA module. The reason lies in fact that if the failed SA unit is considered as a short circuit, the voltage distribution on remaining healthy units are dependent on the number of these units.

It is assumed that a SA unit fails in an ideal short circuit [32]. The relationship between the voltage of a single SA in the healthy column (V_{HC}) and the voltage of a single SA in the partially-failed column (V_{FC}) is given as

$$\boldsymbol{V_{FC} = \frac{N_s}{N_s - 1} \cdot V_{HC}, \quad N_s \geq 2} \tag{19}$$

It is seen that the voltage on a single healthy unit in the failed column increases because the number of units sharing the voltage decreases. This in turn causes the failed column to draw much higher current and may cause cascaded unit failure. From the above equation it is evident that the difference between V_{FC} and V_{HC} decreases with N_s. Therefore, increasing the number of series-connected units leads to a more uniform current distribution within the EA module and alleviates this issue.

Figure 2.25 demonstrates the impact of a single-unit failure on the currents of the faulted column (I_{FC}), a healthy column in the faulted module (I_{HC}) and a column in a healthy module (I_{HM}). The column voltages, absorbed charge and energy are also shown. The abbreviations used in labelling of these variables are: FC – failed column, HC – healthy column and HM – column in a healthy module. The results are compared against the base case with no SA failures, while $N_s = 5$.

In comparison with the variables for the healthy columns, current, charge and energy of the units in the failed column are two orders of magnitude higher and hence cannot be properly shown on the same graph. The peak values of these variables in the observed time period are 11.57 kA, 2.11 MJ and 72.66 C, respectively. The discrepancy between I_{th} and peak I_{FC} arises because a small resistor (1.25 mΩ) is connected in series with each

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arrester column to suppress the PSCAD short-circuit check error. Consequently, the current distribution at the very beginning of the fault current suppression period may not be accurately represented.

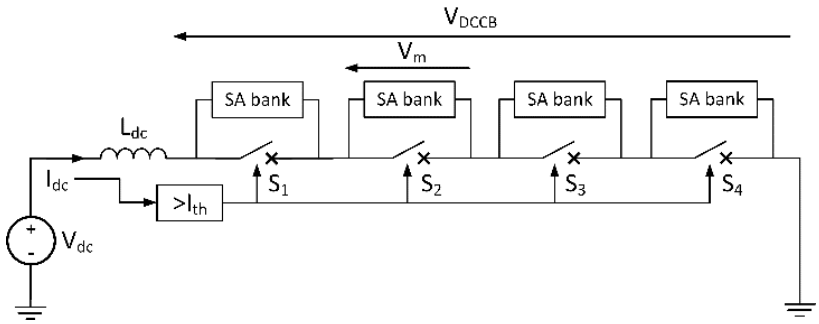

Figure 2.24 Test system for EA characterization

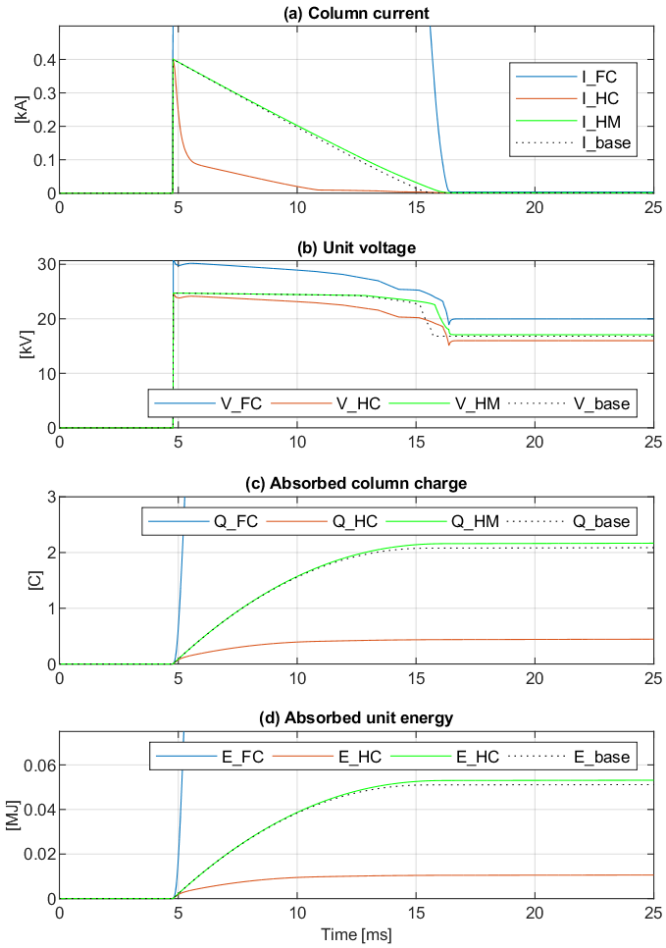

Figure 2.25 Time-domain responses for a single SA unit failure (Ns=5).

Figure 2.26 shows the relationship between the absorbed charge per column and the number of series-connected units. Only a single unit failure is simulated, however, the figure also encompasses the cases of multi-unit failures. The numbers in brackets below N_s indicate the percentages of failed units in a column. A case of $N_s = 5$, for example, illustrates a 20% column failure and is equivalent to a two-unit failure at $N_s = 10$ or a four-unit failure at

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$N_s = 20$. A comparison is made between the base case with no failures (Q_{base}), as well as the repetitive charge transfer rating (Q_{rs}).

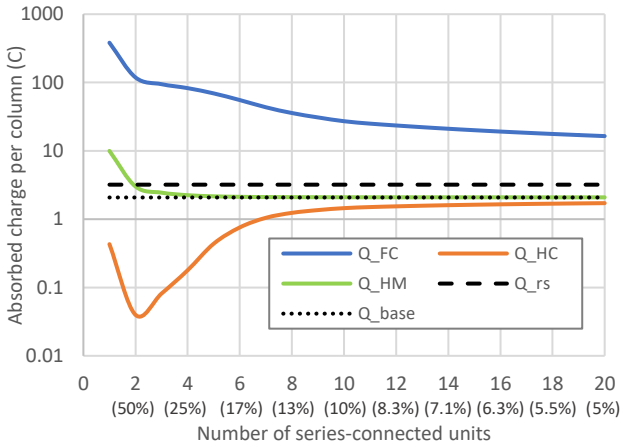

Figure 2.26 Absorbed charge per column in case of a single unit failure

Even with a high N_s, Q_{FC} is several times higher than both Q_{base} and Q_{rs}. This implies that a cascaded failure is probable in a real module. Considering the SA thermal constants, it is very likely that one or more units would fail in one opening, but perhaps not the whole column. However, the failure of each additional unit would increase the proportion of EA current flowing through that column and exacerbate the overloading of healthy units, increasing the probability of a complete column failure.

In order to prevent the cascaded failure of arrester units in a failed column ($Q_{FC} < Q_{rs}$), a series connection of at least 135 units is required. It is highly unlikely that such a design would be feasible in practice because of limited voltage rating (commonly around 6kV) for commercial SA units [31]. It can be concluded that by merely increasing N_s, it would be difficult to enhance the reliability of EAs.

The above study indicates that the failure of one unit would likely lead to a failure of an entire column, and this implies the failure of one module. Figure 2.26 shows that, in the case of a complete module failure (case of $N_s = 1$), the charge on a column in another healthy module reaches $Q_{HM} = 10\ C = 3.125\ Q_{rs}$, i.e. more than three times the rated charge. Therefore, the failure of an arrester column, caused by the failure of a single arrester unit, would possibly lead to the failure of the remaining three healthy modules.

Further investigation has revealed that $Q_{HM}(N_s = 1) < Q_{rs}$ when $I_{th} < 8.45\ kA$. Therefore, the DCCB could in theory absorb the fault energy using only three modules without overloading them if it opens under the current of less than 8.45 kA. However, the residual current level when only three modules are inserted is 334 A (compared to the rated 35.4 A) which implies that the RCB would not be able to open and the arresters would eventually overload, unless the backup protection in the DC grid acts and isolates the fault.

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A potential remedy to this problem is increasing the number of breaker modules. The higher the number of modules, the smaller the peak TIV reduction that occurs in case one module fails. The relationship between the peak TIV of a healthy breaker ($V_{pk}(N_m)$) and the one with a single module failure ($V_{pk}(N_m - 1)$) is

$$V_{pk}(N_m - 1) = \frac{N_m - 1}{N_m} \cdot V_{pk}(N_m) \tag{20}$$

It is evident that increasing N_m reduces the difference between the healthy and the partially failed DCCB.

The test of a single column failure from Figure 2.26 is repeated using five modules while the voltage rating of each module is scaled by 0.8 to provide the same cumulative TIV. A comparison between the main performance indicators for a four- and five-module DCCB under a single module failure is given in Table 2.6. The base case from Table 2.5 is also provided for the reference.

Table 2.6 EA performance indicators under a single module failure depending on the number of modules

Performance indicator	4 modules	5 modules	No failure
Peak TIV	371.93 kV (1.16 p.u.)	396.63 kV (1.24 p.u.)	494.44 kV (1.55 p.u.)
Absorbed charge per column	9.99 C	5.65 C	2.08 C
Total absorbed charge	399.47 C	226.16 C	83.17 C
Total absorbed energy	147 MJ	88.79 MJ	40.66 MJ
Fault current suppression time	58.7 ms	32.7 ms	11 ms
Residual current level	334 A	213 A	35.4 A

Increasing the number of modules from four to five increases the peak TIV in case of a single module failure by 0.075 p.u. Although the difference is seemingly low, it results in a considerable reduction in the absorbed charge, energy, fault current suppression time and residual current level. While all measurements indicate that a five-module breaker would still be overloaded, there is substantial reduction in the module stress. Because the cost of a single module is highly dependent on the voltage rating, increasing N_m is not likely to produce significant cost penalties if the voltage rating of each module is proportionally reduced. Nevertheless, utilizing high N_m may exacerbate the challenges of voltage balancing during simultaneous module opening. In order to ensure that Q_{rs} is not exceeded, $N_m \geq 9$ would be required.

The problem of highly uneven current distribution in SA banks under a single unit failure can be tackled by employing parallel interconnectors between columns, as shown in Figure 2.27. It is proposed that the interconnectors are inserted between every row of SA units, resulting in full meshing of the arrester bank. When a single SA unit fails, the circuit ensures that the corresponding row is bypassed. The implicit assumption is that the failed unit can take full load current, which has been confirmed in experimental studies in Figure 2.16. Since an equal number of healthy arresters remains inserted in the current path in each column, $V_{FC} = V_{HC} = V_{HM}$, now there is no discrepancy between column currents. Consequently, $Q_{FC} = Q_{HC} = Q_{HM}$, except for the bypassed row where the failed unit conducts majority of the current.

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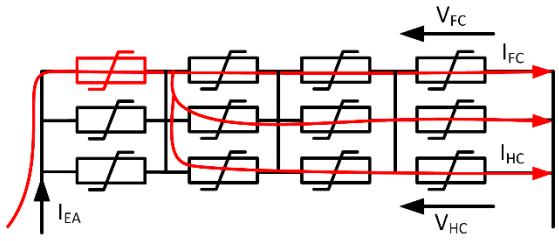

Figure 2.27 Surge arrester bank with parallel interconnectors

The time-domain response for a single-unit failure with $N_s = 5$ in a SA bank with interconnectors is shown in Figure 2.28. As expected, there is no difference between the voltages of healthy arresters in the failed and healthy column. No further overload occurs and cascaded failure is unlikely.

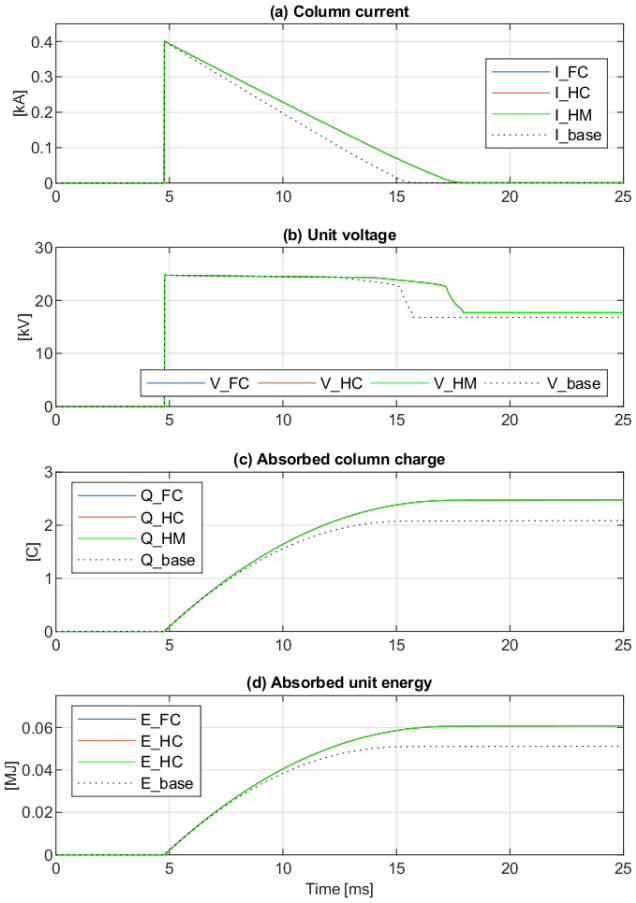

Figure 2.28. Time-domain responses for a single SA unit failure with in a SA bank with interconnectors, (Ns=5).

Figure 2.29 illustrates the impact of increasing N_s on the absorbed column charge when the interconnectors are used. For $N_s \geq 3$, $Q_{FC} < Q_{rs}$ which means that a cascaded failure will not occur if the number of series-connected units is 3 or more. As the N_s grows larger, the diminishing returns are evident. For $N_s \geq 9$, the difference between Q_{FC} and Q_{base} is less than 10% and further increase in N_s has no value.

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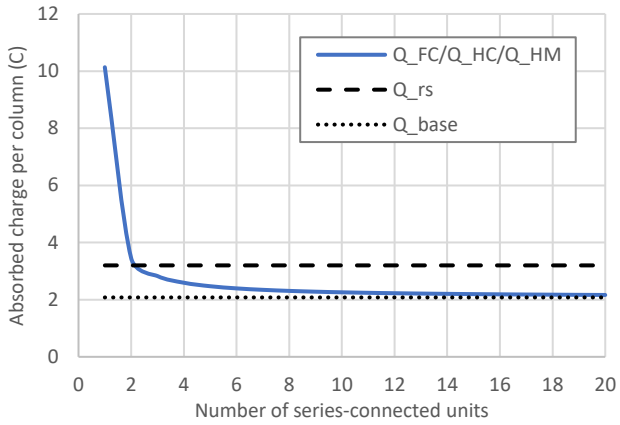

Figure 2.29. Absorbed charge per column in case of a single unit failure in a SA bank with interconnectors

The potential downside of utilizing the meshed layout of SA banks is that such design pronounces the differences in individual arrester I-V characteristics and promotes a more uneven current distribution. The imperfections in individual SA units cancel each other out in topologies with long columns. In a fully meshed configuration, higher current always flows through the arrester unit with the lower voltage rating which could hasten the failure of these units. Nevertheless, this is not likely to be a major drawback of the meshed EA topology since N_s will in most cases be very low (2 or 3 is sufficient to prevent cascaded failure). Moreover, manufacturers will ensure that units are matched prior to installation. Another challenge is the mechanical design of meshed interconnectors which should be of low-inductance.

2.7 FAILURE OF RESIDUAL CURRENT BREAKER

After fault clearance, the RCB interrupts the residual current and isolates the faulty line from the HVDC grid to protect the arrester banks of the hybrid HVDC breaker from thermal overload. Disconnecting RCBs and the series reactor can be installed outdoors, which significantly reduces the size of the valve hall required for the hybrid HVDC breaker [48]. Once the DCCB is in a close state, an unwanted opening operation of RCB leading to an arc in this breaker and an explosion could happen. Although from reliability viewpoint, the DCCB is taken as a close component, the backup protection needs to operate.

During the opening, the critical factor that influence successful opening of RCB is the level of leakage current in energy absorber. In the previous section in Table 2.6 it has been illustrated that normal leakage current is 35A while in case of a single arrester failure it may increase to over 300A. It may not be possible to substantially overrate RCBs since these are conventional AC CB breakers which have largest chopping current of the order of 100-300A. Therefore, this study illustrates the significance of absorber failure and calls for rapid reaction of backup protection in such case.

Once the DCCB in the open state, an unwanted closing operation has no influence in the system-level due to other open switches. i.e. MB. LCS, UFD.

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RCB is a typical mechanical breaker and some comprehensive surveys have been conducted on failure assessment of these critical components. CIGRE has provided a great insight into the failure statistics based on evaluation of more than 70 000 breakers around the world [49][50][51]. The ACCBs could be divided into three parts, i.e. high voltage, control and auxiliary, and operating mechanism. The high voltage part as the origin of about 25% of failures is comprised of arcing chamber, auxiliary interrupters and resistors, and insulation to earth. The second part comprised of trip/close circuits, auxiliary switches, contactors, and gas density monitor leads to about 30% of failures in ACCBs. It has been revealed that the main origin of failures in the mechanical breakers is the operating mechanism at about 45%, which provides the required energy for the operation of the CBs. The operating mechanism is comprised of compressors, pumps, energy storage, mechanical transmission, actuators and damping devices. The energy storage could be provided by spring, pneumatic and hydraulic viewpoints. Nowadays, the spring drive mechanisms are highly employed in AC CBs owing to their higher reliability.

2.8 AUXILIARY POWER SUPPLY FAILURE

The auxiliary power supply failure is a credible event which is of particular concern for the grid operator. A simulation is carried out to analyse system level consequences, using the test system from Figure 2.6. It is assumed that the auxiliary power failure causes the following consequences:

1) LCS and main breaker become open state since driving circuit losses energy supply.

2) Ultrafast disconnector and residual breaker remain in closed state considering close spring action.

When auxiliary power fails, the LCS opens and the LCS arrester is in parallel with the main energy absorber. The full load current now flows through the LCS arrester. An equilibrium is established according to the V-I arrester curve and depending on the load current. Figure 2.30 shows the simulation results. It is seen in Figure 2.30 a) that there is a voltage difference of a few kV between DC CB terminals, which is identical to LCS voltage in Figure 2.30 c). Figure 2.30 b) illustrates that all current is flowing through the LCS arrester. The energy dissipation in most cases (depending on the load current) will be too large for LCS arresters which elevates risk of physical damage or explosion. Therefore this failure should activate back-up protection.

The adverse effects of auxiliary power supply failure could be alleviated with the use of external energy storage devices such as batteries. The batteries could provide power to the gate drivers for a short period of time after the power supply failure to ensure that the breaker stays on until the power supply becomes functional again or, if the problem persist, to facilitate orderly shutdown of the system (by opening the breaker).

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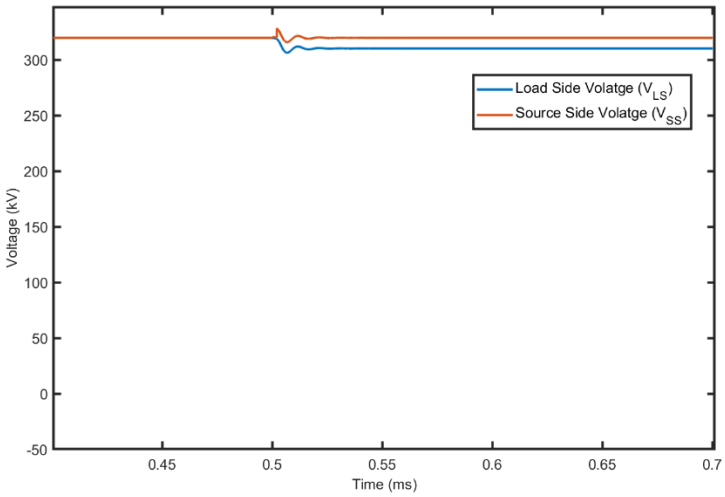
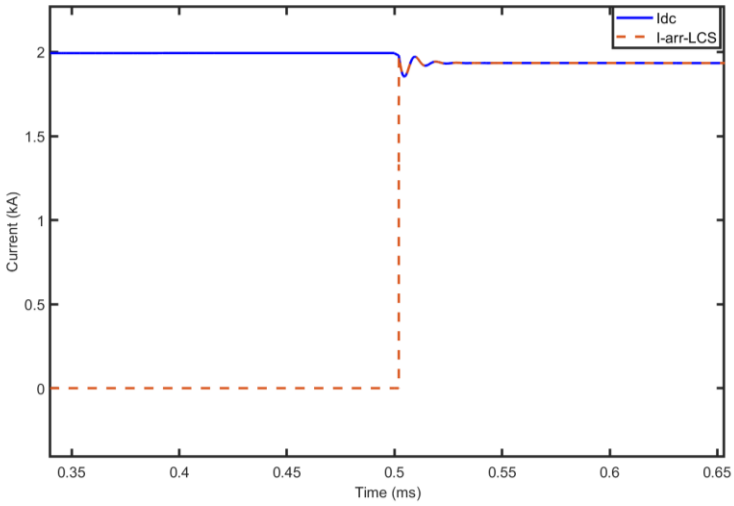
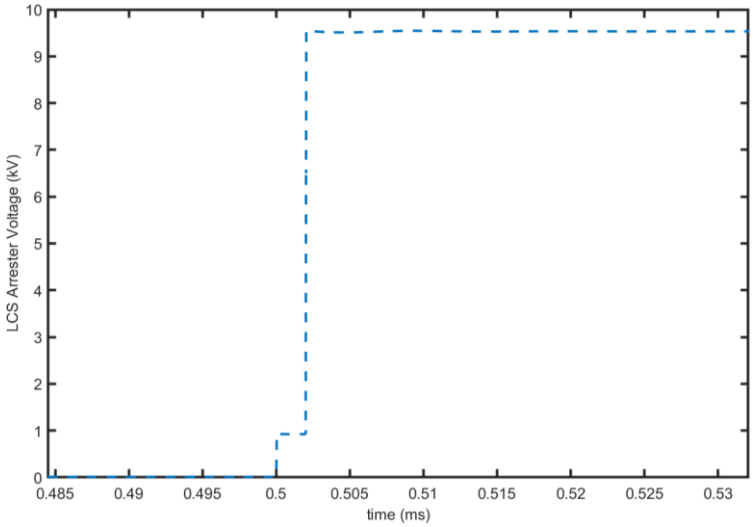


A) DC voltages at terminals of DCCB



b) DC line current and LCS arrester current



c) LCS arrester voltage

Figure 2.30. Simulation of auxiliary power supply failure.

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2.9 ANALYSIS OF INTERRUPTION OF LOAD CURRENT

The load current interruption has been simulated in [13] however only at system-level and on large time scale. In this section, the test system from Figure 2.6 is utilized.

Figure 2.31 shows the detailed graphs of interrupting 2 kA load current. The line-side of DCCB in this case has normal 320 kV voltage and this means that arrester is inserted in series with the line voltage. It is seen that source side of DCCB experiences around 2.5 pu voltage (almost 800 kV) for very brief period of time. Such high voltage would not normally be allowed and therefore there is need to incorporate an arrester to limit this voltage on the source side of DC CB.

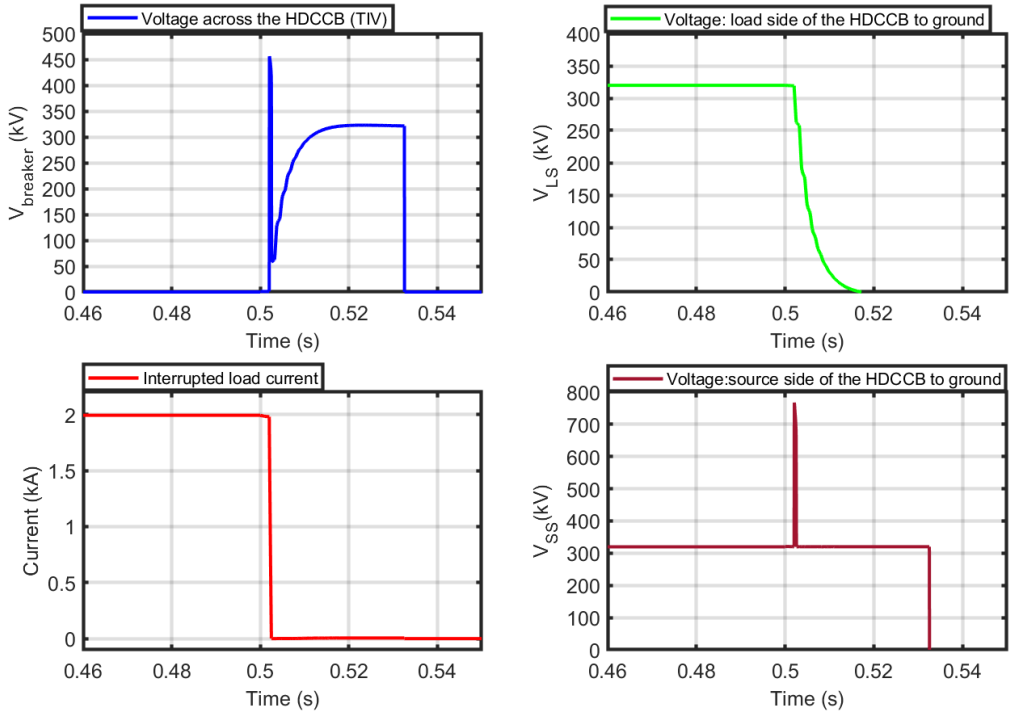

Figure 2.31. Detailed simulation of load current interruption.

2.10 ANALYSIS OF MODULE FAILURE

Hybrid DC CB will be built with modular structure for the main valve [1]. The module rating has previously been reported to be around 80 kV [6], and therefore a 320 kV breaker will have 4 modules in series. It is feasible that one complete module might fail.

Figure 2.32 shows the simulation of fault current interruption assuming one failed module. In this case the fault current suppression takes a much longer time. Also importantly, the residual current has a significantly larger value of around 300A. Residual breaker may not be able to interrupt such large dc currents and this could lead to

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thermal overload of the absorbers on healthy modules. Therefore it would be essential that such failure is identified in a timely manner and that backup protection is activated.

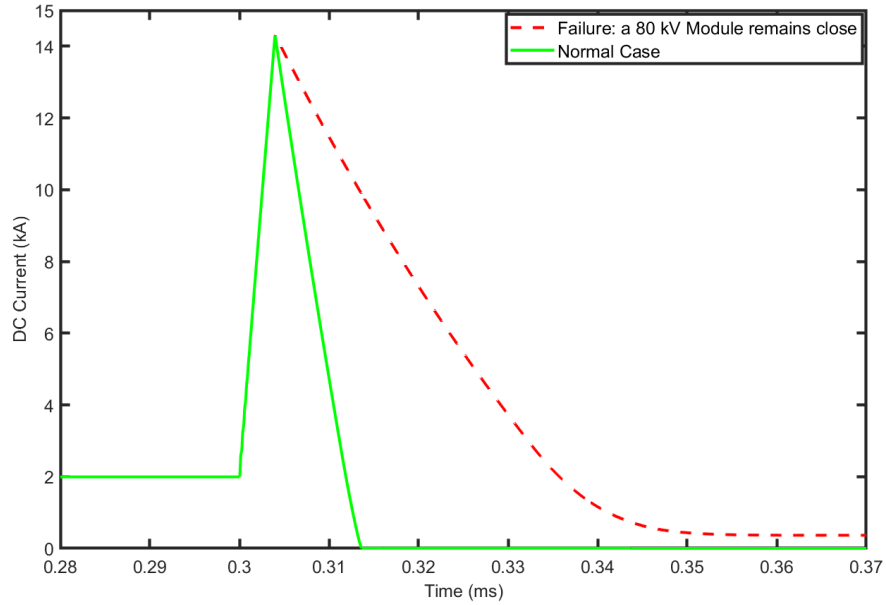

Figure 2.32. Simulation of fault current interruption assuming one failed module.

2.11 CONCLUSION

This chapter analysed the failure modes of the hybrid DCCB components in detail. The modular structure of the MB and, to a lesser extent LCS, ensures that these components are robust and resistant to single-unit failure. Self- and driver-level protection protects these devices against high current and thermal overload. The most likely cause of failure of these devices would be axuiliary power system failure, but this can be prevented with the use of an alternative power supply. The FO and FWO UFD failure modes will result in arcing. The analytical arc models for air and SF6 are developed and demonstrated on a hardware prototype (for air) and in PSCAD (for SF6). The experimental results show good agreement between the measured and calculated arc voltages while the simulation model correctly enters and exits the arcing mode. The reliability analysis of surge arrester banks revealed their vulnerability to single-component failures. Because of highly nonlinear I-V characteristics of surge arresters, even a small difference in applied voltages results in a large difference in drawn current. Since surge arresters always fail in a short circuit, current in the column with the failed arrester unit greatly increases and leads to overloading of all the arresters in that column. This in turn facilitates the cascaded failure of arrester units and results in the failure of the whole breaker module. A meshed energy absorber topology is proposed as a solution to these issues and is shown to greatly enhance their reliability.

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The findings of this chapter are summarized in Table 2.7. For each breaker component, an open- and closed-circuit failure is assessed for three states of the hybrid DCCB: open, closed and opening. The system-level impact on the DCCB, as well as the main components, is given for every combination of the states.

Table 2.7 Overview of hybrid DCCB failure modes

COMPONENT	FAILURE TYPE	DCCB STATE	IMPACT ON DCCB
Load commutation switch	Open circuit*	Open	No impact.
		Closed	Current commutates into the MB, increased conduction losses.
		Opening	No impact.
	Closed circuit	Open	No impact.
		Closed	No impact.
		Opening	Failed interruption.
Ultrafast disconnector	Open circuit	Open	No impact.
		Closed	Arcing in the UFD, increased on-state voltage drop.
		Opening	Arcing in the UFD, failed interruption.
	Closed circuit	Open	No impact.
		Closed	No impact.
		Opening	Failed interruption, possible damage to the LCS.
Main breaker	Open circuit*	Open	No impact.
		Closed	No impact.
		Opening	Damage to LCS if it occurs before the UFD fully opens.
	Closed circuit	Open	No impact.
		Closed	No impact.
		Opening	Failed interruption, possible damage to the LCS.
Energy absorber	Open circuit	Open	Failure of energy absorbers in an open circuit is not possible under a single DCCB opening. Ruptured arresters arc.
		Closed	
		Opening	
	Closed circuit	Open	No impact.
		Closed	No impact.
		Opening	Failed interruption, DCCB becomes a permanent short circuit.
Residual current breaker	Open circuit	Open	No impact.
		Closed	Arcing at high current, current interruption at low current.
		Opening	Temporary arcing but successful interruption.
	Closed circuit	Open	Leakage current flows through the EA, possible EA overload.
		Closed	No impact.
		Opening	Leakage current flows through the EA, possible EA overload.

* Possible only due to auxiliary power supply failure. Independent power supplies are assumed for the LCS and the MB.

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3 FAILURE MODE ANALYSIS OF MECHANICAL DC CB

3.1 INTRODUCTION

The current injection DC CB has been analysed and a model was developed in [13]. The laboratory scale 500 A prototype has been presented in [13] and it is used for the study in this report. The hardware demonstrator in [13] however employs 3 air interrupters while full-scale breakers employ vacuum interrupters. It is known that air interrupters would not be able to adequately represent behaviour of a full scale unit in critical studies like interrupter failure mode because of substantially different arcing and interruption characteristics. Therefore some responses in this chapter may not be representative of full-power DCCBs. The majority of conclusions however, like system level failures or injection timing would also be valid for full scale units. The study in this chapter will be also supplemented with digital simulation using the PSCAD DC CB model developed in [13].

Figure 3.1 shows the structure of a mechanical DC CB, which includes multiple VI (vacuum interrupters) in the main branch, injection circuit and energy absorber. The charging resistor is assumed a part of the commutation branch (current injection branch).

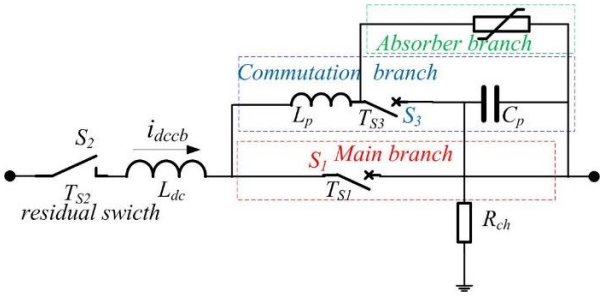

Figure 3.1. The structure of a DCCB based on the mechanical CBs, [17]

3.2 FAULT TREE DIAGRAM

Similar to the fault tree diagrams of the hybrid DCCB from [11], and using same assumptions the fault tree diagrams for the current injection DC CB are developed and shown in Figure 3.2. It is noted that all 3 switches are considered as single units in these diagrams. In HV implementation these switches may consist of series connected modules as shown in Figure 3.1, and failure diagrams may look differently if each module is separately analysed.

In the closed state (Fail Open) it is necessary that either the RCB or the VI and injection circuits simultaneously fail in order for the breaker to transition to open state. The failure of the energy absorbed has no impact, as shown in Figure 3.2 (a). In the open state, according to Figure 3.2 (b), it is required that at least two units fail

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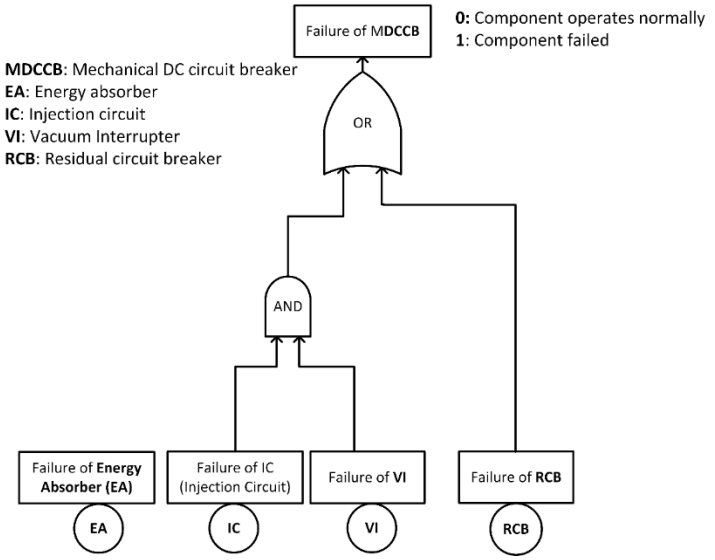
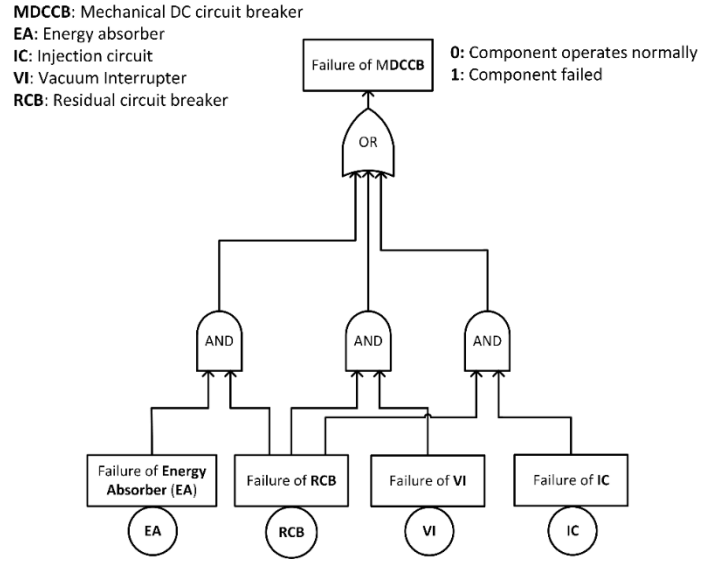
(a) Fail open



(b) Fail close



(c) Failure while opening

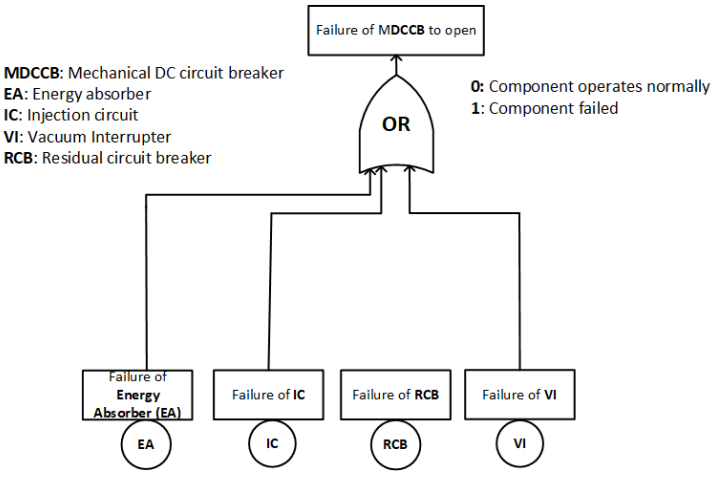


Figure 3.2. Failure Tree Diagram for current injection DC CB.

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simultaneously in order to transition the breaker into the closed state. During the opening process, all the components are critical and a failure of any component causes a system level failure, as shown in Figure 3.2 (c). The failure of RCB is not critical since it would take long time (longer than time considered for primary and back up protection) to cause thermal destruction of energy absorber, as discussed in [11]. RCB failure is further analysed in Section 3.6.

3.3 FAILURE OF THE MAIN BREAKER

As show in Figure 3.1, the load current passes through the normal current branch (which includes multiple main breaker units) during both normal and fault conditions. Thomson coil driven vacuum interrupters (VI) are usually employed as the main breaker owing to the fast operation speed and recovery time as well as the high dielectric strength within compact size and an excellent quenching capability at higher frequencies. Figure 3.3 presents a schematic of a VI (AC CB) used in Mechanical DC Circuit Breakers. As it can be seen, it is comprised of an interrupter and drive mechanism. In order to reach high speed operation, the operating drive mechanism is similar to that employed for UFDs including Thomson coil and bi-stable spring along with a mechanical damper. Consequently, the malfunctions of the drive mechanism would be similar for the two devices. The consequence of drive mechanism failure would be that switch remains in the closed state. Partial opening is unlikely because of the bi-stable mechanism.

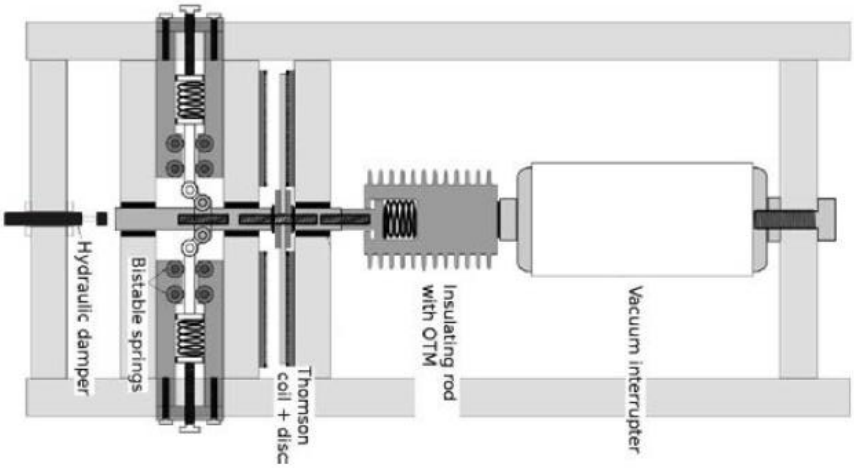

Figure 3.3. The structure of a vacuum interrupter [55]

Since the main interrupter is very similar to the conventional AC CBs, the vast experience with the AC CBs in service will be reviewed firstly. Generally, the failure in AC CBs are dependent on the operating mechanism, voltage level, indoor/outdoor location, function, age and so forth [49]-[51]. The failures are divided into major and minor failures. Major failures lead to the termination of one or more of the breaker's fundamental functions which results in an immediate action in the power system operating conditions, e.g. the backup protective equipment needs to operate to remove the fault, or mandatory removal from service for a non-scheduled maintenance. The

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other failures have been categorized as the minor failures such as small gas leakage due to corrosion or other causes. The lack of fundamental functions of AC Circuit Breakers are as follows [50]:

• does not close or open on command;
• closes or opens without command;
• does not make or break the current;
• fails to carry the current;
• breakdown to earth or between poles;
• breakdown across open pole (internal or external);
• locked in open or closed position.

In order to evaluate the origin of the failures in CBs, it has been divided into three main parts as follows:

- High voltage parts including arcing chamber, auxiliary interrupters, and insulation to earth.
- Control and auxiliary including trip/close coil, auxiliary switch, contactors, etc.
- Operating mechanism comprising of spring, compressor, pumps, actuators, mechanical transmission, damping device, etc.

Three world-wide comprehensive surveys have been conducted by CIGRE between 1970 and 2014 [50]-[52]. It has been reported that about 45%, 30% and 25% of failures originate from the operating mechanism, high voltage, secondary and auxiliary circuits of CBs, respectively. In addition, it is revealed that the technology of the operating mechanism is changing toward spring mechanisms: from a portion of 40% in the early days to 60% these days owing to the lower failure rate in comparison with the other mechanisms. The main breaker in Mechanical DC CB is not expected to suffer failure rates associated with hydraulic or pneumatic mechanisms, and the reliability data for drives using Thomson coils is not available. The above data may have importance for the design of residual breaker which uses conventional AC CB technologies. While wear, aging, and contact erosion have been reported as the most important reasons of major failure (about 50%), design faults, manufacturing faults, and incorrect maintenance together are reported as causes for 15% of the major failure [50]-[52].

3.3.1 Relay failure and self-protection

The self-protection of current injection DC CB is briefly discussed in [14]. The strategy is to keep the breaker closed in the case that the protection system fails to send a trip signal, under high current conditions.

3.3.2 Voltage level impact in a prototype Mechanical DCCB

A hardware small-scale test set-up of a mechanical DC CB implemented in UoA HVDC lab is described in [13] and is also shown in Figure 3.4. The normal current branch consists of the switches S1, S2, and inductor Ldc. S1 refers to the three interrupters connected in series; R_g and C_g stand for the snubber circuit; the injection circuit includes an inductor (L), switch S3a, and a capacitor (C) pre-charged through permanent charging resistor R_{ch}. Once the Mechanical DC CB is open, this capacitor could be charged to the system voltage level. The test parameters are presented in Table 3.1. The structure of the high-voltage Mechanical DC CB is very similar (including the charging circuit) as reported in [4] and [10].

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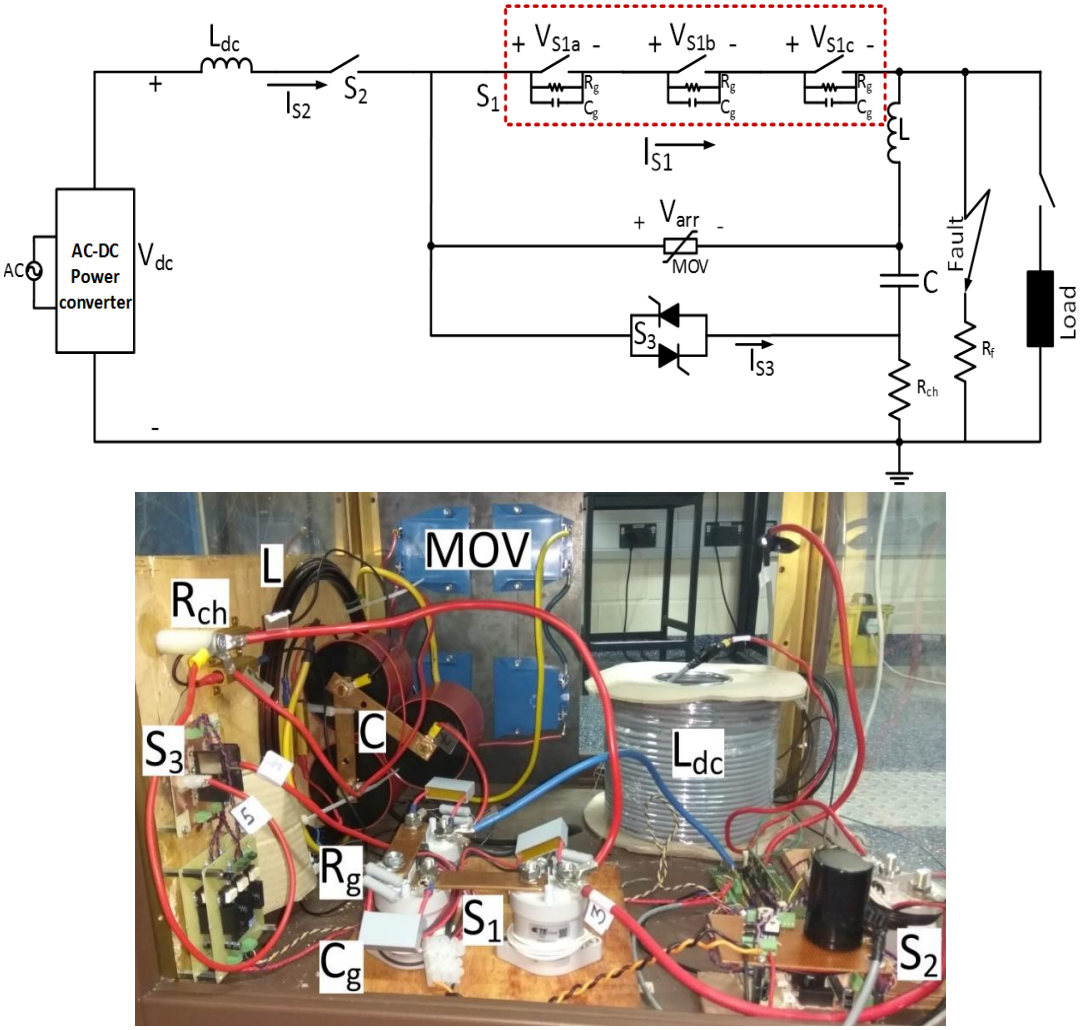

Figure 3.4. 500 A Mechanical DC CB test set-up

Table 3.1 Test set-up parampeter for Mechanical DCCB

parameter	Values
C	60 uF
L	46 uH
R_{ch}	50 kΩ
R_g	7.5 kΩ
C_g	100 nF
V_{dc}	700 V

The voltage level has direct impact on the number of series connected interrupters. In the initial design, 2 air-interrupters (rated for 900V) are connected in series. The details on the interrupters are provided in [13]. The test DC CB enables successful interruption of test current of around 300 A at a DC voltage around 500 V as shown in Figure 3.5. It is seen that S1a and S1b share the voltage stress (not necessarily equally) while S2 operates later (not in the shown timescale). However, for higher voltages and currents (Vdc = 650 V, Idc = 380 A) the interruption is difficult and uncertain as shown Figure 3.6. Although this figure shows successful interruption, there are multiple

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zero crossings and restrikes. Interruption was not successful for any further increase in current. This has led to the change in the design and 3 interrupters are subsequently connected in series.

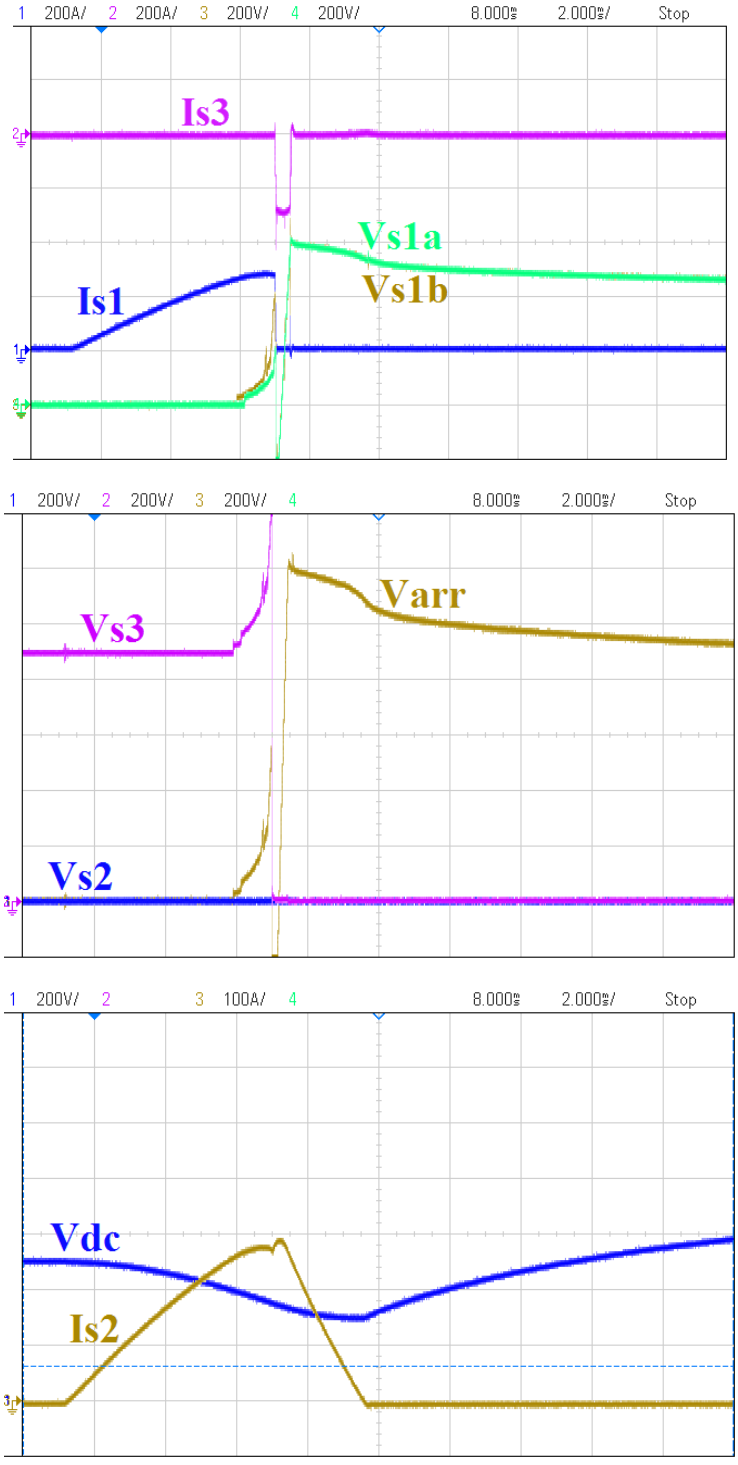

Figure 3.5. Hardware test results with 2 interrupters in series, Vdc=500V, S3 trigerred at 5ms.

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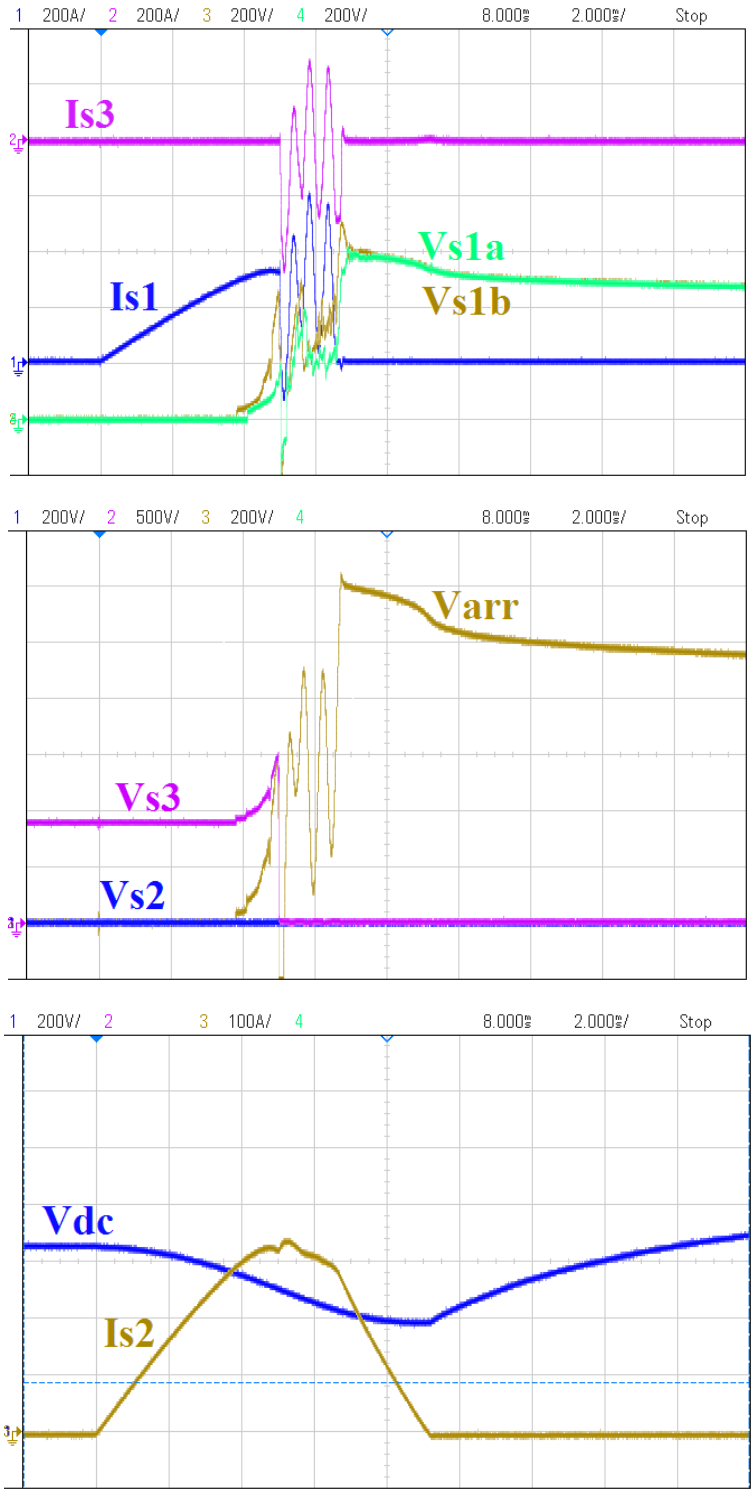

Figure 3.6. Hardware test results with 2 interrupters in series, Vdc=650V, S3 trigerred at 5ms.

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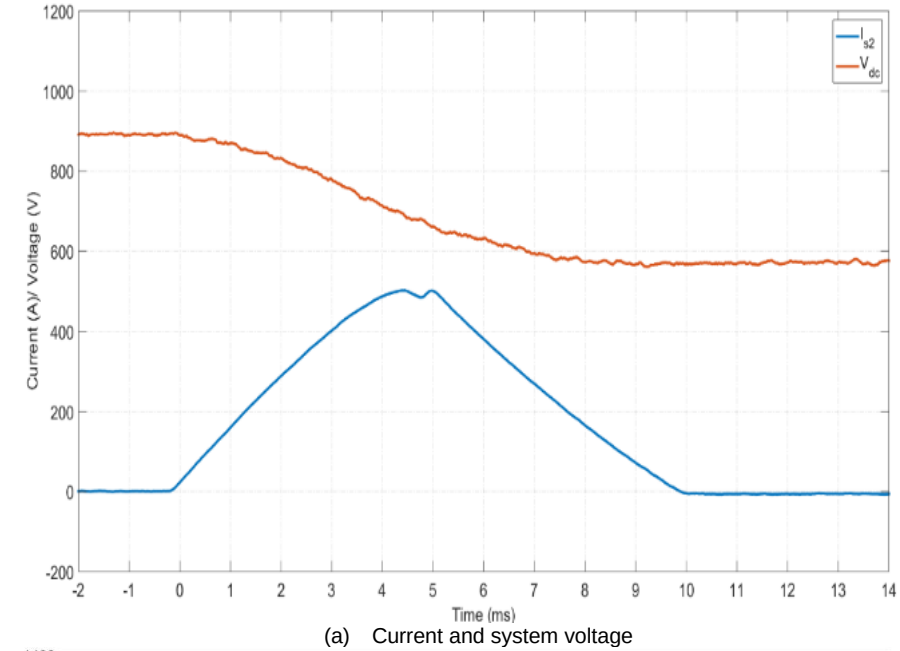
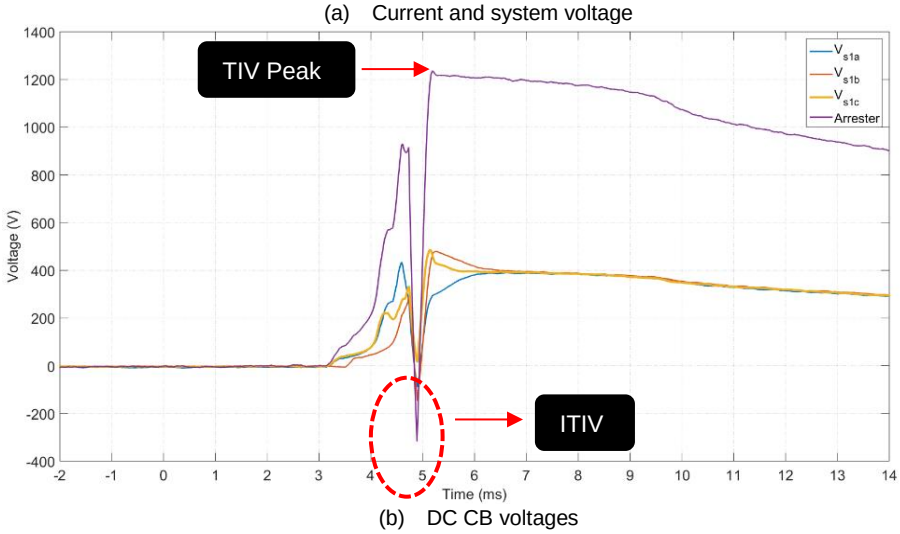
3.3.3 Failure caused by degraded contacts

Figure 3.7 presents the results of a rated positive current interruption case with 3 fully functional interrupters in series. As it can be seen, once the interrupters operate, arcing happens, and the voltage of the arc is increasing. In this mechanical DC CB the arc voltage is quite high and rises close to the system voltage because of the air-medium. In the high-voltage unit, which use vacuum as the medium, the arc voltage will be much lower.



(a) Current and system voltage



(b) DC CB voltages

Figure 3.7. Hardware test for DCCB stress in current interruption,

While the switch S3 is closed, a high frequency current is injected (I_{S3}) and provides a forced-current-zero for the Mechanical DC CB. In this moment, the interrupters interrupt the current. Subsequently, TIV is built-up (about 1.2 kV) as the arrester is inserted in the circuit which leads to a decrease in the current. As it can be seen in Figure 3.7 (b), due to remnant charge, the initial voltage on C changes polarity and leads to the ITIV (Initial Transient

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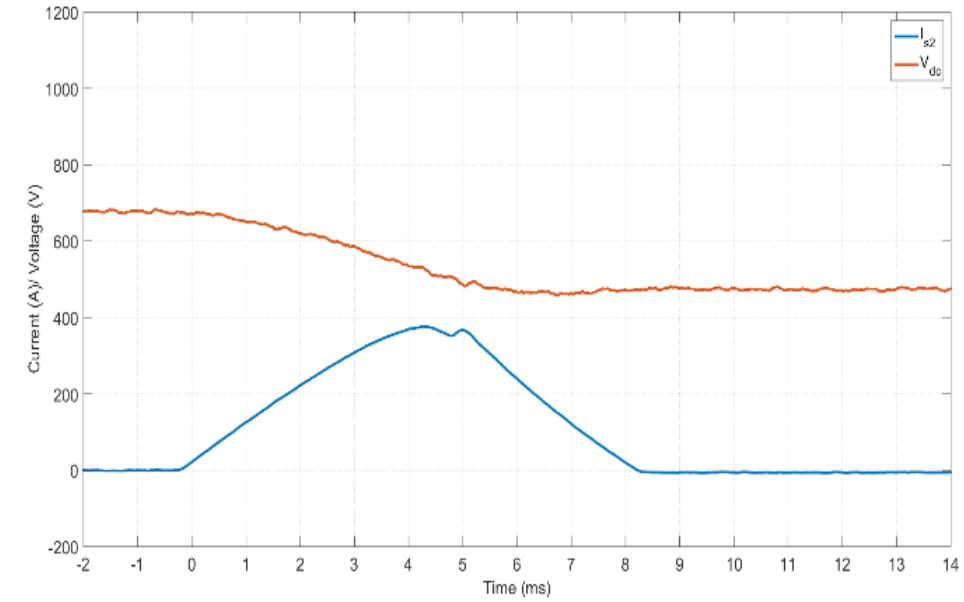
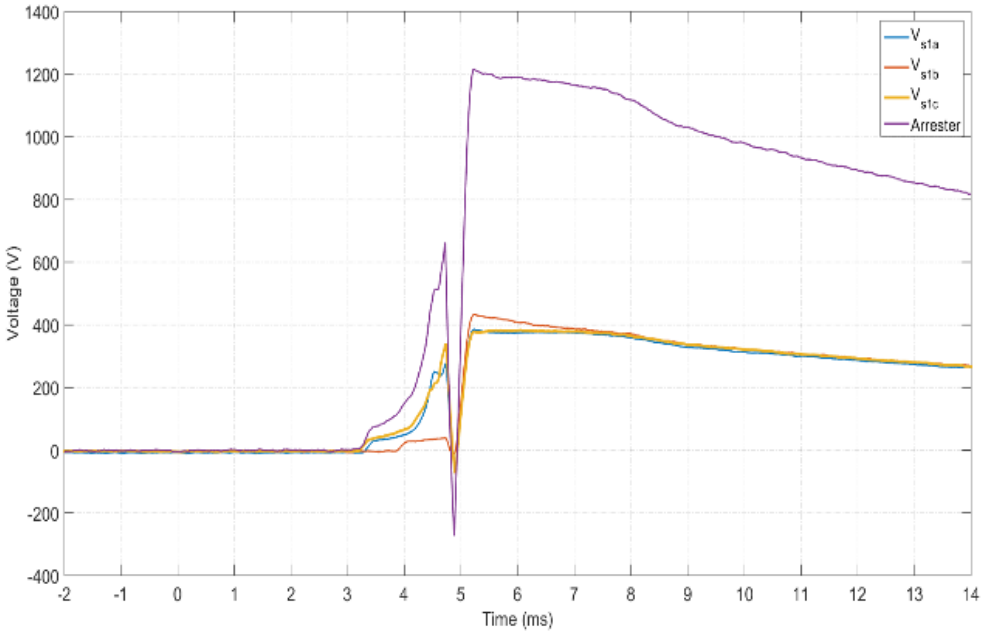
Interruption Voltage) while current increase in the LC resonant circuit. The circuit breaker is required to withstand TIV including this ITIV. In the test system, ITIV is about -400 V. It is seen that the transient voltage across the three VIs are quite uniformly distributed because of the use of snubbers.

Figure 3.8 indicates the voltage and current in case of degraded contacts. The contacts in switch b have been degraded due to numerous operations, leading to a notable change in the observed V_{s1b}. The arc voltage is lower and it rises later because of contact erosion. The erosion of contact surface has been confirmed by inspection.



a) Current and system voltage



b) DC CB voltages

Figure 3.8. Hardware test for current interruption with degraded contacts,

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3.3.4 PSCAD simulation of failure of the main breaker actuator.

A failure of the main breaker actuator is possible for various reasons, like auxiliary system failure. The result would be that S1 remains in the closed position. This case is simulated on the PSCAD model as shown in Figure 3.9. It is seen that the oscillating current is injected and multiple zero-crossings are created, however there is no interruption of the fault current.

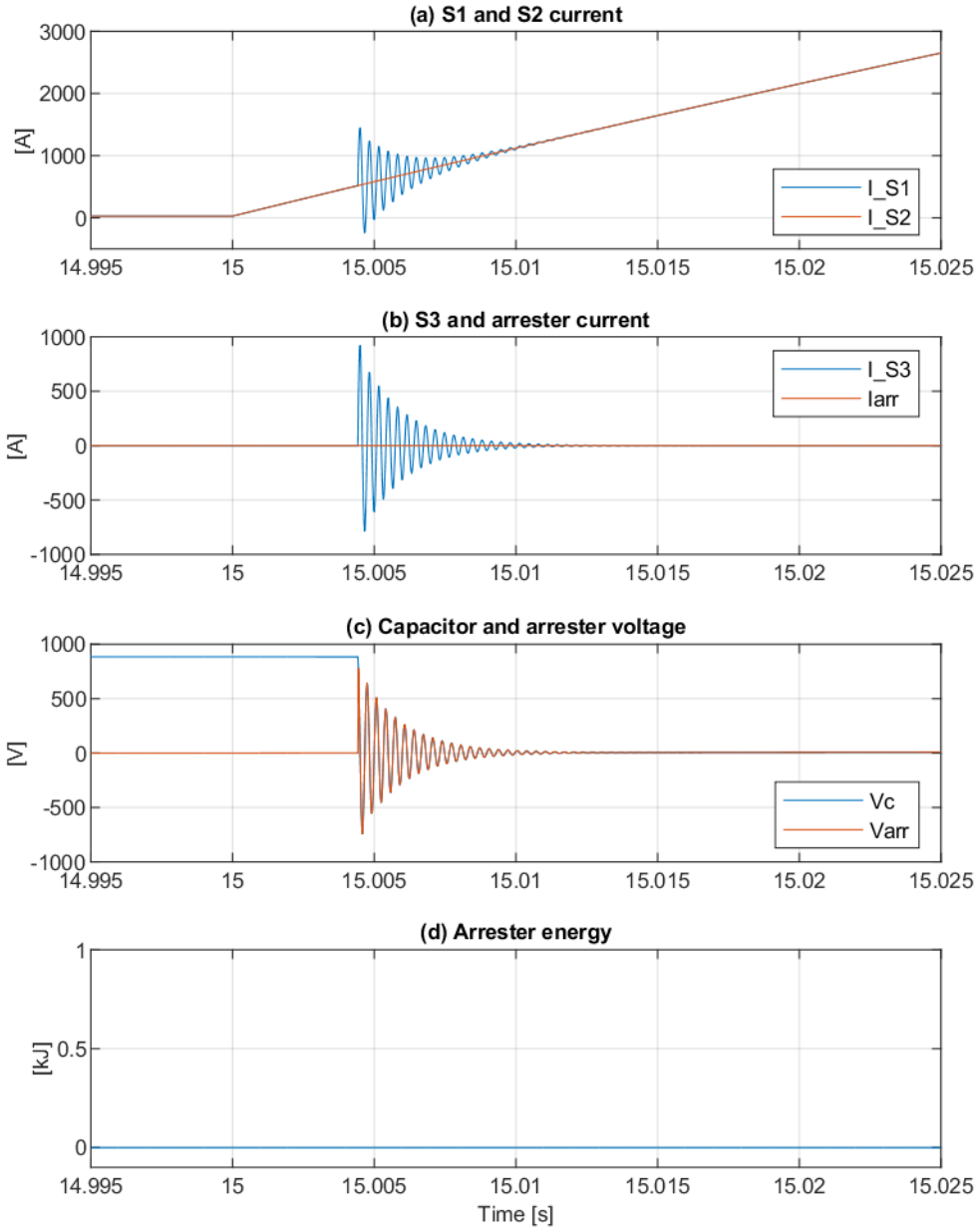

Figure 3.9. Simulation of Mechanical DCCB operation with failed actuator in the main breaker.

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3.4 FAILURE OF INJECTION CIRCUIT

3.4.1 Introduction

The injection circuit (IC) system is employed to impose an oscillatory current on the normal current branch current providing a forced current-zero for interrupting. It is implemented through a pre-charged capacitor and an inductor as shown in Figure 3.4. Once the breaker is in the close state, the operation of the IC has no impact on the system state. The IC is critical for the operation of mechanical DC CB. The VIs cannot interrupt DC fault current without superimposed oscillating current which should have correct timing, magnitude and frequency. Any fault in IC should initiate the backup protection operation.

The primary concern for failure comes from incorrect timing of IC activation. During the opening, the IC system might operate earlier, with some delay or even fail completely resulting from malfunction in the closing switch (S3 in Figure 3.4), operating mechanism, auxiliary power supply or control system.

It is known that VIs may not interrupt current in the first current zeros [54][55]. Once the current reaches close to zero, the vacuum arc changes from the constricted mode to the diffusion mode, as the current breaking is attempted. However, while the rate of rise of TIV is more than the dielectric strength, or owing to the thermal re-ignition, the arc may be re-established which is called reignition or restrike depending on the cause and time after current zero [54] [55].

3.4.2 Experimental evaluation of Injection Circuit failure

The experimental tests have been carried on the above test set up by varying the delay of injection circuit activation. The worst case scenario of negative peak current (-500 A) is chosen. S3 is triggered with delay between 2.5 ms and 6 ms in small steps, and results are shown in Figure 3.10 to Figure 3.14. Note that in these figures variables are shown as labelled in Figure 3.4. The source voltage is Vdc, while the arresters' voltage Varr may take much different values since it is separated from Vdc by the inductor Ldc. The current is common but the voltages across there series interrupters will differ.

It is seen in Figure 3.10 that 6 ms is a too long delay for a successful interruption at the first zero crossing. The arcing period is much longer than one injection current cycle and thermal phenomena lead to reignitions and multiple failed interruptions. This behaviour is unwanted as prolonged arcing leads to contact erosion. The oscillating current is seen to slightly increase which is attributed to the negative arc resistance. Such phenomenon may not be observed in high-voltage units although multiple zero-crossings may occur [54], [19]. Also, longer S3 delays result in higher peak current and voltage stresses, which may not be adequately represented in laboratory tests since a pre-charged capacitor is used to supply fault current. Figure 3.14 illustrates that a delay of 2.5 ms is too short since in this case the contacts have not separated to an adequate distance to enable withstand of the full TIV and repeated restrikes occur. On the basis of this analysis and further detailed examination a delay of 4.2 ms is selected as optimal for this breaker prototype. This illustrates the importance of precise current injection timing in this breaker topology and is applicable to HV breakers as well.

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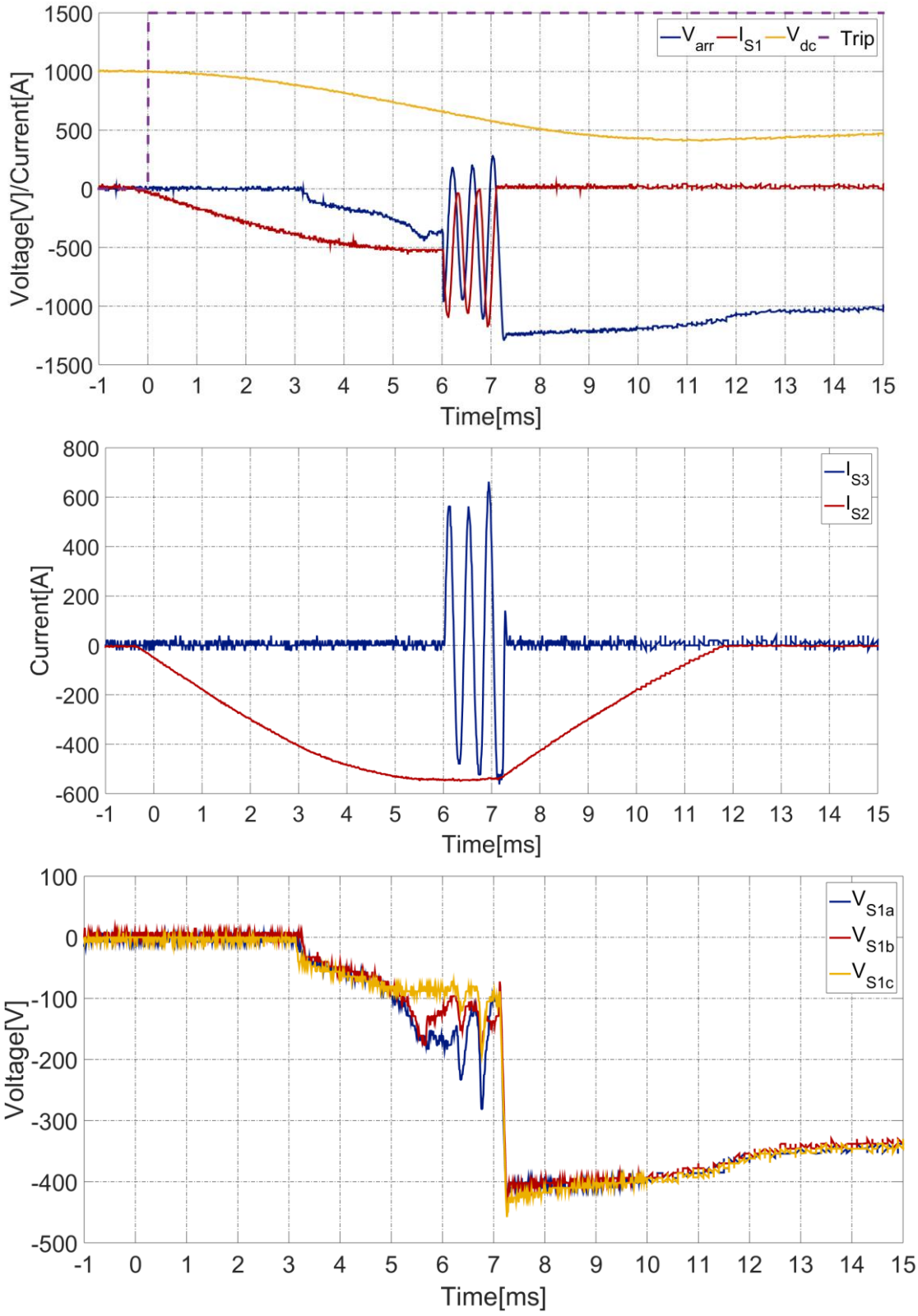

Figure 3.10. Hardware test for mechanical DC CB interruption of -500 A DC current. S3 triggered with 6 ms delay.

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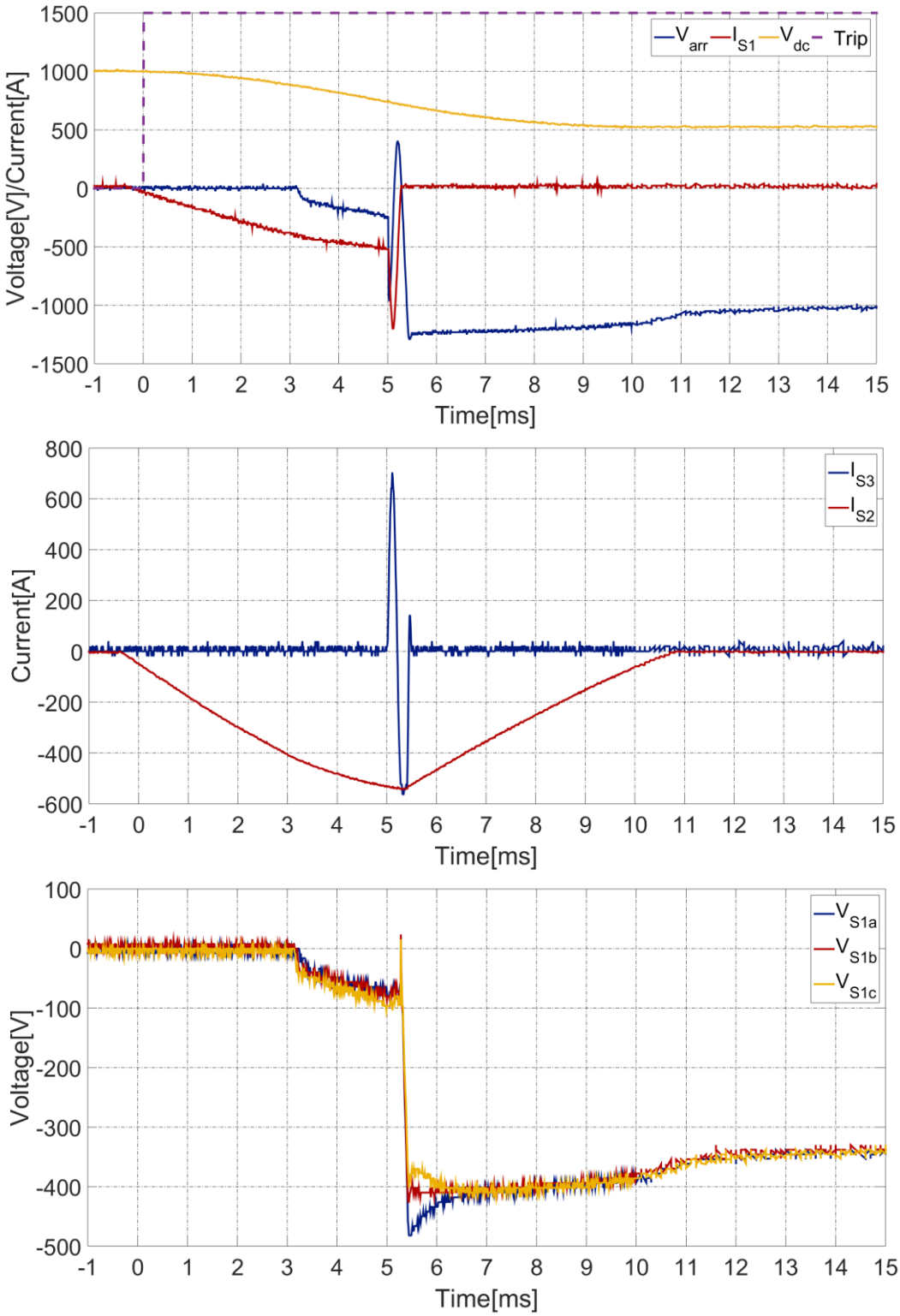

Figure 3.11. Hardware test for mechanical DC CB interruption of -500 A DC current. S3 triggered with 5 ms delay.

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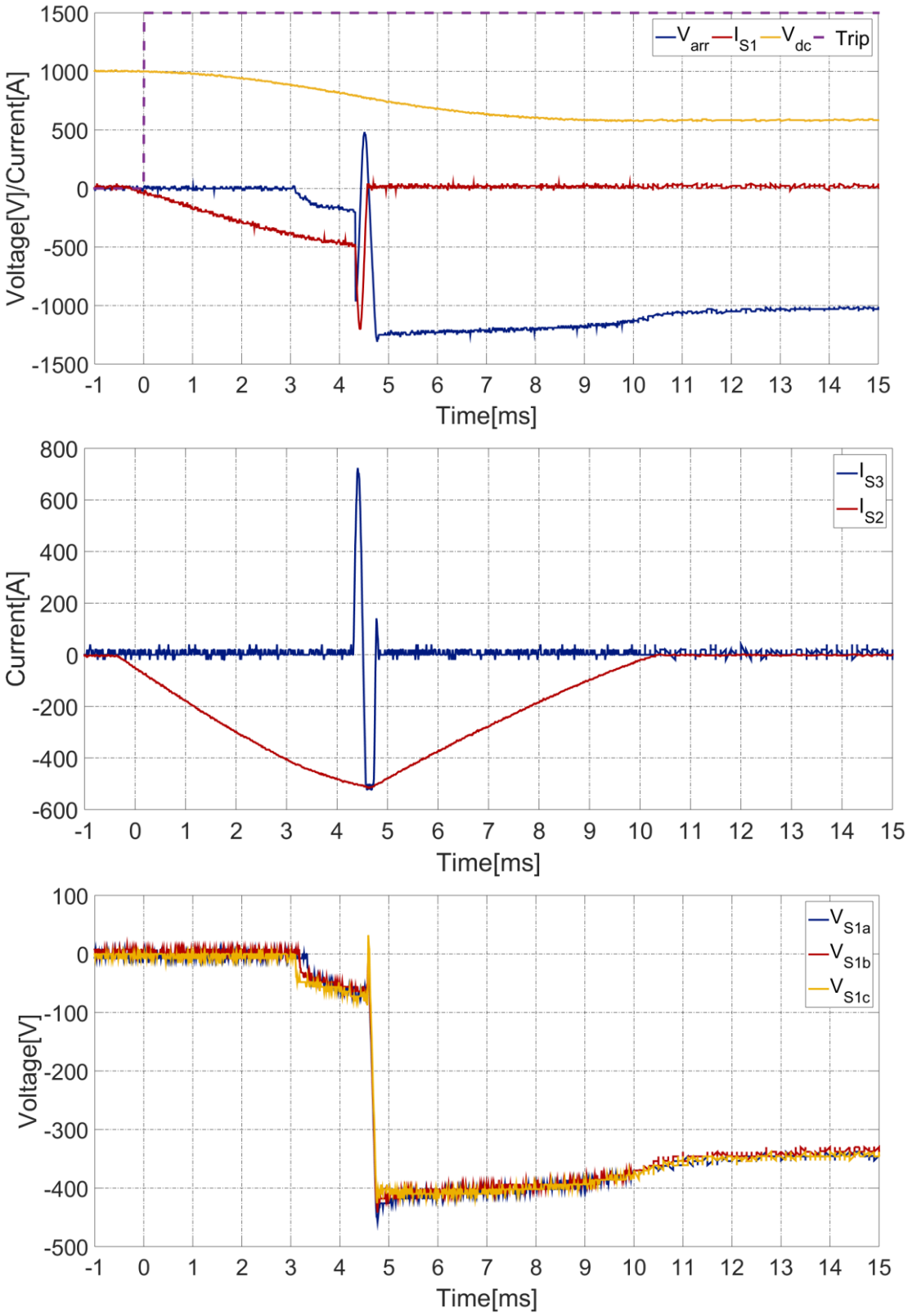

Figure 3.12. Hardware test for mechanical DC CB interruption of -500 A DC current. S3 triggered with 4 ms delay.

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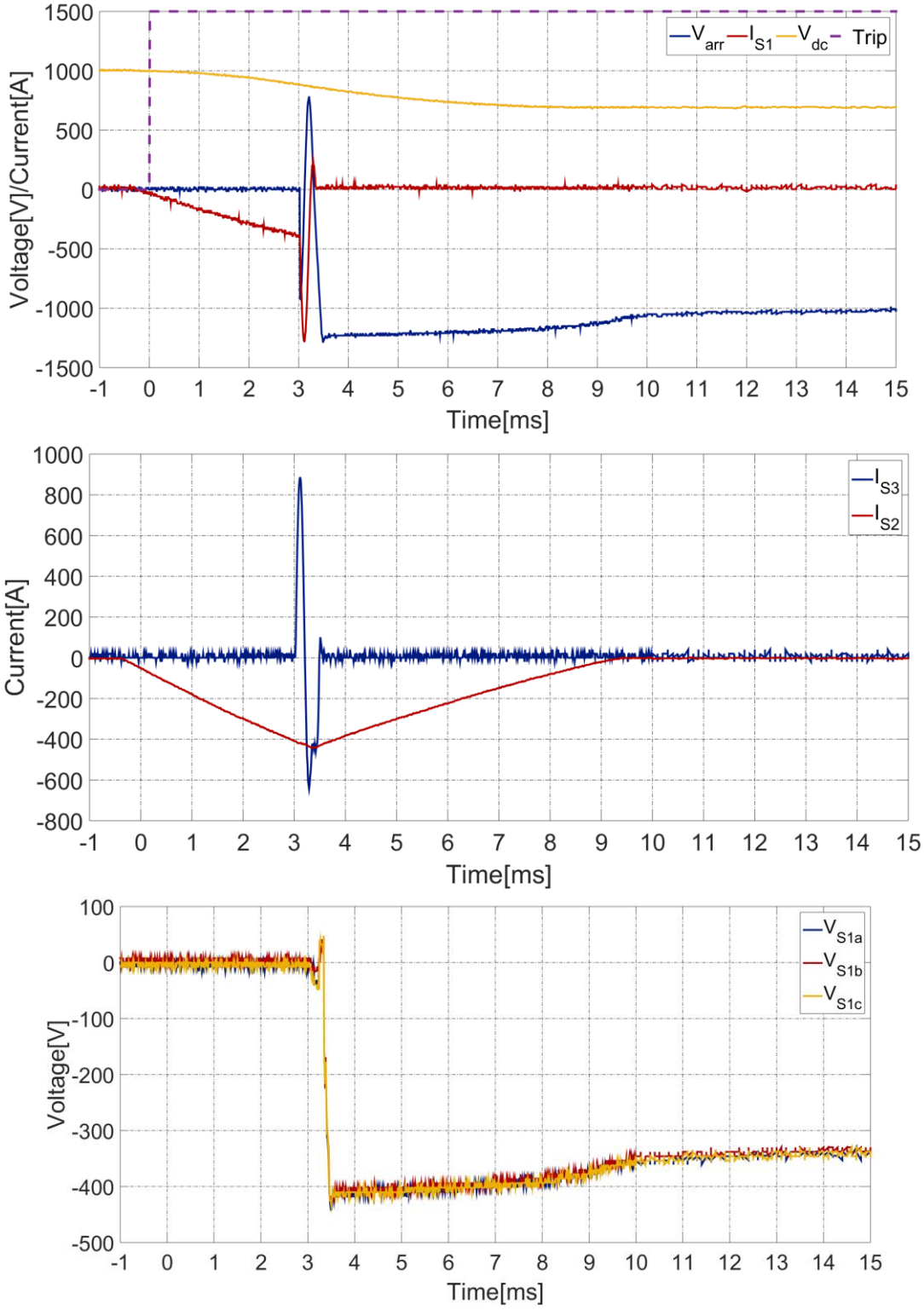

Figure 3.13. Hardware test for mechanical DC CB interruption of -500 A DC current. S3 triggered with 3ms delay.

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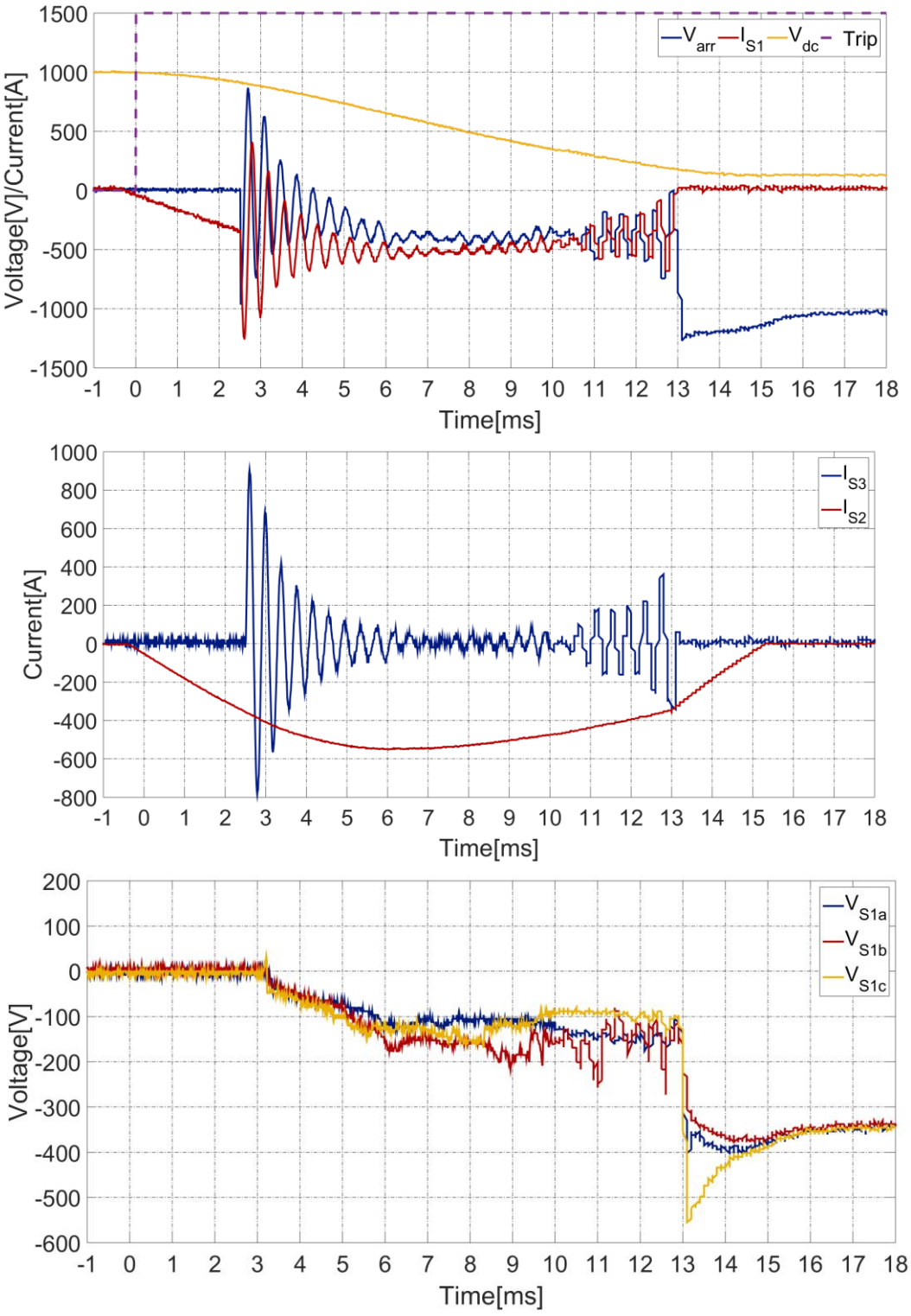

Figure 3.14. Hardware test for mechanical DC CB interruption of -500 A DC current. S3 triggered with 2.5ms delay.

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3.4.3 PSCAD simulation of Injection Circuit failure

The experimental results in the section above provide valuable results in failure analysis, but they cannot support analytical studies and deep understanding of the internal causes of failure. A PSCAD simulation of the mechanical breaker prototype has the advantage that all internal variables can be observed and there is no restriction on the number of case runs. In order to analyse the impact of failures of the IC and timing of series VI breakers, seven fault scenarios have been defined and presented in Table 3.2 For each case simulations are conducted in PSCAD to assess the impact on the performance of the Mechanical DCCB. S1a, S1b, S1c and S3 refer to the delay time between the trip signal and command to VIs and IC, respectively. “Base/Healthy” stands for the healthy operation. A 0.1 ms delay is added between the opening times of S1a, S1b and S1c to simulate delays that can be encountered in regular breaker operation. The cases F1-4 are concerned with the early and delayed timing of IC, while F5-7 simulate the delayed opening of VI in the main breaker.

Table 3.2 Various timing scenarios for IC and VIs

CASE NUMBER	Timing of trip command to VIS (ms)			Timing of IC (ms)
	S1a	S1b	S1c	S3
Base/Healthy	3.9	4	4.1	4.2
F1	3.9	4	4.1	**5**
F2	3.9	4	4.1	**7**
F3	3.9	4	4.1	**3.5**
F4	3.9	4	4.1	**2.5**
F5	**4.5**	4	4.1	4.2
F6	**5.5**	4	4.1	4.2
F7	**Same “F6” but considering the restrikes**			

Figure 3.15 indicates the results of simulations for failure F1 and F2, i.e. the delayed injection time of IC as well as the healthy case (Base). As it can be seen, the small delay in injection circuit timing (Case F1) would still facilitate current zero crossing and successful interruption. It is also seen in Figure 3.15 (e) that delays lead to an increase in the absorbed energy ($E_{F1} > E_B$). From the voltage stress point of view, as seen in Figure 3.15 (c) and (d)), a delay does not have a notable influence.

Case F2 illustrates that a substantial delay in IC operation (7 ms) would lead to failed current interruption. This is the same scenario as discussed under self-protection in Section 3.3.1. Mechanical DC CB needs to operate by a certain time after the fault event, or otherwise interruption will not be possible. Figure 3.15 (a), showing currents through S1 and S2, indicates that a long delay in triggering the current injection circuit (case F2) leads to failed interruption because the amplitude of oscillating current is lower than the DC current magnitude at all times. Therefore, the electrical status of the arcing VIs appears as a closed state.

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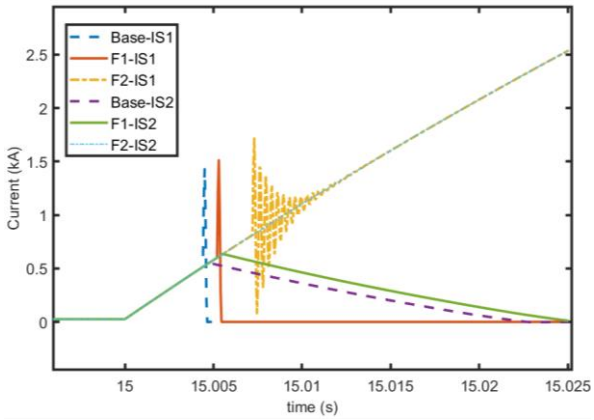
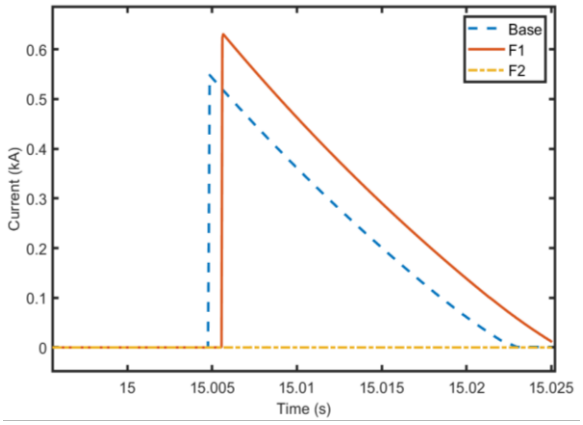
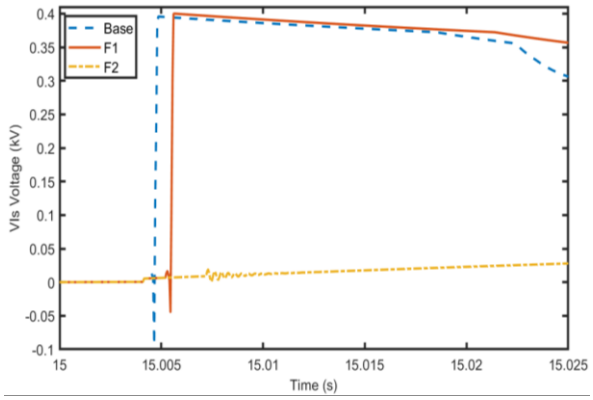


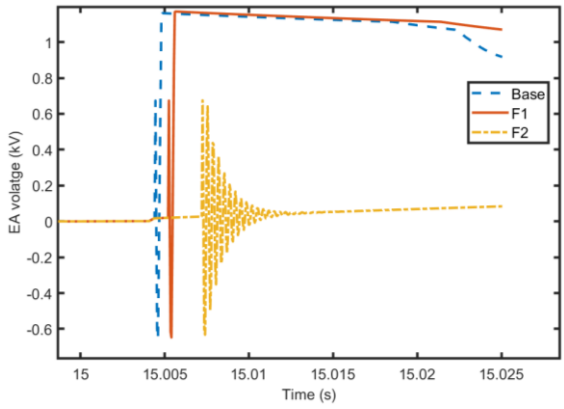
(a) IS1 and IS2



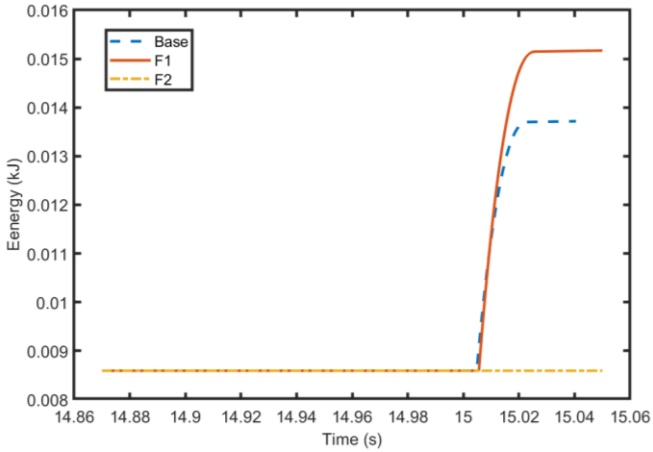
(b) EA current



(c) VIs voltages



(d) EA voltage



(e): Energy of EA

Figure 3.15. Simulation of impact of injection timing on Mechanical DC CB; F1 and F2 test cases from Table 3.2.

The cases F3 and F4 simulate the earlier operation of S3 as shown in Figure 3.16. Slightly earlier IC timing (F3 case) might lead to multiple zero crossings before the contacts have adequately separated to enable sufficient dielectric withstand of the full voltage. If injection is too early (case F4) the interruption may not succeed since the

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distance between contacts is not sufficient for the required TIV. These findings are in general agreement with experimental results from Section 3.4.2.

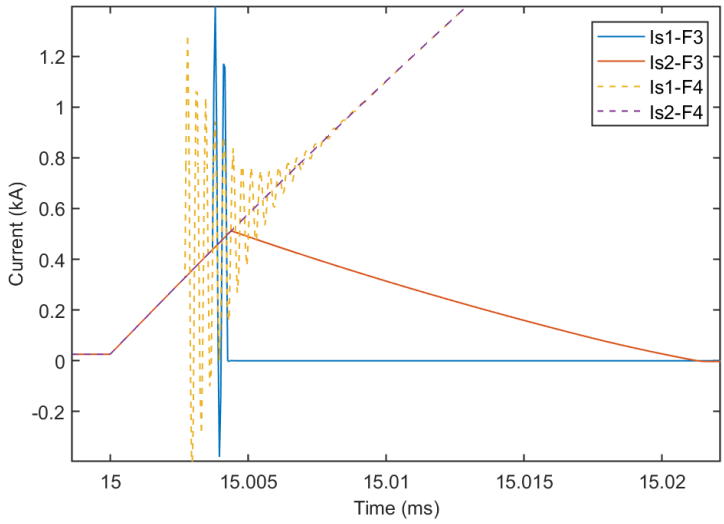

Figure 3.16. Simulation of impact of injection timing on Mechanical DC CB; F3 and F4 test cases from Table 3.2

In order to scrutinize the impact of timing of the three VIs on performance of the DC CB, two more scenarios, i.e. F5 and F6, have been defined where the VI "a" operates with short (F5) and long (F6) delay in comparison with the healthy case. No changes are observed in the current and EA waveforms owing to successful interruption in these cases. However, as shown in Figure 3.17, the voltage stress on the three VIs are significantly different in comparison with the normal case. The interrupters with earlier opening will have more stress (healthy breakers with no delay) ($V_{bc\text{-}F6}>V_{bc\text{-}F5}>V_{bc\text{-}normal}$). in case of F6, the worst delay time, the healthy VIs ("b" and "c") need to tolerate half of the arrester residual voltage (about 0.6 kV). In comparison to the healthy case (about 0.4 kV), this is a 50% increase in voltage stress, which is significant. Clearly timing accuracy will have significant impact on the design of mechanical DC CB.

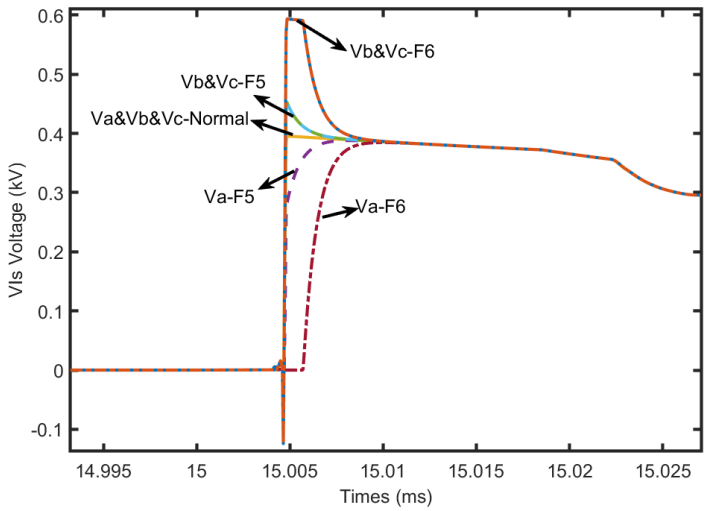

Figure 3.17. The distribution of the voltage across the VIs in healthy and faulty cases

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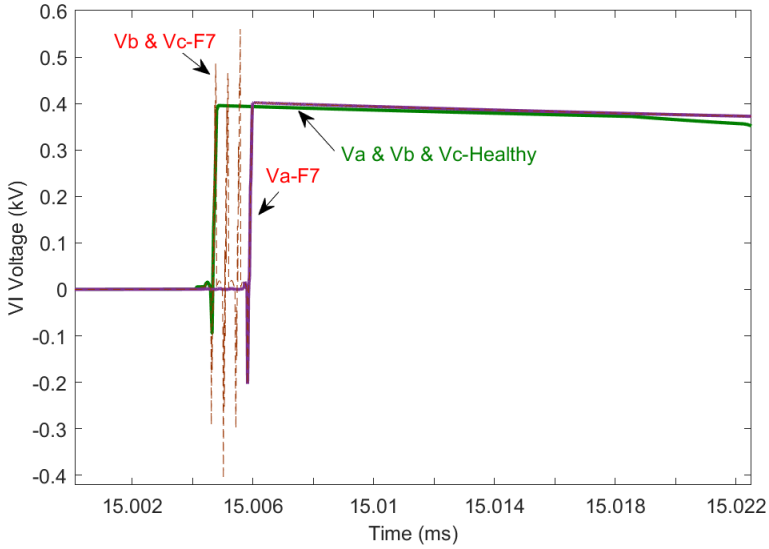
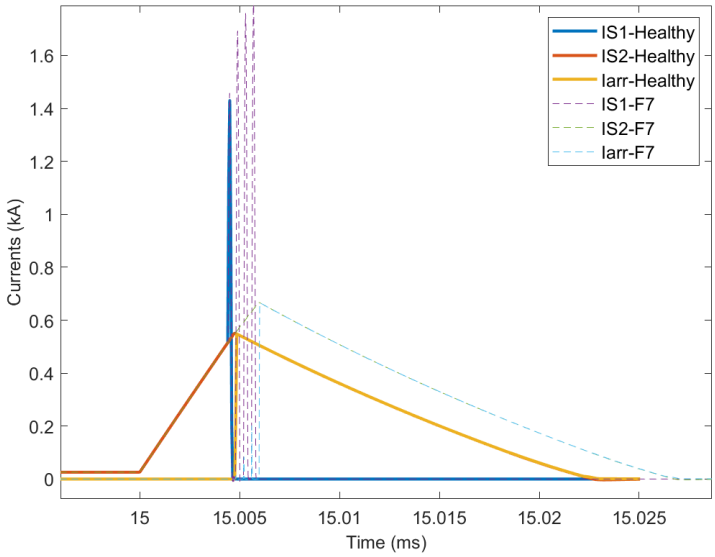
In order to evaluate the impact of a restrike, case F7 is introduced which is similar to case F6 but considering 0.55 kV as the maximum tolerable TIV peak by VIs. It is noted that this is a hypothetical value to investigate the resulting restrikes. The results of simulations are indicated in Figure 3.18. As it can be comprehended from Figure 3.18 (a), the breakers *b* and *c* could not tolerate the TIV in the faulty case and restrikes happen. These restrikes lead to multiple cycles of oscillating current of the IC until the last VI opens as shown in Figure 3.18 (b). In addition, this failure results in an increase of the interrupted current and the opening time as shown in Figure 3.18 (b). Furthermore, this case leads to an increase (about 15%) of the absorbed energy in EA as obtained in Figure 3.18 (c). This in turn could lead to an increase in the EA temperature and accelerated-aging.



(a): Voltage Across the VIs



(b): currents in Mechanical DCCB

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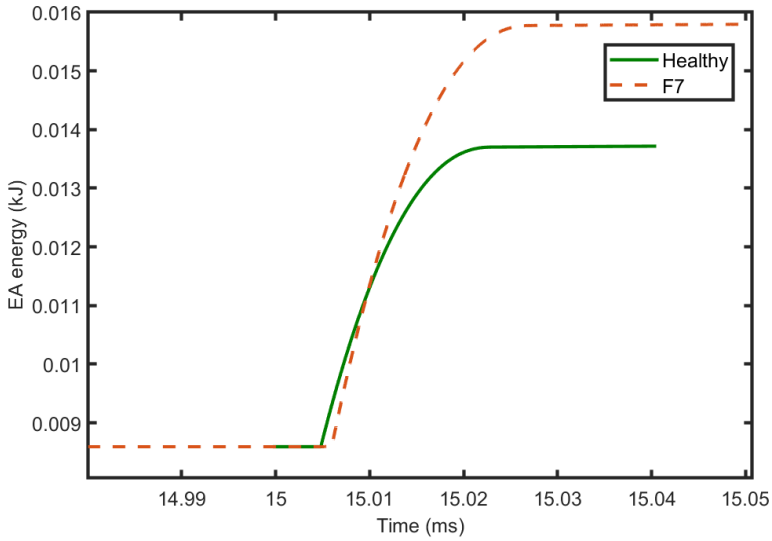

(c): Total energy of the EA branch

Figure 3.18. Simulation of Mechanical DCCB under fault condition F7.

A feasible failure of injection circuit is inadequate charge of capacitor C. In the existing designs C is normally charged directly from the line using a charging resistor as shown in Figure 3.4. As an example unenergized line or damaged charging resistor would prevent charging of C. Figure 3.19 shows the simulation results, assuming that capacitor is pre-charged to 30 V (instead of 900V). It is seen that some oscillating current is injected but the current magnitude is low and inadequate for creating zero crossing in the main interrupter. This failure would have system-level impact and therefore monitoring of capacitor C voltage could be implemented to enable timely activation of back-up protection in case of such failure.

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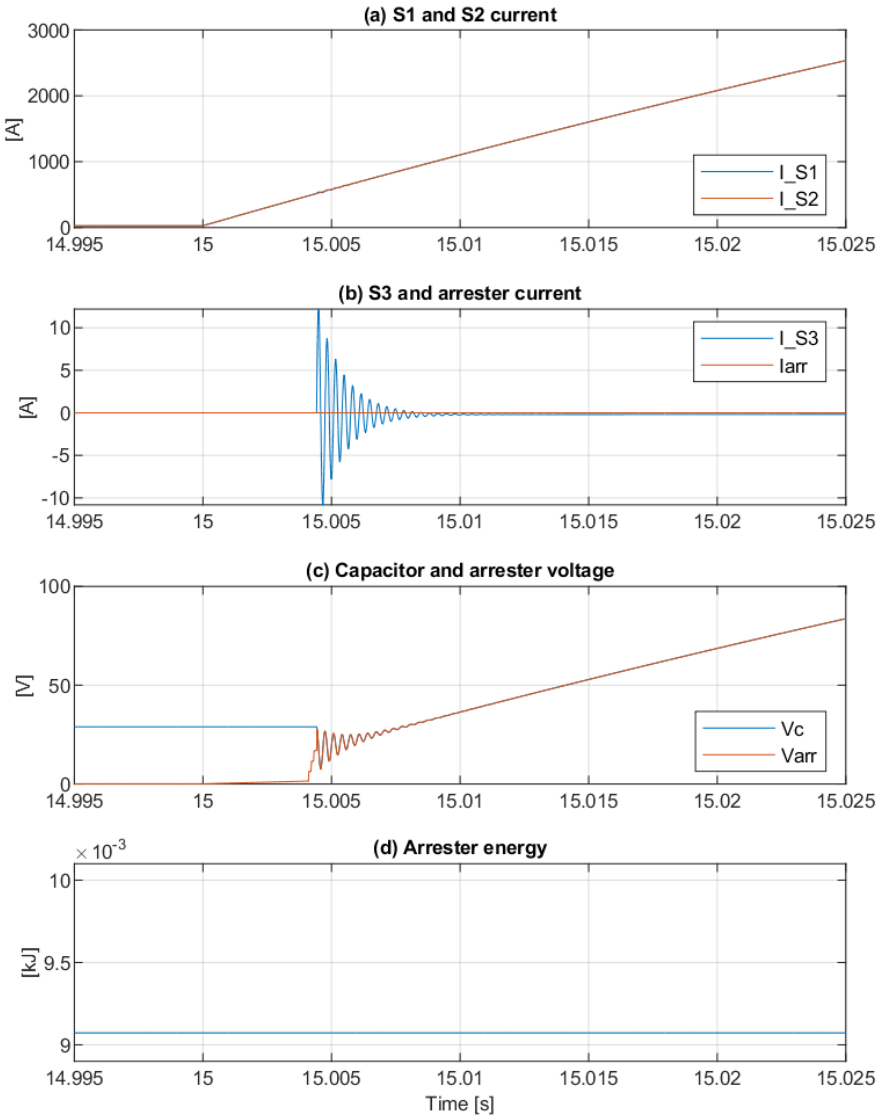

Figure 3.19. Simulation of Mechanical DCCB operation with low precharged voltage on C.

3.5 FAILURE OF ENERGY ABSORBER

The role and stress of EA are similar to those presented for a hybrid DC CB. Most of the conclusions presented in section 2.6 are applicable here. However, unlike the hybrid DC CB where each breaking module has its own energy absorber, the mechanical breaker from [17] is shown to incorporate a single, lumped energy absorber. Depending on the internal structure of the absorber, its reliability and robustness or mechanical DC CBs to single arrester unit failures may be different to those of a hybrid DC CB. If the non-meshed structure from Figure 2.10 is adopted for the arrester bank, a single-unit failure is likely to cause a catastrophic failure of the whole energy absorber, short circuitng the breaker. However, if a fully or partially meshed topology is adopted, the resilience to single-unit failures will be greatly improved and the energy absorber will become more robust and reliable. Partial meshing considers shorting some rows beween individual arrester units, but not all as in Figure 2.27. Using partial

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meshing, the arrester bank can be divided into an arbitrary number of sub-modules which perform identically to those in hybrid DC CBs. For example, if the arrester bank is divided into four submodules and one of the modules fails, the resulting system-level impact will be analogous to the one observed in Figure 2.32.

3.6 FAILURE OF RESIDUAL BREAKER

The RCB with mechanical and hybrid DCCB are similar and stresses are similar. Therefore the study provided in Section 2.7 is largely applicable here. However, mechanical DC CB has different commutation branch which includes a series capacitor and this capacitor may create oscillations with the DC cable. These oscillations are visible in the experimental tests on full-scale DC CB reported recently [56]. Figure 3.20 shows the simulation of fault current interruption with failed RCB, using the same PSCAD model of the 900V laboratory DCCB. It is seen that the interruption is successful, but there are persistent small-magnitude current oscillations. The magnitude of these oscillations will depend on the operating conditions.

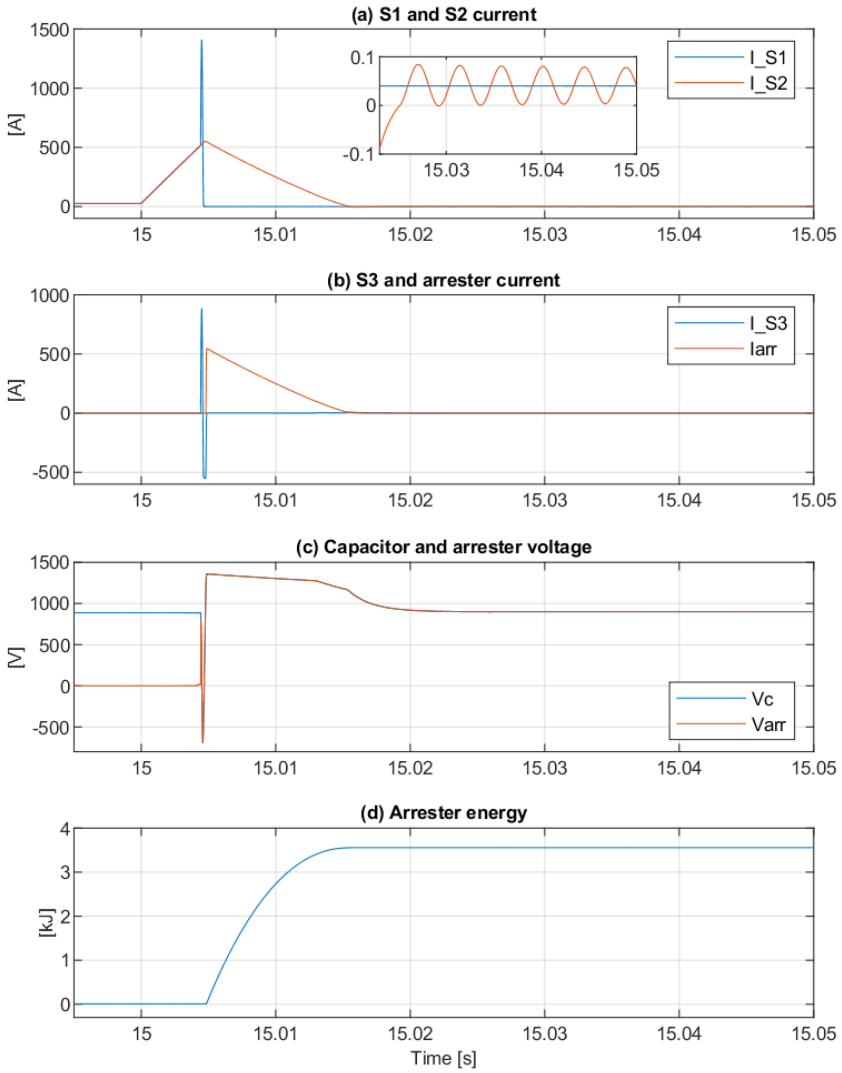

Figure 3.20. Simulation of Mechanical DCCB operation with a failed residual current breaker

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3.7 FAILURE OF AUXILIARY POWER SUPPLY

The auxiliary power supply is required for activation of: main breaker S1, closing switch S3 and residual breaker S2. Additionally, all the internal controls will require a power supply. Normally, a back-up battery will be provided to supply auxiliary power in case of loss of main supply. It is noted that capacitor charging is achieved directly from the line as discussed in Section 3.4.3 and therefore it is not a part of the auxiliary circuit.

In case of a total loss of auxiliary power (including battery loss) the following will occur: all three switches will remain in the same position because of the (bi-stable) spring action in the drive mechanism. A closed DCCB therefore remains closed. This is different behaviour from the hybrid DC CB discussed in Section 2.8 (which changes state).

In case that only one of the three switches loses power supply then the DC CB will respond as discussed in the previous sections (failure of main breaker in Section 0, injection switch in Section 3.4 and RCB in Section 3.6).

3.8 CONCLUSION

This chapter presented a detailed failure mode analysis of the mechanical DC CB. The fault tree diagrams link the state of the DC CB as whole with the states (healthy/failed) of individual components. The failure of the main breaker and the failure of the injection circuit are studied experimentally on detailed on a 1 kV breaker prototype. The experimental work is further substantiated by PSCAD simulations which are used to analyse additional test cases and offer an insight into all the state variables at any point in time. The erosion of VI contacts is shown to reduce the arc voltage and increase TIV across the switch which may lead to restrikes and arc reignition. In case of an VI actuator failure, the mechanical breaker remains a closed circuit and line current is not interrupted. The timing of injection circuit firing has a very significant impact on the performance of the breaker. Too early or too late triggering leads to failed current interruption and arc-reignition, although the current may be interrupted on subsequent zero crossings. Nevertheless, the prolonged arcing time has a negative impact on the VI which may suffer from contact erosion. In case of inadequate capacitor voltage, no zero crossing is generated in the interrupter and current interruption fails. The mechanisms behind energy absorber failure are identical to those for hybrid DC CBs. In case of an RCB failure, persistent current oscillations occur between the breaker's LC circuit and the remainder of the grid. These oscillations are generally small in magnitude, but do differ depending on the system parameters. In case of auxiliary power supply failure, the mechanical breaker does not change its state.

The findings of this chapter are summarized in Table 3.3. As with the hybrid DCCB, the open- and closed-circuit failures of each component are paired with the three states of the mechanical DCCB: open, closed and opening. All combinations are taken into account.

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Table 3.3 Overview of mechanical DCCB failure modes

COMPONENT	FAILURE TYPE	DCCB STATE	IMPACT ON DCCB
Main breaker	Open circuit	Open	No impact.
		Closed	Arcing in the VI, increased on-state voltage drop.
		Opening	Prolonged arcing but successful interruption.
	Closed circuit	Open	No impact.
		Closed	No impact.
		Opening	Failed interruption.
Injection circuit	Open circuit	Open	No impact.
		Closed	No impact.
		Opening	Failed interruption, no zero crossing is created in the VI.
	Closed circuit	Open	Capacitor partially discharges through the arrester, but no system-level impact.
		Closed	Increased VI current, but no system-level impact.
		Opening	Possible failed interruption if the capacitor discharges early.
Energy absorber	Open circuit	Open	Failure of energy absorbers in an open circuit is not possible under a single DCCB opening. Ruptured arresters arc.
		Closed	
		Opening	
	Closed circuit	Open	No impact.
		Closed	No impact.
		Opening	Failed interruption, DCCB becomes a permanent short circuit.
Residual current breaker	Open circuit	Open	No impact.
		Closed	Arcing at high current, current interruption at low current.
		Opening	Temporary arcing but successful interruption.
	Closed circuit	Open	Leakage current flows through the EA, possible EA overload.
		Closed	No impact.
		Opening	Leakage current flows through the EA, possible EA overload.

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4 CONCLUSION

This report presents the findings of the failure mode study on two DC Circuit Breaker topologies: hybrid breaker and mechanical breaker.

The failure of all major internal components in a hybrid DC CB has been studied. A model for an air-based disconnector in arcing (failure) mode is developed and shows good accuracy compared with the experimental results on laboratory 5 kV hardware. The model for a SF_6 320 kV disconnector in arcing mode is also developed and PSCAD simulation confirmed the expected responses for various modes and mode transitions. A comprehensive experimental study of the energy absorber failure has been conducted. The experimental results at 1 kV level confirmed that arresters are expected to fail in short circuit (or lower resistance state). Further analysis at the level of energy absorbers indicated that cascaded failure is feasible and likely. It was demonstrated that a single arrester failure (in a 2x2 matrix of arresters) leads to an overload of the other arresters in the same column and eventually the whole column fails. A proposal is made for interconnecting arresters between rows in order to better spread current and prevent cascaded failure in case of a single unit failure. The testing with an arrester across the load commutation at 1 kV level switch demonstrated that it would fail in short circuit and that such failure would not be electrically damaging for the LCS. The analysis of auxiliary power failure on a full-scale PSCAD model concluded that LCS arrester would take full load current and that DC CB would respond like a resistor with around 9-10 kV voltage drop. In case of one 80 kV module failure in a 320 kV breaker, the fault current would be interrupted in a much longer time and the residual current would be large, probably beyond the ability of residual breakers.

The failure of all major components of the mechanical DC CB has also been studied. The hardware testing at the 1 kV level demonstrated that timing of activation of the injection circuit has a significant impact on the success of DC current interruption. Too early current injection led to restrikes and failed interruption because contacts did not adequately separate at the instant of current injection. Too late current injection was demonstrated to deteriorate interruption (multiple zero crossings) because of prolonged arcing which resulted in thermal-based re-striking. The study of timing inaccuracies between the series connected vacuum interrupters demonstrated that interrupters that open firstly would have most significant voltage stress. The auxiliary power failure in mechanical DC CB would not change state of the breaker. Additional simulation studies would be required to assess the stresses on a full-scale mechanical DC CB under component failure, however, this falls out of the scope of this report.

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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

6 APPENDIX - ULTRAFAST DISCONNECTOR DESIGN

Figure 6.1 show photograph of the porotype 5 kV UFD and Table 6.1 presents the parameter values for TC and driver. The TC and armature used in this UFD is shown in Figure 6.2. Two nine-turn TCs are driven from 2700 µF capacitors at voltage around 300 V to provide double (reciprocal) contact motion for opening/closing operation. The reciprocal motion results in an improvement in the contact separation speed. The mass of each moving assembly (armature, rod and contacts) is about 175 gr. The contacts maximum distance is about 3.5 mm.

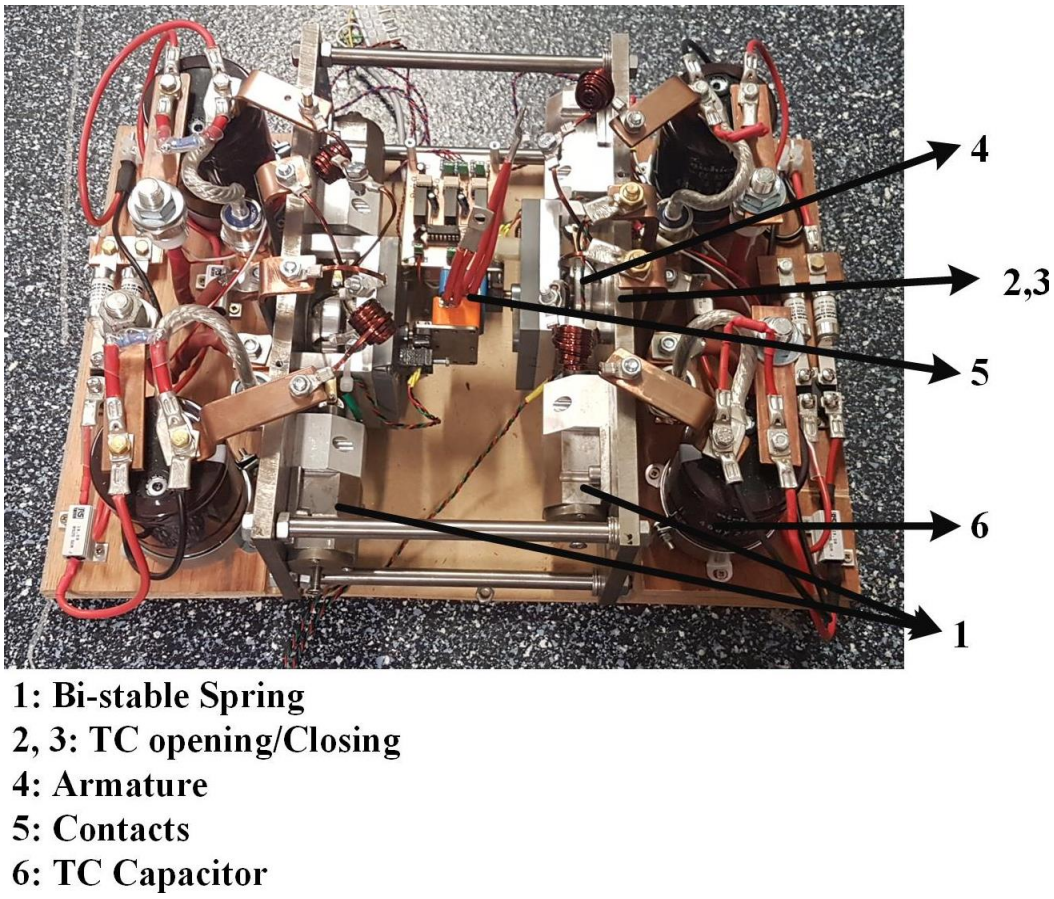

Figure 6.1. Photograph of the laboratory 5kV UFD.

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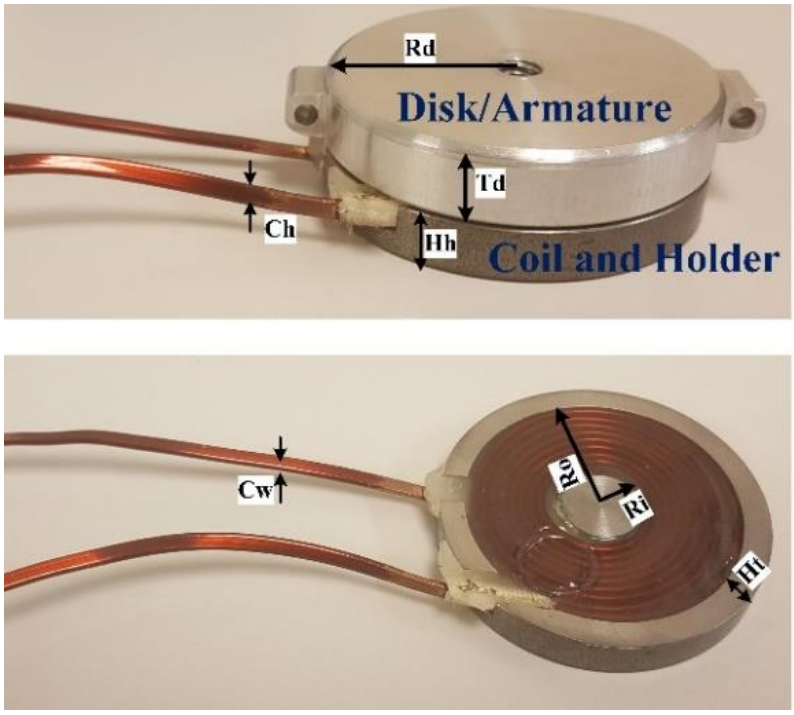

Figure 6.2. The laboratory Thomson Coil (coil, holder and armature)

Table 6.1 TC and TC driver parameters for a 5 kV and 320 kV UFD

Parameters	5 kV	320 kV
Capacitor bank (C_{tc})	2.7 mF	11 mF
Voltage (V_{tc})	300 V	900 V
R_C	15 mΩ	20 mΩ
Disk radiuses (R_d)	25 mm	65 mm
Disk thickness (T_d)	10 mm	30 mm
Disk material	Aluminum	Aluminum
Thickness of holder (H_t)	4.5 mm	6 mm
Height of holder (H_h)	7 mm	10 mm
Holder martial	Carbon Steel	Carbon Steel
Number turn	9	20
Coil width (C_w)	1.4 mm	2 mm
Coil height (C_h)	2.75 mm	4 mm
Inner radiuses of coil (R_i)	6.5 mm	27.5 mm
Outer radius of coil (R_0)	21 mm	47.5 mm

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