D9.1 – Real-time models for benchmark DC grid systems
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<thead>
<tr>
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<table>
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<tr>
<th>TERM</th>
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<tbody>
<tr>
<td>ACCB</td>
<td>Alternating Current Circuit Breaker</td>
</tr>
<tr>
<td>CB</td>
<td>Circuit Breaker</td>
</tr>
<tr>
<td>CHIL</td>
<td>Control Hardware in the Loop</td>
</tr>
<tr>
<td>CMS</td>
<td>Caithness-Moray-Shetland</td>
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<tr>
<td>CO</td>
<td>Continuous Operation</td>
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<tr>
<td>DBS</td>
<td>Dynamic Breaking System</td>
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<tr>
<td>DCCB</td>
<td>Direct Current Circuit Breaker</td>
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<tr>
<td>DX.Y</td>
<td>PROMOTioN Deliverable, where ‘X’ is the WP number and ‘Y’ is the deliverable number of that WP e.g. D9.1</td>
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<tr>
<td>FRTS</td>
<td>Fault Ride Through Scenario</td>
</tr>
<tr>
<td>GB</td>
<td>Great Britain</td>
</tr>
<tr>
<td>HB</td>
<td>Half-bridge</td>
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<tr>
<td>HIL</td>
<td>Hardware in the Loop</td>
</tr>
<tr>
<td>HVDC</td>
<td>High Voltage Direct Current</td>
</tr>
<tr>
<td>IED</td>
<td>Intelligent Electronic Device</td>
</tr>
<tr>
<td>IP</td>
<td>Intellectual Property</td>
</tr>
<tr>
<td>KPIs</td>
<td>Key Performance Indicators</td>
</tr>
<tr>
<td>Meshed grid</td>
<td>Grid that contains at least one loop</td>
</tr>
<tr>
<td>MITS</td>
<td>Main Interconnected Transmission System</td>
</tr>
<tr>
<td>MMC</td>
<td>Modular Multilevel Converter</td>
</tr>
<tr>
<td>MOG</td>
<td>Meshed Offshore Grid</td>
</tr>
<tr>
<td>Multi-terminal</td>
<td>More than two stations</td>
</tr>
<tr>
<td>Point-to-Point</td>
<td>(Inter) connection between two points</td>
</tr>
<tr>
<td>PROMOTioN</td>
<td>Progress on Meshed HVDC Offshore Transmission Networks</td>
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<tr>
<td>PS</td>
<td>Permanent Stop</td>
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<tr>
<td>Radial grid</td>
<td>Grid that does not contain a loop</td>
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<tr>
<td>TERM</td>
<td>MEANING</td>
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<tr>
<td>RTS</td>
<td>Real-time Simulator</td>
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<tr>
<td>SM</td>
<td>Sub-module</td>
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<tr>
<td>TRL</td>
<td>Technology Readiness Level</td>
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<td>TS</td>
<td>Temporary Stop</td>
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<tr>
<td>VSC</td>
<td>Voltage-source Converter</td>
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1 INTRODUCTION TO DEMONSTRATION OF HVDC PROTECTION SYSTEMS AND ASSOCIATED REAL-TIME MODELLING

1.1 INTRODUCTION

Within the PROMOtion project there have been many developments in: HVDC protection strategy and protection algorithm design (WP4); HVDC protection IED development and test (WP4 towards WP9); and modelling and testing of HVDC circuit breakers (WP5, WP6 and WP10). The aim of WP9 is to validate the correct operation and performance of protection strategies designed in WP4, with representative HVDC circuit breaker models from WP6, in a realistic HVDC network and with prototype hardware protection IEDs. Whilst the protection strategies have been studied in detail in offline simulation, and the protection IEDs have been tested independently, the key contribution of WP9 is to test all of the elements together in system-level tests in order to validate the correct operation of the protection system as a whole. This real-time validation is performed for both non-selective HVDC protection, partially selective HVDC protection, and fully selective HVDC protection.

This document describes the base models used for testing of the partially and fully selective protection strategies for demonstration events D9.3 and D9.4 covering the topics of partially selective HVDC protection, and fully selective HVDC protection. The non-selective strategy is covered separately in the modelling report equivalent to this, D9.5, and a further demonstration event D9.6.

1.2 HARDWARE AND REAL-TIME SIMULATION COMPONENTS

The validation of partially and fully selective HVDC protection strategies can be considered realistic and a step beyond the simulations performed in WP4, due to the combination of hardware devices (both an industrial HVDC protection IED prototype and an academic HVDC protection IED) and validated real-time simulation models (of both the HVDC system and the HVDC circuit breakers). The combination of these key components will bring confidence in the conclusions of future technical results, and aim to contribute to an increase in TRL for HVDC grid protection through the demonstration of HVDC protection systems in as realistic environment as possible without testing in a real power system.

1.2.1 AIM AND SCOPE OF REAL-TIME SIMULATION

The benefit of performing simulations in real-time is that hardware devices (protection IEDs and converter control replicas) are to be tested. These devices must be interfaced to the real-time simulation in a Control Hardware-in-the-Loop (CHIL) configuration. Real-time simulation models of sufficient fidelity are required to represent the salient features of the power system that should be represented. Models have to be representative in steady-state and under transient conditions (both fault and non-fault scenarios) such that realistic stimuli can be provided to the CHIL and so that the impact of the CHIL action on the power system simulation can be evaluated. The models should be representative for all anticipated test cases, including (but not limited to): system start-up, non-fault
switching, power flow reversal, system reconfiguration, DC-side faults, converter station fault response (blocking, ACCB protection), post-fault converter behaviour and AC-side faults. The simulations (and the results to be captured) will focus on several aspects; correct operation of the protection IEDs, the correct operation of the overall protection system, and operational performance of a multivendor HVDC protection system.

1.2.2 INTRODUCTION TO HVDC SYSTEM TOPOLOGY AND CONFIGURATION

Testing of partially selective and fully selective protection strategies will be performed on the most realistic simulation model of an industrial multiterminal HVDC network that can be developed within the project. Open-access converter models have been configured to represent the fully designed three-terminal extension to the existing point-to-point Caithness-Moray HVDC scheme. The three-terminal HVDC system is modelled in the RTS with realistic HVDC cable parameters. The use of a validated real-time simulation model – with the associated project-specific details that were not available in previous work – allows HVDC protection to be thoroughly evaluated in the context of a realistic system.

1.2.3 INTRODUCTION TO PROTECTION IED HARDWARE

Two HVDC protection IED prototypes are available for testing; the PROMOTioN WP4 prototype (developed at KTH, Stockholm) and the Mitsubishi Electric prototype. Each is programmed with one or more line protection algorithms, and can execute the same algorithm(s) within multiple functional units, nominally representing several lines around a bus. The use of both industrial and academic prototypes aims to validate that detection and discrimination of faulted lines is possible in a realistic system (e.g. not just in simulation for which some elements of a real device might be idealised), and the overall protection system is operable. The performance of the protection IEDs within the overall protection system will be examined. Multi-vendor interoperability will also be examined.

1.2.4 INTRODUCTION TO CIRCUIT BREAKER MODELS

HVDC circuit breaker (CB) modelling has been examined in detail in WP6, and validated models have been developed in collaboration with manufacturers [1]. These models will be integrated into the test setup for the partially selective and fully selective testing, allowing for an accurate representation of the circuit breaker behaviour and associated device and network constraints (e.g. maximum current, energy dissipation, opening and reclosing performance). Two circuit breaker topologies have been examined, with models representing the Mitsubishi Electric mechanical circuit breaker and the ABB hybrid circuit breaker.

1.2.5 INTRODUCTION TO CONVERTER CONTROL MODELS

The modular multi-level converters implemented in the multi-terminal HVDC system are based on open-source real-time models commissioned by The National HVDC Centre and developed through a research project in collaboration with the University of Strathclyde, UK [2-4].

1.2.6 INTRODUCTION TO CONVERTER CONTROL REPLICAS AND HVDC SYSTEM REPLICAS

Manufacturer replicas of the CMS HVDC system [5] have been used for internal validation of non-selective simulation models (the ‘base case’ from which partially selective and fully selective models are developed). This
is not to say that the performance has been truly replicated but to give confidence that the responses are realistic. Use of the replicas for validation increases confidence that the results presented are representative of a realistic industrial system.

1.3 REVIEW OF EXISTING WORK ON HVDC PROTECTION STRATEGIES

Extensive study has been performed in WP4, first considering a high-level comparison of protection strategies (e.g. non-selective, partially-selective, fully-selective) and particular implementations of protection strategies (e.g. with mechanical or hybrid HVDC CBs in fully-selective strategy), including the study of suitable protection algorithms [6]. Detailed analysis and comparison of selected protection strategies and implementations were then performed, for each of which key performance indicators (KPIs) were evaluated. Detail of relevant device trade-offs are included where appropriate (e.g. for pole rebalancing equipment) [7]. In general, it has been shown that protection algorithms and strategies are available and successfully isolate HVDC faults with various strategy and implementation of specific trade-offs.

1.4 REVIEW OF EXISTING WORK TOWARDS TESTING AND SYSTEM INTEGRATION OF HVDC GRIDS

The intention of this document is to provide detail of the modelling and parameterisation of the HVDC network and associated controllers, systems, hardware, and other associated details. The system integration and system testing will therefore be not be covered in great detail in this document, however, the hardware/system integration, and the configuration of the testing (and associated test procedures) are clearly highly relevant.

Previous work has been published demonstrating a fully selective protection system from a single vendor indicating that one solution for the control and protection system may be viable [8], however, the protection system design is not optimised and the control and protection is performed in a centralised manner (i.e. not using standalone protection IEDs as is expected in a future meshed system [9]). There are several multiterminal VSC HVDC systems in operation or under construction today, including the Zhang Bei project which is a multivendor system [10, 11], although full details of the protection system are not publicly available.

Guidelines for functional specifications of HVDC systems are being introduced, including details on system integration [9]. The testing performed in PROMOTioN WP9 could be classified as ‘off-site testing of the HVDC control and protection system’ and will select tests from the ‘factory test scenarios’ presented in order to ensure thorough testing of the proposed protection systems [9].

1.5 GAPS AND OPPORTUNITIES

Existing work in WP4 has extensively examined the most promising HVDC protection strategies for protection of a multiterminal HVDC system against DC-side faults. Work has thoroughly examined operation on simplified networks, and each protection strategy implementation has been evaluated against harmonised performance indicators. It has been shown that each protection strategy can effectively protect an HVDC network, with various trade-offs. Considering AC system impact, the choice of protection strategy influences the duration of momentary loss-of-infeed / loss-of-export of real and reactive power to the connected AC system. Different protection strategy
implementations could also have implications, e.g. different numbers of circuit breakers (which could be costly) and different sized additional inductance (which can reduce the dynamic performance of the HVDC system as well as increasing costs, especially offshore where space and weight allowance is at a premium).

WP4 has provided a robust overview of the different options, and their application to generic test networks. The parameters of these test networks and associated components are approximated based on best practice, common assumptions and published information on existing and planned HVDC systems. The network topologies under examination were chosen to be interesting test cases for the demonstration of HVDC protection systems. The converter models are based on publicly available data and therefore cannot be fully representative of a real converter station with the associated confidential control structure. Although significant efforts have been made to attempt to make the WP4 simulations as realistic as possible, with reasonable assumptions made where necessary, it should be clear that these networks do not fully represent a real system.

In this respect, there is a significant opportunity in WP9 to implement protection strategies on a more realistic network topology and validate the successful operation of HVDC protection on a realistic system (e.g. with realistic converters, realistic cable parameters and lengths…). The use of hardware protection IEDs in WP9 will allow further demonstration of the readiness of HVDC protection technologies. The final goal is to increase the TRL in HVDC protection. Additionally, it can be shown that elements of a multi-vendor protection system are feasible – this is something that is examined in WP4 but can only be fully validated in WP9 (e.g. circuit breakers from multiple vendors, protection IEDs from multiple vendors,…).
2 METHODOLOGY

The reasoning behind the network topologies and protection system configurations for the partially selective and fully selective protection validation is discussed in the following sections.

2.1 NETWORK TOPOLOGIES TO BE CONSIDERED

With the focus being to prove the technology on the most realistic system possible the base case was selected as the proposed (and fully designed) Caithness-Moray-Shetland (CMS) radial multiterminal HVDC scheme. The Caithness-Moray section is embedded within the main integrated transmission system (MITS) in GB. Shetland however is a standalone island system, not currently connected to the MITS. The first phase of the project links Spittal in Caithness and Blackhillock in Moray with ±320kV submarine HVDC cables. However, as shown in Figure 1 the scheme is designed as a three, four or five multi-terminal scheme allowing for future extension [12].

![Figure 1: Schematic of Full CMS HVDC Scheme](image)

Currently, Phase 1 Caithness-Moray radial connection is in operation, commissioning having completed in December 2018. This phase was not considered for the WP9 testing given that a point-to-point scheme would not typically require a DC-side protection scheme such as those under examination in the PROMOTioN project.
For the partially selective scheme that is considered for this testing, it was conceivable that a DCCB and associated protection logic could be added to the scheme at the DC switching station on the feeder to the yet to be constructed Shetland terminal. This would bring the benefit of continued operation of the embedded HVDC link between Caithness and Moray for any cable faults on the long subsea cable to Shetland. Full system details are provided in Section 4.

### 2.2 PROTECTION SYSTEM DESIGN METHODOLOGY

There are several key choices when designing a protection system, including the selection of protection strategy and implementation. The choices can impact the performance of the protection system, the impact of a DC fault, and the cost of the protection system, in addition to the dynamic performance in non-fault conditions. The flow chart in Figure 3 is a workflow to determine the specification of a protection system based on functional system requirements. Each step is discussed in detail in the following sections. Note that this is one method to make reasonable choices based on technical performance parameters, however, there are other possible methods which could achieve different results, and in a real system, it would be expected that a cost-benefit analysis (CBA) would be used to fully assess the techno-economic trade-offs. Preparation of cost-benefit analysis from a protection point of view is investigated in PROMOTiON deliverable D4.7. It should be expected that achieving a final design would be an iterative process.
2.2.1 CHOICE OF PROTECTION PHILOSOPHY

Depending on the constraints of the connected AC system(s), a choice of overall protection philosophy must be made. The system could be protected by a non-selective, partially selective, or fully selective protection system (these terms are defined in [6]), each of which implies a variety of trade-offs regarding possible cost of protection system and prospective impact.

2.2.2 DEFINITION OF MINIMUM BEHAVIOUR AT EACH CONVERTER

An HVDC fault can have various implications on converter station operation, which can be in part defined by the protection matrix approach taken in D4.2; each converter station having the option of continuous operation (CO) which is defined as no blocking, temporary stop (TS) for which a short duration outage of power transmission is allowable and permanent stop (PS) for which no power flow recovery is required in the seconds following the fault [6]. An extension of this method can be to define more detailed fault ride through strategies for each converter location [14]. The choice of converter behaviour leads to subsequent design choices which impact, for example, required circuit breaker speed and required additional fault current limiting inductance. Three possible fault ride through scenarios (FRTS) are as follows: DC-FRTS1 does not allow any converters to be blocked (CO) and therefore implies a requirement for large inductors and/or fast circuit breakers; DC-FRTS2 allows for temporary blocking of local converters (TS), while remote converters are not allowed to block (CO); and DC-FRTS3 allows all converters on the network to block (TS). The selection would be influenced by the AC system requirements.
2.2.3 CHOICE OF PROTECTION SYSTEM IMPLEMENTATION

The particular implementation of the protection strategy should then be examined. In particular, for partially-selective or non-selective protection strategies there are choices between protection devices (e.g. for non-selective a converter station could be protected using AC-side CBs at an HB-MMC, a FB-MMC, or an HB-MMC + DC-side CB). Any constraints in protection system equipment should also be identified here (e.g. constraint regarding circuit breaker topology or operation speed).

2.2.4 LOCATION OF CIRCUIT BREAKERS AND OTHER PROTECTION EQUIPMENT

The protection system should be designed according to operational constraints on the HVDC network and connected AC systems (e.g. for partially selective strategies there may be operational advantages to one part of the system having a higher availability). Locations for other protection related switchgear (e.g. high-speed switch) should also be identified here. Any additional protection equipment should also be specified, for example, pole rebalancing equipment.

2.2.5 SELECTION OF INDUCTOR RATING

Additional current limiting inductance at the cable ends, where present (e.g. anticipated in all partially-selective and non-selective strategies), should be specified according to the system that has been designed.

The additional current limiting inductor sizing is a system design choice. The required inductor size is dependent on the network configuration and location (e.g. system voltage, number of converters at the bus, number of cables at the bus, length of cables, ...). For a particular location, a larger inductor implies a requirement for a circuit breaker with a lower current breaking capacity and/or a circuit breaker with slower operation time, while a smaller inductor implies a requirement for a faster circuit breaker and/or a higher current breaking capacity. Additionally, the HVDC converter also could block based on overcurrent, therefore the inductor sizing impacts the response of the converter to a fault. Given all of these trade-offs, the defined DC-FRTS are used to categorise fault responses and appropriately size the associated additional inductance [14].

For networks which do not allow any converter stations to be blocked (DC-FRTS1), the analytical method in reference [14] can be used to determine the required inductor size. This method – using an analytical approximation representing the fault response of the converter and the additional inductance – estimates the expected current following a DC cable fault and can calculate the required inductor value for each converter to ensure that they will not be blocked.

For networks which allow converters local to the fault to be blocked but remote converters not to be blocked (DC-FRTS2), the analytical method in reference [14] can be used. The method – using an analytical approximation representing the time-dependent dynamics of both the converter and the cable – can be used to output the expected fault current at the converter, and through iteration can determine the requirement for the inductor size in order for remote converter stations to remain in continuous operation following a DC fault.
For networks for which all converters are allowed to block following a fault (DC-FRTS3), time-domain simulations can be used to determine the required inductor sizing according to the operation time of the HVDC CB. Through manual or automated time-domain simulation, the minimum inductor size which allows the circuit breaker to isolate the fault in the time (circuit breaker operation time + fault detection time) before the peak circuit breaker current is exceeded can be determined.

2.2.6 EXAMINATION/DEFINITION OF BACKUP PROTECTION STRATEGY

All protection strategies require a method of backup protection which must operate in case a failure in primary protection. The exact implementation depends on the protection strategy and also the level of reliability that is required from the system. For example, it might be allowable for one particular partially-selective system to use AC-side protection in case of DC CB failure, while another system might require the application of redundant DC CBs.

For networks on which backup protection is provided by adjacent CBs (AC and/or DC), there is no anticipated requirement for an increase in additional inductance for the purposes of backup protection (e.g. as discussed in [15]).

For the case of redundant (i.e. series) circuit breakers, the need for increasing the additional inductance depends on the desired compliance to fault ride through scenarios and in some cases the equipment that will be providing the backup protection. If it is acceptable for, in the case of backup protection, the DC-FRTS requirement to be relaxed, then there is no anticipated requirement for increasing the additional inductance. If the DC-FRTS requirements must be complied with, even in the event of backup protection, then the fault current limiting inductance may need to be increased to take into account backup protection (e.g. when using series redundant DC CBs that take additional time to operate following the detection of primary protection failure).

2.2.7 SETTING OF PROTECTION IED THRESHOLDS

The initial IED threshold setting can be determined by investigating the algorithm behaviour for the fault that is: hardest to detect inside of the protection zone (usually at the remote line end); and for the fault hardest to discriminate outside of the protection zone (usually close backward fault). The threshold should be set with sufficient margins, i.e. sufficiently below the fault that is hardest to detect (dependable) and sufficiently above the worst fault for which no trip is to be issued (secure). Margins are important to consider modelling inaccuracies. Note that these initial threshold settings still need to be systematically batch-tested.

2.3 REAL-TIME SIMULATION OF HVDC NETWORKS

2.3.1 REAL-TIME SIMULATION EQUIPMENT

To perform any closed-loop studies using the prototype equipment, a real-time simulator (RTS) is required. This is a combination of hardware and software which allows the test devices to operate as if connected to a real system. An RTS allows the testing and operation of the prototype IED(s) in real-time (known as ‘hardware-in-the-loop’ or HIL) [3].
With offline simulation, as the test system increases in size and/or complexity the simulation time increases. However, for the real-time simulation, the time allowed to compute each time step is fixed therefore the available hardware becomes the limitation on system size and/or complexity. The National HVDC Centre uses RTDS® Technologies simulator hardware, with the RSCAD software. The hardware available comprises:

- 6 x NovaCor chassis (RTDS®’s latest generation hardware);
- 3 x RTDS Racks, each including (5 x PB5 cards, 1 x GTWIF);
- 12 x FPGA Units (flexible support units typically used to simulate the valves or small-time step frequency dependent cable models);
- A GTSYNC card (to synchronise simulations); and
- A range of input/output cards: GTNETx2, GTAO, GTAI, GTDO and GTDI.

This provides significant simulation capability, both in terms of simulated network size and complexity.

![Photograph of the NovaCor and GTFPGA Units.](image)

2.3.2 CONFIGURATION OF REAL-TIME SIMULATION MODELS

All converter stations and DC-side electrical circuits are simulated in the small-time step (~3 µs). All AC-side circuits are simulated in the main time step (50 µs). Each converter model is executed in a small-time step bridge box and connected to the rest of the network using small time step stub lines. Cables are modelled using frequency-dependent phase domain representations (the most accurate commercially available model), executed at a small-time step on a GTFPGA unit. No communication is used for time-sensitive operations (e.g. DC protection). Any communication performed is delayed by an appropriate time for the distance travelled. The three-terminal network requires two NovaCor simulators. AC networks are modelled in the main time step as a source and equivalent impedance. Further details are presented in Section 3.5.
2.4 PROTECTION IED HARDWARE INTERFACES

Within WP9, two hardware IEDs are utilised. Each has a number of digital and analogue inputs and outputs, used for measurement and DCCB tripping. The IEDs are software programmable, allowing various algorithms to be verified. A typical set-up is shown in Figure 5, where the IED covers a single bus, four lines and one converter station connection. The exact connection of the device is system and test condition specific.

Generally, the analogue signals of voltage and current for each pole of each circuit need input to the IED from the RTS (these are the signals that are processed by the IED to decide if a fault is present); a digital reset needs input to the IED (this allows for automation of multiple tests without requiring a manual reset) from the RTS; and the digital trip signals need to be output from the IED into the RTS (this indicates when a protection sequence should be initiated).

![Diagram of HVDC protection IED](image)

Figure 5: Example configuration of HVDC protection IED around a HVDC bus [16]

Full details of the PROMOTioN protection IED are provided in reference [16].
3 THREE-TERMINAL SYSTEM FOR DEMONSTRATION

This section describes the details of the network topology and the models and hardware devices that will be used to demonstrate the three-terminal HVDC network in the real-time simulation environment.

3.1 THREE-TERMINAL HVDC SYSTEM

A 3-terminal, 2-circuit HVDC network, which connects a converter station on an island AC network to two onshore converter terminals embedded into a mainland AC grid, is used for demonstration of non-selective, partially selective and fully selective DC protection strategies. The multi-terminal HVDC scheme uses voltage source converter (VSC) technology based on the modular multi-level (MMC) type.

3.1.1 ARCHITECTURE AND DESIGN

The 3-terminal DC network is modelled using the RSCAD real-time simulation tool for hardware-in-the-loop testing of the three different DC protection strategies. Figure 6 shows the schematic diagram for the 3-terminal DC network for the non-selective strategy with no DC circuit breakers.

Figure 6: DC network for non-selective strategy with no DC circuit breakers

Figure 7 shows the schematic diagram for the 3-terminal DC network for the partially selective strategy with DDCB at the ‘DC Switching Station’ for the connection to ‘Convertor Station 3’.

Figure 7: DC network for partially selective strategy
Figure 8 shows the schematic diagram for the 3-terminal DC network for the fully selective strategy with DCCBs at the ‘DC Switching Station’ for all connections.

Table 1 is a summary of the technical parameters for the three-terminal VSC-HVDC system.

### Table 1: Parameters of 3-Terminal HVDC System

<table>
<thead>
<tr>
<th>Item</th>
<th>Station 1</th>
<th>Station 2</th>
<th>Station 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Apparent Power (S)</td>
<td>840MVA</td>
<td>1265MVA</td>
<td>626MVA</td>
</tr>
<tr>
<td>Rated Active Power (P)</td>
<td>±800MW</td>
<td>±1200MW</td>
<td>±600MW</td>
</tr>
<tr>
<td>Converter Nominal DC Voltage</td>
<td>640kV (±320kV)</td>
<td>640kV (±320kV)</td>
<td>640kV (±320kV)</td>
</tr>
<tr>
<td>Converter Nominal AC voltage</td>
<td>380kV</td>
<td>380kV</td>
<td>380kV</td>
</tr>
<tr>
<td>AC Grid Voltage</td>
<td>275kV</td>
<td>400kV</td>
<td>132kV</td>
</tr>
<tr>
<td>Nominal Frequency</td>
<td>50Hz</td>
<td>50Hz</td>
<td>50Hz</td>
</tr>
<tr>
<td>SCR</td>
<td>2.5</td>
<td>15</td>
<td>-</td>
</tr>
<tr>
<td>X/R Ratio</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Transformer rated Power</td>
<td>840MVA</td>
<td>1265MVA</td>
<td>626MVA</td>
</tr>
<tr>
<td>Transformer Voltage ratio</td>
<td>275/380kV</td>
<td>400/380kV</td>
<td>132/380kV</td>
</tr>
<tr>
<td>Transformer Reactance</td>
<td>0.16pu</td>
<td>0.16pu</td>
<td>0.16pu</td>
</tr>
</tbody>
</table>

Table 2 is a summary of the modular multilevel converter parameters.

### Table 2: MMC System parameters

<table>
<thead>
<tr>
<th>Item</th>
<th>MMC 1</th>
<th>MMC 2</th>
<th>MMC 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arm inductance</td>
<td>13%</td>
<td>13%</td>
<td>13%</td>
</tr>
<tr>
<td>Number of cells per arm (N)</td>
<td>350</td>
<td>350</td>
<td>350</td>
</tr>
<tr>
<td>Cell capacitance</td>
<td>7.2mF</td>
<td>10.8mF</td>
<td>5.4mF</td>
</tr>
<tr>
<td>Average cell capacitance</td>
<td>20.55μF</td>
<td>30.83μF</td>
<td>15.4μF</td>
</tr>
</tbody>
</table>
Table 3 is a summary of the wind farm system parameters.

<table>
<thead>
<tr>
<th>Item</th>
<th>Windfarm (WF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Apparent Power (S)</td>
<td>626MVA</td>
</tr>
<tr>
<td>Rated Active Power (P)</td>
<td>±600MW</td>
</tr>
<tr>
<td>Converter Nominal DC Voltage</td>
<td>1.2kV</td>
</tr>
<tr>
<td>Converter Nominal AC voltage</td>
<td>0.69kV</td>
</tr>
<tr>
<td>AC Grid Voltage</td>
<td>132kV</td>
</tr>
<tr>
<td>Nominal Frequency</td>
<td>50Hz</td>
</tr>
<tr>
<td>Transformer rated Power</td>
<td>840MVA</td>
</tr>
<tr>
<td>Transformer Voltage ratio</td>
<td>132/0.69kV</td>
</tr>
<tr>
<td>Transformer Reactance</td>
<td>0.16pu</td>
</tr>
<tr>
<td>Local Load</td>
<td>100MW</td>
</tr>
</tbody>
</table>

3.2 MMC CONVERTER MODELLING AND CONTROL DESIGN

The modular multi-level converters implemented in the multi-terminal HVDC system are based on open-source real-time models commissioned by The National HVDC Centre and developed through a research project in collaboration with the University of Strathclyde, UK. This section is adapted from [2-4] and describes the converter architecture, outlines the control strategy and highlights the validation approach.

3.2.1 HALF-BRIDGE MMC MODELLING METHOD

shows a typical power circuit for the three-phase MMC with half-bridge type sub-modules (SMs), which consists of six arms, with each arm comprising of a chain link between the SMs and an arm inductor.

Use of an MMC average model was promoted by the need to have computation efficient model suitable for wide range of power system studies. To achieve this objective, the following assumptions are made:

The switching voltages being developed across the upper and lower arms of each phase are replaced by their average voltages meaning the inter-SM dynamics in each arm is neglected; thus, SM capacitor voltages of each arm oscillate together (considering the SM voltages in each of the arm are balanced),
This representation can be used to calculate the average voltage and the total SM capacitor voltage of each arm when the MMC is in operation, as graphically shown in Figure 10(a) for an upper arm. However, to accurately mimic the typical MMC behaviour when all its switches are blocked, i.e. all the IGBTs in the SMs are switched or gated off (e.g. during a DC fault), additional considerations are required to ensure all the possible current paths are included in the model. Considering the current paths in the upper MMC arm with a detailed representation of the switching devices as shown in Figure 10(b), when the gating signals to the MMC are inhibited (or blocked), the positive arm current (when $i_{\text{arm}}$ is pointing downward) flows through the diodes $d_{\text{X}}$ and the SM capacitor and thus, the arm voltage will be the combined DC voltages of the SM capacitors. Whilst the negative arm current (when $i_{\text{arm}}$ is pointing upward) flows through each SM through the freewheeling diode $d_{\text{m}}$ that bypasses the SM capacitor. Thus, the arm voltage is considered to be zero. Figure 10(c) shows the averaged model with additional IGBTs and diodes devices providing the necessary conduction path to facilitate the recreation of the MMC typical behaviour during blocked states. The modified MMC average arm presents identical to those shown in Figure 10(d). Also, when the converter blocking is activated (gated-off of all switches), the switch $s_x$ must be turned off and $m$ is set to 1 to mimic the MMC behaviour stated above, particularly, quenching of the positive arm current.
3.2.2 MMC CONTROL SYSTEM DESIGN

Figure 11 (a) depicts the generic control block diagram of the MMC used. A detailed block diagram that highlights individual controllers of the MMC employed are summarized in Figure 11(b). This includes the inner and outer loop controls required for giving a realistic response for the studies. Full details are available in [2].
3.2.3 DC CABLE

A travelling wave frequency-dependent phase model is used for the DC cable of the 3-terminal system implemented in RSCAD. The DC cable parameters and lengths are representative of the Caithness Moray HVDC transmission project [17].

The use of the appropriate cable model is very important for the protection studies to be undertaken. This model gives accurate v, i characteristics. This is important for realistic detection by IED which in turn is important for overall protection system TRL demonstration. If a less detailed (i.e. not frequency dependant representation) or one which executed at a larger time step (i.e. less definition) was used then it would have a negative impact on the assessment of the IED performance since they have high sample rates and very fast operation times, as required for HVDC application.
3.3 PROTECTION SYSTEM DESIGN FOR THREE-TERMINAL RADIAL HVDC NETWORK

According to the method presented in Section 2.2, the protection system will now be designed for several protection philosophies and protection system implementations; both partially selective and fully selective protection of the three-terminal network, and with the hybrid circuit breaker and the mechanical circuit breaker. These options are chosen to enable validation of several protection philosophies and with circuit breakers from several manufacturers.

3.3.1 SYSTEM OPTIONS

Even for the three-terminal radial design described there are a great number of combinations of possible options. Table 4 summarises all the possible options. For the following sections the fully selective design was limited to a single DCCB technology to manage the scope of the work. Similarly only DC-FRTS3 was considered – this particular behaviour was chosen as the lower inductance of this choice is the most onerous for the IEDs, the devices under test.

<table>
<thead>
<tr>
<th>Base Model</th>
<th>Minimum Behaviour at Each Convertor</th>
<th>Protection Philosophy</th>
<th>IED</th>
<th>DCCB Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Three terminal System</td>
<td>DC FRTS1 DC-FRTS2 DC-FRTS3</td>
<td>Partially Selective</td>
<td>Simulated MELCO PROMOTioN WP4 Mix*</td>
<td>Mechanical Hybrid Mix*</td>
</tr>
</tbody>
</table>

*For a fully selective scheme there are many possible combinations of IED/DCCB placement
3.3.2 PARTIALLY SELECTIVE WITH MECHANICAL CIRCUIT BREAKER

To examine a partially selective protection strategy with mechanical circuit breakers, the following protection system design choices are made. Converter stations across the network will be allowed to temporarily block following a fault (DC-FRTS3). According to the design of the three-terminal network, Section 3.1.1 and Figure 7, one circuit breaker per pole will be used to split the HVDC network in the event of a DC fault, on Cable 3 at the switching station. According to DC-FRTS3, an inductor value (to be replicated on both positive and negative poles at the circuit breaker location) is then determined from time-domain simulation, in which the minimum inductance required to operate the DC CB within its operational limits (for the mechanical circuit breaker 16 kA peak current and 8 ms operation time) is evaluated. Based on the time domain simulation the inductor value for this protection system design case is 105 mH. The backup protection strategy (in case the DC CB fails to isolate the fault or in case the protection IED fails to detect the fault) is the operation of the CBs at the AC-side of the converter stations. As such, there is no requirement for additional inductance at the DC CB to allow for backup protection operation. The protection system design is summarised in Figure 12.

![Diagram of protection system design](image)

**Figure 12:** Protection system design for partially selective protection of the three terminal network with mechanical circuit breakers.
3.3.3 PARTIALLY SELECTIVE WITH HYBRID CIRCUIT BREAKER

To examine a partially selective protection strategy with hybrid circuit breakers, the following protection system design choices are made. Converter stations across the network will be allowed to temporarily block following a fault (DC-FRTS3). According to the design of the three-terminal network, Section 3.1.1 and Figure 7, one circuit breaker per pole will be used to split the HVDC network in the event of a DC fault, on Cable 3 at the switching station. According to DC-FRTS3, an inductor value (to be replicated on both positive and negative poles at the circuit breaker location) is then determined from time-domain simulation, in which the minimum inductance required to operate the DC CB within its operational limits (for the hybrid circuit breaker 16 kA peak current and 2 ms operation time) is evaluated. Based on the time domain simulation the inductor value for this protection system design case is 25 mH. The backup protection strategy (in case the DC CB fails to isolate the fault or in case the protection IED fails to detect the fault) is the operation of the CBs at the AC-side of the converter stations. As such, there is no requirement for additional inductance at the DC CB to allow for backup protection operation. The protection system design is summarised in Figure 13.

![Diagram](image_url)

**Figure 13:** Protection system design for partially selective protection of the three terminal network with hybrid circuit breakers
To examine a fully selective protection strategy with mechanical circuit breakers, the following protection system design choices are made. Converter stations across the network will be allowed to temporarily block following a fault (DC-FRTS3). According to the design of the three-terminal network, Section 3.1.1 and Figure 8, one circuit breaker per pole will be applied at the switching station end of each cable. According to DC-FRTS3, an inductor value (to be replicated on both positive and negative poles at each circuit breaker location) is then determined from time-domain simulation, in which the minimum inductance required to operate the DC CB within its operational limits (for the mechanical circuit breaker 16 kA peak current and 8 ms operation time) is evaluated. Based on the time domain simulation the inductor value for this protection system design case is 70 mH for the circuit breaker on line 1, 55 mH for the circuit breaker on line 2, and 60 mH for the circuit breaker on line 3. The backup protection strategy (in case the DC CB fails to isolate the fault or in case the protection IED fails to detect the fault) is the operation of the CBs at the AC-side of the converter stations. As such, there is no requirement for additional inductance at the DC CB to allow for backup protection operation. The protection system design is summarised in Figure 14.

Figure 14: Protection system design for fully selective protection of the three terminal network with mechanical circuit breakers
3.3.5 FULLY SELECTIVE WITH HYBRID CIRCUIT BREAKER

To examine a fully selective protection strategy with hybrid circuit breakers, the following protection system design choices are made. Converter stations across the network will be allowed to temporarily block following a fault (DC-FRTS3). According to the design of the three-terminal network, Section 3.1.1 and Figure 8, one circuit breaker per pole will be applied at the switching station end of each cable. According to DC-FRTS3, an inductor value (to be replicated on both positive and negative poles at each circuit breaker location) is then determined from time-domain simulation, in which the minimum inductance required to operate the DC CB within its operational limits (for the hybrid circuit breaker 16 kA peak current and 2 ms operation time) is evaluated. Based on the time domain simulation the inductor value for this protection system design case is 15 mH for the circuit breaker on line 1, 15 mH for the circuit breaker on line 2, and 20 mH for the circuit breaker on line 3. The backup protection strategy (in case the DC CB fails to isolate the fault or in case the protection IED fails to detect the fault) is the operation of the CBs at the AC-side of the converter stations. As such, there is no requirement for additional inductance at the DC CB to allow for backup protection operation. The protection system design is summarised in Figure 15.

![Figure 15: Protection system design for fully selective protection of the three-terminal network with hybrid circuit breakers](image-url)
3.4 DC PROTECTION DEVICES

The following section describes the models and hardware that will be used for demonstration of partially selective and fully selective protection strategies.

3.4.1 HVDC CIRCUIT BREAKERS

Real-time HVDC circuit breaker models, developed in RSCAD by the PROMOTioN project partners in Work Package 6 (WP6) are used for demonstration of partially-selective and full-selective DC protections strategies in WP9. Details of the DCCB designs are briefly summarised in the following sections, are presented in detail in [1, 18-20].

3.4.1.1 CIRCUIT BREAKER MODEL 1 (ADAPTED FROM[1])

Circuit breaker model 1 represents the Mitsubishi Electric mechanical DC circuit breaker, Figure 16. The circuit breaker has a rated current of 16 kA and an 8 ms operation time. There is an option to include functionality to perform multiple circuit breaker operations (i.e. Open-Close-Open).

3.4.1.2 CIRCUIT BREAKER MODEL 2 (ADAPTED FROM[1])

Circuit breaker model 2 represents the ABB Hybrid DC circuit breaker, Figure 17. The model has been validated against a detailed PSCAD model in collaboration with industrial partners in WP9. The circuit breaker has a rated current of 16 kA and a 2 ms operation time. Control is available representing the opening sequence, closing sequence and there is provision for self-protection. The IGBT temperatures are also calculated with a thermal model.
3.4.2 HARDWARE INTELLIGENT ELECTRONIC DEVICE (IED)

Several physical protection IEDs will be used within the protection system validation; the PROMOTioN WP4 IED and the Mitsubishi Electric IED. Each protection IED has been pre-tested (i.e. unit tested) within WP4 and has been confirmed to operate successfully and in a timely manner when presented with realistic input waveforms [21, 22].

Details for the IED interfaces are provided in Section 2.4.

3.5 ONSHORE AC NETWORK REPRESENTATION

Although the focus of the protection studies and validation will be on the DC-side, it is important to represent the connected AC systems in a sufficiently accurate manner for the phenomena under study.

A three-phase Thevenin equivalent model is implemented to represent AC networks with different fault levels connected to the two onshore converter terminals on MMC1 and MMC2. The offshore wind farm is implemented using a 600MW two-level, 3-phase inverter with power control and a fixed DC voltage source.
4 PROTECTION SEQUENCES

Protection sequences have been detailed in WP4. This chapter summarises the sequences that will be used in WP9 and presents the steps that are required to implement those strategies for the demonstrator and with additional industrialised details where applicable. Each protection sequence includes primary and backup protection, and post-fault recovery.

4.1 PROTECTION SEQUENCES FOR NON-SELECTIVE AC CIRCUIT BREAKER STRATEGY (BASE CASE)

The following protection sequence, Figure 18, was developed in WP4 to perform protective actions and post-fault recovery in a non-selective HVDC network [1]. It is assumed that a similar protection sequence would be used in the non-selective CMS system, although in the present strategy this would be controlled manually by a system operator. It is used in WP9 as the ‘base case’ for which other protection strategies can be compared to. This protection strategy/sequence is only used for benchmarking/validation purposes.

Figure 18: Primary protection sequence for non-selective AC-side circuit breaker protection strategy. Reproduced from PROMOTioN Deliverable 4.3[1].
4.2 PROTECTION SEQUENCES FOR PARTIALLY-SELECTIVE STRATEGIES

The protection sequence for the partially selective protection strategy, Figure 19, uses a grid splitting HVDC circuit breaker at one or more positions in the network [1]. Generic protection sequences are included here to show the full protection sequence including recovery, although it is not presently planned to test post fault recovery on a partially selective system. Note that the HVDC Grid splitting takes place as a parallel process to the identification of the faulted line.

Figure 19: Primary protection sequence for partially selective protection strategy using DC circuit breakers. Reproduced from PROMOTioN Deliverable 4.3
4.3 PROTECTION SEQUENCES FOR FULLY-SELECTIVE STRATEGIES

The protection sequence for the fully-selective HVDC protection strategies is shown in Figure 20 (primary and backup protection). These generic protection sequences are being applied to the CMS system in the fully selective configuration. In the present implementation, the protection sequences are developed using control blocks in the real-time simulation.

Figure 20: Primary and backup protection sequence for fully selective protection strategies on a symmetrical monopolar system, including pole rebalancing using DBS. Reproduced from PROMOTioN Deliverable 4.3[1].
5 HVDC PROTECTION IED REAL-TIME SIMULATION MODEL

In the WP9 testing of HVDC protection systems, when testing HVDC networks with many nodes, it will not always be possible to provide a hardware protection IED for each cable end (due to limited numbers of hardware protection IEDs). For the testing of faults in a particular network area, and for testing focused on examining the behaviour of the protection IED rather than the whole protection system, it is sometimes sufficient to simulate the protection IED. This section describes the real-time simulation models used when a simulated IED is required.

5.1 ALGORITHM(S) TO BE INCLUDED IN THE SIMULATED IED

It is the intention that all of the relevant available algorithms to be tested in hardware in WP9 will be represented in a simulation model so that hardware IEDs are not required for every node in the test network. In the present implementation the following algorithms have been implemented: voltage derivative, travelling wave-based, voltage threshold (Undervoltage), current threshold (overcurrent), current derivative and transient-based. The algorithms can be implemented independently or in conjunction. The algorithms implemented and corresponding conditions for fault detection are indicated in the Table 5.

Table 5: Fault Detection algorithms for DC lines

<table>
<thead>
<tr>
<th>Fault Detection Algorithm</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Derivative</td>
<td>$\Delta v \leq \Delta v_{\text{thresh}}$</td>
</tr>
<tr>
<td>Travelling-Wave Based</td>
<td>$\Delta(v - i \cdot Z_c) \leq (v - i \cdot Z_c)_{\text{thresh}}$</td>
</tr>
<tr>
<td>Undervoltage</td>
<td>$v \leq v_{\text{thresh}}$</td>
</tr>
<tr>
<td>Current Derivative</td>
<td>$\Delta i \geq \Delta i_{\text{thresh}}$</td>
</tr>
<tr>
<td>Overcurrent</td>
<td>$i \geq i_{\text{thresh}}$</td>
</tr>
</tbody>
</table>

5.2 FILTERS TO BE INCLUDED IN THE SIMULATED IED

Some algorithms in the IED require signal processing. This simulation provides options for implementing the following discrete-time filters: a casual FIR filter (average of 10 most recent values), a 2nd order Butterworth filter and a 2nd order Chebyshev filter. The filter specifications are outlined in the Table 6. The coefficients for the Butterworth and Chebyshev filter can be configured in the associated C file (IED_v1_0.c).

Table 6: Filters available in the simulated IED

<table>
<thead>
<tr>
<th>Filter name</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIR</td>
<td>Weighted average of 10 most recent values</td>
</tr>
<tr>
<td>Butterworth</td>
<td>2nd order, a normalized cut-off frequency $w_n = 0.2$</td>
</tr>
<tr>
<td>Chebyshev</td>
<td>2nd order, a ripple of -1 dB, a normalized cut-off frequency $w_n = 0.2$</td>
</tr>
</tbody>
</table>
5.3 REAL-TIME MODELLING

A real-time simulation model of an HVDC protection IED has been developed in RSCAD, Figure 21. The configuration of the simulated IED allows for different algorithms to be enabled and for algorithm settings to be entered, Figure 22.

![HVDC protection IED simulation model](image1)

**Figure 21:** HVDC protection IED simulation model, capable of non-unit protection of an HVDC cable pole

![Configuration options](image2)

**Figure 22:** Configuration options for HVDC protection IED simulation model

5.4 IED PARAMETERS

One can activate the algorithm as an independent condition (OR gate) by setting the value of the enable parameter to 1. The algorithms can operate in conduction (AND gate) if the parameter values of two or more enable parameters are set to 2. For reference, see Figure 23.
Figure 23: Enable an algorithm (OR)

Figure 24: Enable multiple algorithms in conjunction (AND)

The threshold of the algorithm condition is set in a separate tab that appears when the corresponding algorithm is enabled, Figure 25.
The digital filters can be enabled in the “Filters” tab of the IED component settings, Figure 26.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Value</th>
<th>Unit</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIR</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Butterworth</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Chebyshev</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 26: Filter settings of the IED
6 PRACTICAL ASPECTS OF DC NETWORK DEMONSTRATIONS

There are numerous practical considerations to be taken into account when testing physical hardware in a HIL setup. This chapter provides a summary of some of the practical considerations to that need to be accounted for when designing and executing such tests.

6.1 SUMMARY OF MODEL DESCRIBED

With the focus being to prove the DC-side protection technology on the most realistic system possible, the base case was selected as the proposed (and fully designed) Caithness- Moray-Shetland (CMS) radial three-terminal HVDC scheme. Although not currently planned, it is conceivable that a DCCB and associated protection logic could be added to the scheme at the DC switching station on the feeder to the yet to be constructed Shetland terminal.

Hardware implementations of prototype protection IEDs were successfully integrated into a realistic multi-terminal HVDC system to implement testing of a partially selective protection scheme. This was achieved by building on the work through the PROMOTioN project; real-time DCCB models from Work Package 6 were combined with the protection schemes and hardware prototypes developed in Work Package 4.

The RTDS hardware used to implement the model described was:

- 2x NovaCor chassis (each with 5 out of 10 cores licensed and available for use);
- 5x GTFPGA Units (to simulate frequency dependant cables);
- 1x Global Bus Hub (to synchronise simulations, for two chassis simulation direct connection could have been used);
- 1x IRC Switch (for inter-rack communication, for two chassis simulation direct connection could have been used);
- 1x GTAO card (for outputting analogue signals from the simulation as inputs to the IED);
- 1x GTDI card (for inputting digital trip signal(s) from the IED); and
- 1x GTDO card (for outputting digital control signal(s) to the IED).

It is worth highlighting that these are generic models and that the scheme does not currently include the DCCB inductance that is required to provide the security of the protection system. The testing used the minimum inductance required by the DCCB to limit the fault current to prove the effectiveness of the protection (as implemented on the prototype IEDs) without introducing additional inductance.

6.2 APPLICABILITY OF MODEL DESCRIBED AND FURTHER MODEL UPDATES

The model in its current state is not suitable for testing the protection system against all the KPIs previously identified in WP4. Currently, it can be used to assess the performance of the IEDs against their specific KPIs. This allows for verification of the unit testing undertaken in WP4 and can give further confidence in the readiness of
these prototype devices. The further post fault functionality of the system facilitating the measurement of the KPIs is still under development and is expected to be available for the final demonstration.

Work is ongoing within WP9 to further investigate fully selective schemes and non-selective schemes using different combinations of HVDC technologies. Further confidence in the feasibility of the HVDC grid will be developed with further testing including: expansion of the test system (with a key focus being to introduce a mesh section), and inclusion of pole rebalancing and post-fault recovery sequences to allow assessment of overall system performance and impact.

6.3 INITIAL LESSONS LEARNT

Given hardware constraints for real-time computation large and complex power system simulation cases require that the electrical model be split across different hardware devices. Such a split (e.g. across CPU cores), and the associated communication, implies a time delay between the execution of the network solutions at either end of the interface. When splitting electrical systems, this delay is often modelled as a Bergeron stub line, which introduces a section of impedance for which the time for a signal to travel along exceeds one time step to allow time for communication of the signals between devices. A typical main time step for an RTDS solution is around 50 μs, however, this is insufficient resolution for the testing being undertaken. This required application of the ‘small-time step’ functionality to reduce the time step to around 4 μs. Converter and DC-side electrical elements are modelled exclusively in the small-time step. Mid-cable interface lines are specified such that the ratio of C to L matches that of the modelled cable. For a time step of 3.57 μs, and for the cable parameters of C34, this results in: C=0.16232 μF and L=78.562 μH, equivalent to 748.2 m of cable. Interface lines at circuit breaker locations are configured such that part of the additional inductance required at the circuit breaker is included in the interface. By modelling the interfaces in this manner, there is minimal impact on the transient response of the simulation model. The cables were modelled on GTFPGA units allowing for frequency-dependent cable models to be used in the small-time step. This approach was applied given that the accuracy was required for assessment of the fast-acting IEDs, but the computational burden of this complex model in a small-time step in real-time required the use of an external additional piece of hardware [18].

Although the developed model structure varies depending on the requirements of the particular test case (e.g. multivendor, different DCCB topologies, different IED configurations), a typical model uses two RTDS Novacor racks each with three to four small time step bridge boxes. When using functional units of one physical protection IED at different network locations (e.g. at different cable ends around the same bus) the analogue inputs to the IED are required to be sourced from different bridge boxes. Given that each GTA0 card can only communicate with one bridge box, and communicating signals to another bridge box would incur a delay and loss of resolution, each pair of IED functional units (positive and negative) is configured with a separate GTA0 card. For the two physical IEDs, each with three pairs of functional units, six GTA0 cards are utilised.

To deal with having two different IEDs, to minimise the amount of rewiring or additional modelling requirements we took the approach of mirroring the setup across two sets of RTDS hardware (with all the I/O on the same ports.
and channels etc) so that the physical set up could be fixed and only one model needed to be updated as we develop the test system.

Where simulated IEDs are required, they are executed in substep hierarchy boxes and interfaced to the small-time step elements through GTA0 and GTA1 cards. This is the only way to communicate between the small-time step and substep environments without significantly losing temporal resolution (e.g. 250 kSamples/s to 20 kSamples/s) and incurring a delay of one main time step (e.g. 50 μs).

IED testing is performed using automated repetitive scripts in order to evaluate the performance of the IED and the overall security and dependability of the protection system, e.g. as described in reference [21]. Scripts with differing objectives are used for different tests; testing the protection IED performance (e.g. for multivendor tests) requires the recording of the operation time, whereas the system-level testing requires scripts that evaluate KPIs to determine system-level performance.

Full lessons learnt will be evaluated at the end of the work package once all testing has been completed.
7 REFERENCES


[17] ABB, “Building for the future with opportunity to integrate renewable power generation and reinforcing the existing grid,” Caithness Moray HVDC Link, 2018; Available at: https://new.abb.com/systems/hvdc/references/caithness-moray-hvdc-link [Accessed 22 May 2019].


