HVDC Grid Protection System Demonstration – Interoperability, Primary and Back-up Protection in Non-Selective Strategies

Work package 9

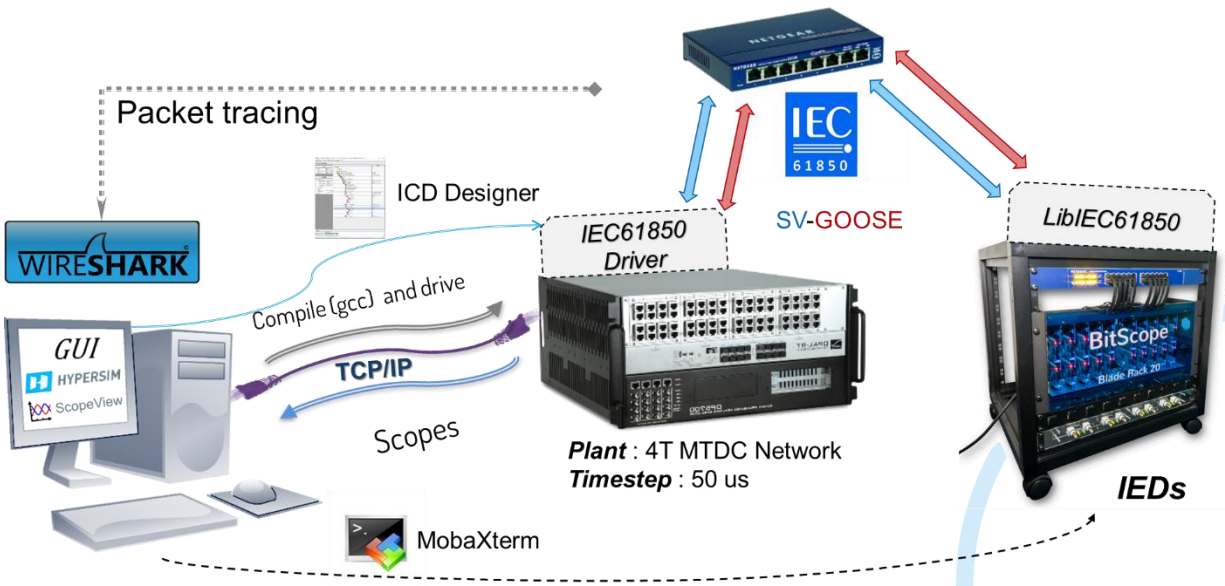
Work Package 9 represents the culmination and integration of a number of other work packages. A range of grid protection strategies and implementations have been taken from Work Package 4, where they have previously been verified using off-line simulation. The use of hardware in the loop techniques allows an opportunity to verify and increase the Technology Readiness Level (TRL) of the overall protection system.

Hardware in the loop (HIL) testing

In PROMOTioN WP9 Tasks 9.7 and 9.8, the HIL test setup is composed of a powerful workstation connected through TCP/IP to an Opal-RT OP5700 (real-time simulation target) to compile, drive and monitor the simulated plant. The plant is a four terminal HVDC network running at 50µs execution time step. The devices under test are prototyped IEDs arranged in a cluster, which can be accessed from the workstation through a terminal. The Opal-RT simulator manages the IEC61850 communication protocol through a proprietary driver which is configured using IED capability description files. On the other side, the IEDs can also communicate through an open source library for the IEC61850. A network sniffer such as Wireshark allows us to analyse the information flowing through this network.

Plant: real-time simulated HVDC network

Two systems have been tested. One is a four terminal asymmetrical monopole to test the CBS strategy. This HVDC network has 11 mechanical circuit breakers per pole, 4 DC cables and 4 Half-bridge Modular Multi-level Converters. On the other side there is a four terminal symmetrical monopole for the FBS strategy. It has 4 Full-bridge MMCs, no DC breakers on the converter side but 8 high speed switches per pole are required to protect the system. About a thousand network elements and up to 2000 control elements were used from the HYPERSIM library.



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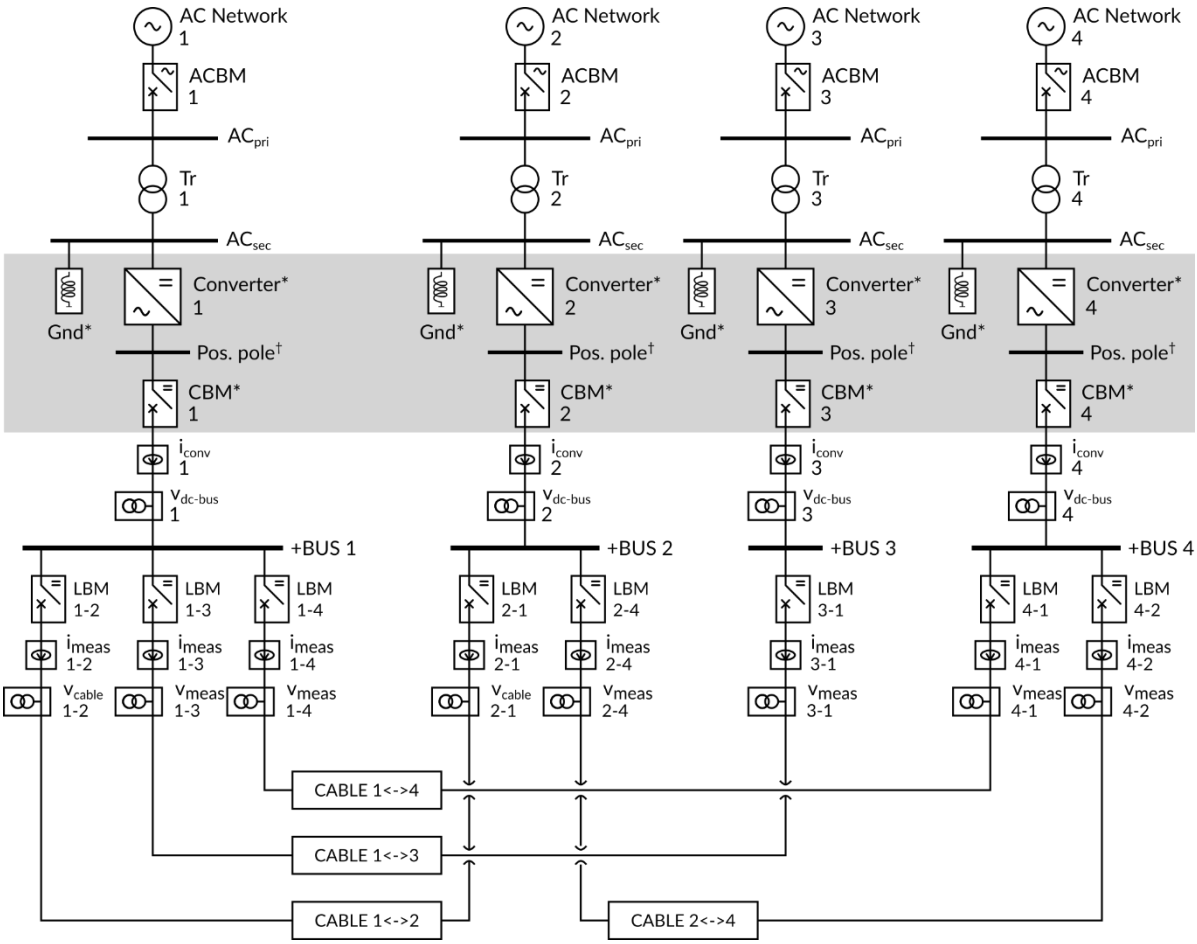
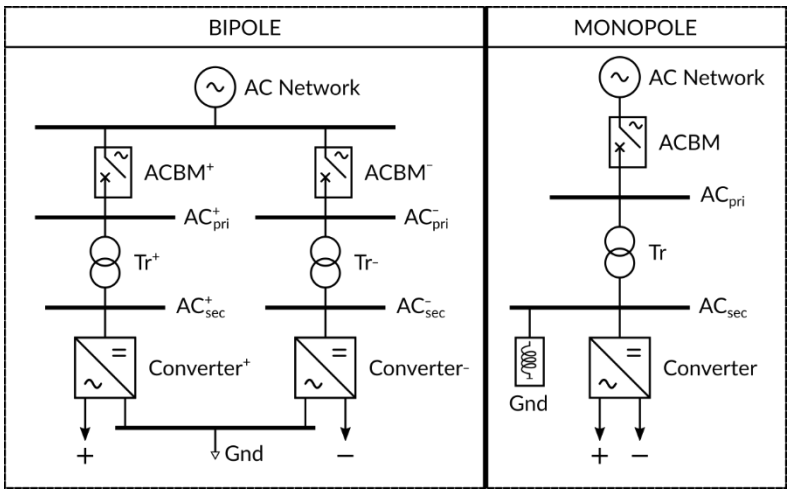
Small Impact Study Network Topology for PROMOTioN WP9 T9.7/T7.8



*For CBS the converter is HB-MMC in bipole, solidly grounded inside the converter (star-point reactor is absent), CBM is present. For FBS the converter is a FB-MMC in monopole, with star-point reactor for grounding, CBM is absent.
†Only one pole is illustrated for simplicity, the negative pole is symmetrical for both bipolar and monopolar cases:



One-line diagram of the four-terminal meshed HVDC system studied in WP9, proposed in [8].

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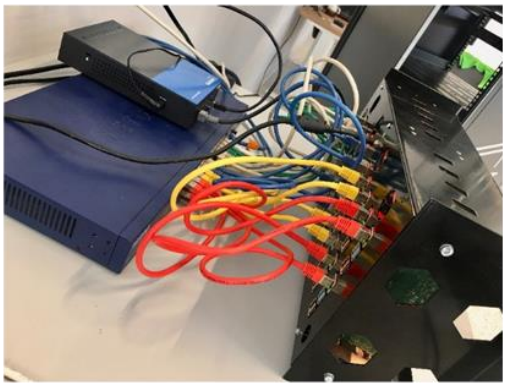
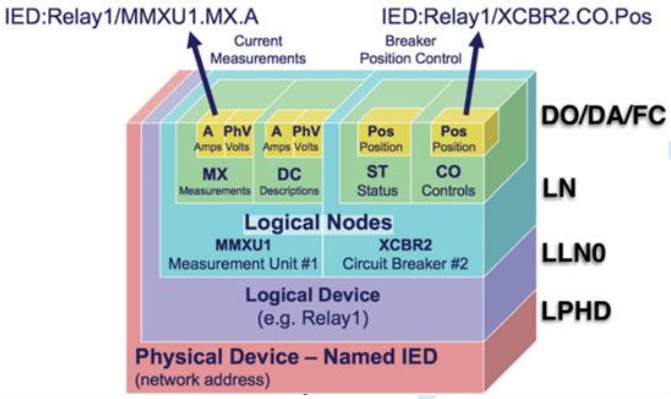
Device under test: Intelligent Electronic Device (IED)

On the other end of the HIL setup we find the Intelligent electronic device prototypes. We used Raspberry-pi to prototype the IEDs and C code programming language because of its flexibility and execution speed. Also with a well-structured coding approach we can ensure modularity and ease the repetition and evolution of the program to be implemented in different kinds of IEDs. One of them is the protection IED. The C code was written based on specifications provided in WP4 or in Simulink blocks like in the FBS case. First we tested the program in Hypersim, so that the code runs in synchrony with the simulation, before putting the program in the RPI based IED for HIL tests. Similarly, we developed Supervision IEDs. Supervision algorithms are generated from SUPREMICA, a software to design automation systems using discrete event systems theory.

Interface: IEC61850

The link between the simulation and the devices under test are made through IEC61850, which is a standard meant to create an interoperable environment in digital substations. It is also considered a fast Ethernet communication protocol, which allowed us to obtain satisfactory performances in terms of speed for the non-selective protection strategies. IEC61850 implementation is not straightforward: comprehension of the norm semantics is required as well as a clear definition of the functional architecture of the system.





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