PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

D5.6 Software and analysis report on candidate test-circuits and their effectiveness

PROMOTioN – Progress on Meshed HVDC Offshore Transmission Networks
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EXECUTIVE SUMMARY

The HVDC circuit breaker (HVDC CB) is one of the essential building blocks of the future MT-HVDC grids. In the last few years substantial R&D has been conducted on HVDC CBs as a result of which a few industrial concepts have been proposed. However, the practicality of these concepts still remains a fact to be proven. Especially the lack of sufficient experience of MT-HVDC networks with DC side protection poses a significant challenge to accurately characterize the expected fault conditions to which these breakers are exposed. Nevertheless, simulation investigations of multi-terminal HVDC networks indicate that an HVDC CB must be designed so that it is able to absorb not only the energy stored in the system inductance but also the energy contributed by sources (converter stations) during the interruption process. Hence, HVDC CB test methods must ensure to stress the breakers with sufficient energy equivalent to practical HVDC grids. A major challenge is that the requirements of an HVDC CB are not yet standardized let alone the standardized method to test these devices. The primary reason for this is the absence of well-defined and agreed upon procedures since the requirements are dependent on the type of converter, design and topology of HVDC networks, protection philosophy, etc.

Throughout the recent development of HVDC switchgear, several types of test circuits and methods have been proposed and discussed in the technical literature. The choice of test circuit varies based on the type of test object, the ratings to be verified and the functionality to be demonstrated. Due to the relative immaturity of the field of HVDC circuit breakers, no standards prescribing test methods and clear test requirements exist. In order to enable standardised testing of HVDC circuit breakers, a comparison of available test circuits and methods, based on their ability to adequately, safely, practically and economically verify ratings and functionality is required to provide future owners with insight into the relevant choices regarding testing.

Based on the stresses which are exerted onto HVDC circuit breakers during DC fault current breaking operations, requirements for test circuits in which DC short-circuit current breaking capability is to be verified, have been presented. Four hypothetical test circuits based on a controlled rectifier, a charged capacitor, a charged inductor, and an AC short-circuit generator operated at reduced frequency, have been qualitatively discussed and compared to the test circuit requirements.

It is concluded that only a controlled rectifier circuit could directly synthesize all necessary stresses but is likely to be prohibitively expensive and complex at the required power ratings and functionality. Depending on the charging circuit, the charged reactor method may prove to be unsuitable for testing hybrid HVDC circuit breakers. Both the charged capacitor and AC short-circuit generators are capable of producing a suitable DC short-circuit test current. However, AC short-circuit generators offer the possibility to deliver high energy stresses, which may be unpractical to achieve using a charged capacitor circuit, due to the large required capacitance. The latter is especially relevant for testing HVDC circuit breakers with long breaker operation times.

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It is shown that AC short-circuit generators operated at reduced frequency offer flexible control of the rate of rise of test current, and the amount of energy delivered to the HVDC circuit breaker by carefully chosing the generator frequency, the test circuit impedance, the generator source voltage magnitude, and the making angle. The AC characteristic implies that an inherent limitation exists on testing HVDC circuit breakers with long breaker operation times, as the entire fault neutralisation time must be less than the longest possible half wave period of the applied test current.

A method to protect the test object and the test circuit from damage in case the HVDC circuit breaker fails to operate correctly, has been presented. A high-speed level-detector triggered spark-gap, combined with an auxiliary breaker can by-pass the prospective test current and isolate the test object from the test source.

Apart from the controlled rectifier circuit, none of the discussed test sources is capable of supplying DC voltage stress after interruption without additional measures. In case of AC short circuit generators, it is shown that for HVDC circuit breakers with active current injection, it is possible to achieve DC voltage stress by trapping charge in the injection capacitor, or otherwise by injecting a DC voltage stress from an external DC voltage source.

Finally, it is recognized that no practical test circuit can supply the required stresses to directly test EHV full-pole HVDC circuit breakers. Some suggestions for verififying performance of a modular part of a breaker i.e. unit testing, or separately verifying different functionalities i.e. multi-part testing and realising different stresses from different test sources i.e. synthetic testing are discussed.

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CONTENT

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NOMENCLATURE

ABBREVIATION	EXPLANATION
AC	Alternating Current
CB	Circuit Breaker
D5.3	Deliverable 5.3 (PROMOTioN deliverable)
HVDC CB	Direct Current Circuit Breaker
DCL	DC Current Limiting Reactor
FB	Full Bridge
HB	Half Bridge
HVAC	High voltage AC
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
ITIV	Initial Transient Interruption Voltage
LCC	Line Commutated Converter
MMC	Modular Multi-Level Converter
MTDC	Multi-Terminal HVDC
NLC	Nearest Level Control
OHL	Overhead Line
PCC	Point of Common Coupling
TIV	Transient Interruption Voltage
VSC	Voltage Sourced Converter
WP	Work Package
LCS	Load commutation switch
UFD	Ultra-fast disconnector
RCB	Residual current breaker
MOSA	Metal oxide surge arrestor

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1 INTRODUCTION

The HVDC circuit breaker (HVDC CB) is one of the essential building blocks of the future MT-HVDC grids [1]. In the last few years substantial R&D has been conducted on HVDC CBs as a result of which a few industrial concepts have been proposed. However, the practicality of these concepts still remains a fact to be proven. Especially the lack of sufficient experience of MT-HVDC networks with DC side protection poses a significant challenge to accurately characterize the expected fault conditions to which these breakers are exposed. So far only two multi-terminal systems based on voltage source converter (VSC) HVDC grids, with AC side protection, are in operation [2], [3]. Nevertheless, simulation investigations of multi-terminal HVDC networks indicate that an HVDC CB must be designed so that it is able to absorb not only the energy stored in the system inductance but also the energy contributed by sources (converter stations) during the interruption process [4], [5]. Hence, the HVDC CB test methods must ensure to stress the breakers with sufficient energy equivalent to the practical HVDC grids. A major challenge is that the requirements of an HVDC CB are not yet standardized let alone the standardized method to test these devices. The primary reason for this is the absence of well-defined and agreed upon procedures since the requirements are dependent on the type of converter, design and topology of HVDC networks, protection philosophy, etc.

Apart from few test circuits (with limited power) at various research institutes/companies, there is no known independent HVDC CB test facility with proper and sufficient test set up. In fact, it makes no sense to expect such a test facility in the absence of commercially mature HVDC CB products as well as of standardized test procedures and requirements. In this document an overview and analysis of possible test circuits for testing HVDC CBs is provided. In particular, the use of AC short-circuit generators used to test HVDC CBs has been investigated.

1.1 MOTIVATION

Throughout the development of HVDC switchgear, several types of test circuits and methods have been proposed and discussed in the technical literature. The choice of test circuit varies based on the type of test object, the ratings to be verified and the functionality to be demonstrated. Due to the relative immaturity of the field of HVDC CBs, no standards prescribing test methods and clear test requirements exist. In order to enable standardised testing of HVDC CBs, a comparison of available test circuits and methods, based on their ability to adequately, safely, practically and economically verify ratings and functionality is required to provide future owners with insight into the relevant choices regarding testing.

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1.2 PURPOSE

This deliverable aims to provide an overview and comparison of the various test circuits and their limitations, which can be used to realise the DC current breaking test requirements and procedures discussed in D5.4 and D5.5, respectively. The test circuits' performance is compared to the test requirements. Methods to set-up and tune the test circuits' parameters are presented. Approaches such as multi-part testing, unit (modular) testing and synthetic testing, which seek to maximally test functionality and verify ratings within the test circuit's limitations, will be discussed.

A test circuit designed to test all types of HVDC CBs can ideally reproduce all desired stresses in terms of current, voltage and energy in one test. Given the lack of mature products and standards defining test requirements, testing of HVDC CBs can be aimed at one of the following objectives.

Technology qualification – testing according to the maximum capabilities of the technology. These capabilities are stated by the manufacturer and are determined by the maximum ratings of the subcomponents of the HVDC CB.

Project qualification – testing according to the maximum stresses experienced by an HVDC CB in a specific application in a DC grid. These stresses are stated by the project developer (e.g. TSO) and are determined by system studies (e.g. D5.3).

Development testing – testing of an HVDC CB to study internal phenomena or verify basic capabilities. The test stresses are to be determined according to the purpose of the test.

It should also be clear that there is a distinction between testing the test circuit and testing the HVDC CB. In the absence of an actual project, the PROMOTioN tests are somewhere between development testing and technology qualification. The test circuit is not fully developed and the HVDC CB has not been realized yet at full rating thus specific tests have to be designed to further develop and verify both. In this document it is assumed that both the test circuits and HVDC CBs can be considered ready for testing.

One of the objectives of work package 5 is the development of guidelines towards technology qualification and project qualification. The tests carried out in deliverable 5.7 aim to verify the realization of a test circuit installation. The testing of the HVDC CB performance (technology qualification testing) will then be pursued in work package 10.

1.3 DOCUMENT OVERVIEW

The remainder of the document is organized as follows. In Chapter 2 a background for HVDC CB test circuit requirements as derived from D5.3 is discussed. The candidate test circuits, along with the proposed test methods, are discussed and compared based on the test circuit requirements in Chapter 3. In this chapter,

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comparison of various test methods by simulation is discussed. Chapter 4 provides insight into how AC short-circuit generator based circuit parameters can be adjusted to achieve the required stresses. Furthermore, methods to protect the test object and test circuit from damage in case of failure, as well as methods to provide dielectric stress after current suppression are discussed. Chapter 5 discussed methods such as unit testing, multi-part testing and synthetic testing, which can be used when the stresses required to verify ratings and functionality of a full-pole HVDC CB cannot be reproduced by one single test source. Chapter 6 provides conclusions based on the results of analysis in the document.

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2 REQUIREMENTS FOR TEST CIRCUITS

In this report the terminology proposed in TB 683: Technical requirements and specifications of state-of-the-art DC from CIGRÉ JWG A3-B4:34 is used. An ideal HVDC circuit breaker (HVDC CB) test circuit can economically verify all functionality and ratings of an HVDC CB in one single continuous test. In practise, to reflect the limitations of economical test circuits and the different types of stresses and operational modes that a generic power system component encounters during service life, the verification of functionality and ratings is typically split into several separate tests which all require separate specialised test circuits. This chapter discusses the requirements for a test circuit for verifying the DC current interruption performance of HVDC CBs by qualitatively discussing the stresses an HVDC CB is subjected to during fault clearing and subsequently the resulting requirements for HVDC CB test circuits.

2.1 STRESSES ON HVDC CIRCUIT BREAKERS

In deliverable 5.3 the stresses on two types (hybrid and mechanical with active current injection) of HVDC CBs during DC fault current interruption were studied, in terms of required current, energy, and voltage capability. There are a large number of factors which affect these stresses, some which are:

- Rated system voltage
- Converter configuration – monopole/bi-pole configuration
- Fault type – pole-to-pole; pole-to-ground (for monopole and/or bi-pole)
- System size – number of converters, number dc links connected at dc bus (level of meshing)
- Fault location – distance of fault from converter stations
- Line type – Cable only or over-head line
- Size of DC current limiting reactors
    - HVDC CB breaker operating time
    - HVDC CB rated short-circuit breaking capability
- Strength of neighbouring AC network
- Additional functionality
    - Reclosing
    - Soft openening and closing
    - Current limiting
    - Pro-active breaking
    - Self protection
- If converters are blocked or not during current interruption, etc.

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Nevertheless, important generic conclusions can be deduced from the simulation results of deliverable 5.3. Before going into the details of these deductions, the assumptions used in the simulation are summarized in this section.

In Deliverable 5.3, simulations are performed considering the reported capabilities HVDC CBs at the moment of writing the document. It was assumed that relays can detect and trigger HVDC CBs within 2 ms of fault occurrence, based on local detection. HVDC CB breaker operation times are set based on the values provided by the respective manufacturers. For hybrid HVDC CBs, a breaker operation time of 2 ms is assumed while, for active current injection HVDC CBs a breaker operation time of 8 ms is assumed. Next, the magnitude of the DC current limiting reactor is determined in such a way that, primarily at the end of the fault neutralization time, the peak value of the interrupted current does not exceed the rated short circuit breaking current of the corresponding HVDC CB. As in the case of the breaker operation time, the values of the rated short circuit breaking current of the HVDC CBs is provided by the respective manufacturers. Hence, the rated short-circuit breaking current of both the hybrid HVDC CB as well as the mechanical HVDC CB with active current injection is assumed to be 16 kA.

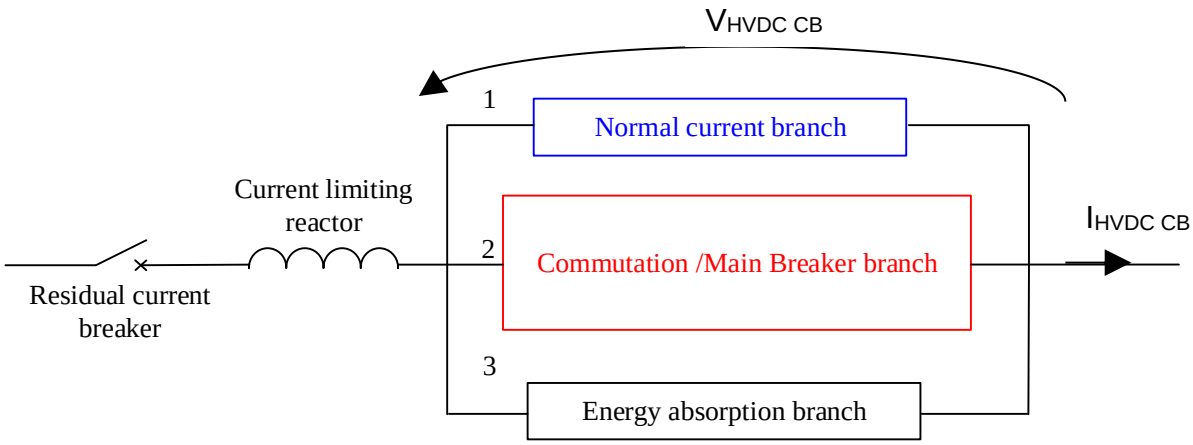

Figure 2-1: Generic model of an HVDC CB

Figure 2-2 provides important conclusions based on simulation results of D5.3. The top diagram shows current through and voltage across the terminals of an HVDC CB, as indicated by $I_{HVDC\ CB}$ and $V_{HVDC\ CB}$, respectively, in the generic HVDC CB schematic shown in Figure 2-1. The middle diagram shows the energy absorbed by the HVDC CB energy absorption branch during a breaking operation. The bottom diagram shows the converter DC voltage during current interruption by HVDC CBs under two conditions. The first is the voltage when a converter is blocked during current interruption, shown by the (solid blue curve), and the second is the voltage when the converter remains unblocked during a fault current interruption (dashed black curve). The latter is a condition that happens when a converter remains in continuous operation throughout the fault clearing process. The two different converter conditions will induce two different stresses on an HVDC CB, especially from the energy dissipation perspective.

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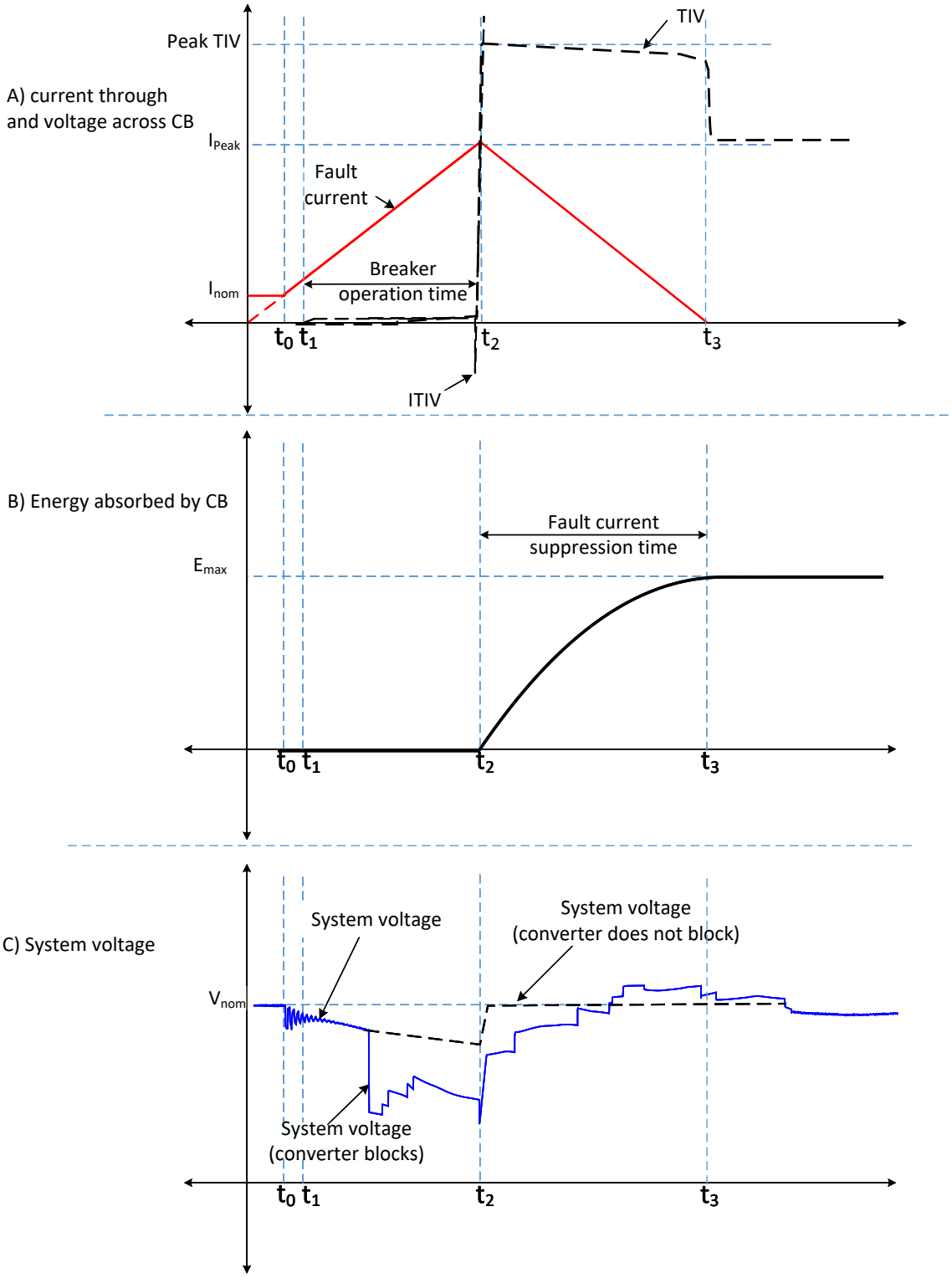

Figure 2-2: Stresses on HVDC CB during DC current interruption A) generic voltage (dashed black) and current (red solid) waveforms B) Energy absorption during fault current suppression C) system voltage when a converter blocks (solid blue) and when a converter does not block (dashed)

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Two approaches are considered assuming two different converter conditions during HVDC CB operation. The first is when a converter remain unblocked during fault clearing operation by HVDC CB. This can be represented by a DC voltage source. The other condition is when a converter blocks under DC fault and the HVDC CB clears the fault. In this case the converter voltage changes significantly, resulting in different current interruption and energy absorption.

In Figure 2-2, four different periods can be discerned in which different stresses on the HVDC CB can be defined:

1. **Normal operation** - Prior to t_0 corresponds to normal operation. The load current can vary bidirectionally between 0 A and the HVDC CB's rated normal current. This is typically 2-3 kA. As the HVDC CB operates at its rated normal current (or short-time withstand current), it will heat up due to dissipation of losses. During normal operation, the rated line voltage will exist across the support structure. In some HVDC CB designs this voltage is required to power internal circuitry such as for example the injection capacitor.

2. **Current commutation** - The moment a fault occurs is represented by t_0 and the time from t_0–t_1 represents relay time (detection + selection). The time from t_1–t_2 represents the breaker operation time as shown in the top graph of Figure 2-2. During this time, the current through the HVDC CB rises steadily, limited by the current limiting inductor and the network impedance. It must be noted that this is the time from trip order until the breaker achieves the dielectric withstand capability corresponding to the transient interruption voltage (TIV). This time is independent from the magnitude of the interrupted current but is technology specific as previously explained. Meanwhile (during the breaker operation time), the short-circuit current should not exceed the rated short circuit breaking current of the HVDC CB.

   Due to the impact of travelling waves, which depend on the distance between the location of the fault and the HVDC CB, and the converter blocking, the fault current may not be rising linearly to the peak interruption value. For testing, however, it is important to produce a range of current magnitudes (duties) up to the rated short circuit breaking current of the HVDC CB within the breaker operation time. Thus, depending on the magnitude of current at the moment that the HVDC CB receives a trip order, the average rate of rise of current to be produced by a test circuit can be calculated as follows,

$$\frac{di}{dt_{avg}} = \frac{I_{peak} - I_0}{\Delta t} \qquad (1)$$

   Where, I_{peak} is the maximum interruption capability of the HVDC CB, I_0 is the magnitude of current at the moment of trip order and $\Delta t = t_2 - t_1$ is the breaker operation time. For example, for a hybrid

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HVDC CB with breaker operation time of 2 ms, relay time of 2 ms and a rated short circuit breaking current of 16 kA this is 4 kA / ms. For a mechanical HVDC CB this is 1,6 kA / ms.

3. **Energy dissipation** - Between t_2 and t_3 the fault current is flowing through the energy dissipation branch. This is typically a metal oxide surge arrestor (MOSA) with a kneepoint voltage chosen as approximately 1.5 times the rated voltage. The HVDC CB exerts a countervoltage to supress the current to zero. During this period both voltage and current stresses are applied to the HVDC CB, resulting in an overall energy stress.

   In D5.3, an approach is introduced where the energy absorbed by the HVDC CB is split into two parts. The first is the magnetic energy stored in the DC current limiting reactor in series with the HVDC CB of the faulted line at the beginning of fault current suppression (t_2 in Figure 2-2). Since the current through the HVDC CB on a faulted line should be brought to zero, the entire energy stored in this reactor at peak current (i.e. $\frac{1}{2}LI_p^2$) must be absorbed. The second, while the HVDC CB is absorbing the magnetic energy stored in the inductance, there is electrical energy contributed by the rest of the system which depends on the bus voltage during the current suppression period. To calculate the energy from each of the sources that are directly or indirectly connected to the faulted line is rather not straight forward since a lot of factors should be taken into account. One way to compute this is in terms electrical energy pushed from the DC bus into the fault (a function of voltage and current) during the fault current suppression is to indicate fault current suppression time). However, from Figure 2-2 it can be seen that both voltage and current are time dependent variables and depends whether a converter blocks or not. By making reasonable assumption regarding system voltage, the maximum energy that an HVDC CB has to absorb can be calculated as follows (in reference to Figure 2-2).

$$E = \frac{1}{2}LI^2 + \int_{t_2}^{t_3} V_{dc,bus} i_{fault} dt \qquad (2)$$

   Where, L is the dc current limiting reactor, I_{peak} is the peak value of the interrupted current, $V_{dc,bus}$ is the converter dc voltage during fault current suppression time, i_{fault} is the fault current flowing through the HVDC CB.

   In deliverable 5.3, different energy absorption requirements were obtained from the simulation results. In one of the simulation sets the converters do not block during fault. Under unblocked converter condition the energy up to 35 MJ is absorbed. In the other simulation sets, the converters are blocked during a fault, making the dc bus voltage equal to uncontrolled rectifier output. As described in deliverable 5.1 (also in Figure 2-2), this voltage is dependent on the magnitude of current fed through the rectifier to the dc fault. The higher the rectifier current the lower the converter dc bus voltage due to significant voltage drop on the AC side impedance. However, as the current is being suppressed this voltage rises to a no-load rectifier value. In this case the energy up to 25 MJ was absorbed by the HVDC CB.

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Hence it is not sufficient to just produce DC test current for testing an HVDC CB. A test circuit also needs to provide proper energy stress to the HVDC CB. Depending on the type of test circuit, there might be additional energy coming from source (proportional to the source voltage) besides the energy stored in the reactor required to limit the rate of rise of current. Therefore, if the test circuit has a driving (source) voltage during the interruption process, the proper magnitude of the voltage should be determined to meet the energy requirement.

The supply of energy is not trivial. For an HVDC CB with rated short-circuit breaking current of 16 kA, a rated voltage of 80 kV and a TIV of 1.5 pu, the momentary power required at the start of current suppression is 16 kA * 1.5 * 80 kV = 1.92 GW.
During the current suppression period, the test circuit must withstand the TIV imposed by the HVDC CB. This is typically 1.5 times it rated voltage. For a single unit, this typically results in about 1.5 * 80 kV = 120 kV, although full pole tests with a TIV of 800 kV have been reported [6].

4. **Dielectric voltage withstand** – from t_4 onwards, the current has been suppressed to zero, and the recovered line voltage appears across the breaker until the residual current breaker (RCB) opens. Depending on the HVDC CB type, this is a DC voltage or it can in some cases be oscillatory in nature.

Note: There is a voltage rise time after breaker operation time where the voltage across HVDC CB rises to the maximum TIV. This time is not shown in Figure 2-2 for simplicity.

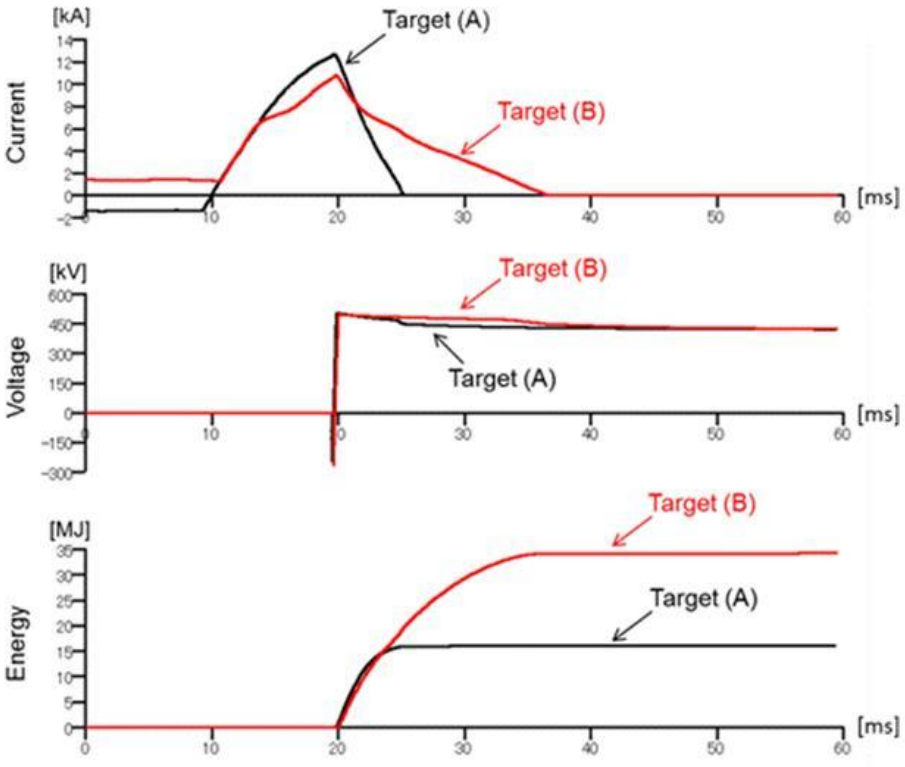

Figure 2-3: Test cases from Deliverable 5.3: (a) higher current duty; (b) higher energy duty

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It is clear from the simulation results of deliverable 5.3 that, in order to successfully interrupt the dc fault current, the HVDC CBs should be able to absorb the inductive energy in the system. However, the quantification of the inductive energy in the system is rather difficult especially in meshed networks since there are a lot of contributions from different sources. It is shown in the simulation results of D5.3 that the HVDC CB stresses can be classed into two categories, broadly: high energy and high current. These are illustrated in Figure 2-3. One is a severe case in terms of interruption current (target A), which corresponds to the duty for an HVDC CB located close to a of fault point and the other is a severe case in terms of dissipation energy (target B), which corresponds to the duty for HVDC CB located near the remote side of fault point.

2.2 HVDC SHORT-CIRCUIT CURRENT BREAKING TEST CIRCUIT REQUIREMENTS

AN HVDC CB should be designed to have sufficiently high ratings to withstand the current, voltage and energy stresses which it encounteres during service life in a practical HVDC system, which are illustrated in Figure 2-2. A test circuit for HVDC CB short-circuit current breaking testing should reproduce the stresses that are relevant for current breaking operations up to the rated values including a test factor where applicable. Furthermore, the test circuit must be able to withstand any stresses such as TIV which are produces and determined by the HVDC CB itself. For a test circuit to provide adequate stresses to HVDC CBs, it should fulfil the following requirements based on the characteristic of the four different periods discussed in the previous section:

1. Pre-condition the HVDC CB to mimic worst case normal service conditions, and ensure internal systems are powered up and charged
2. Produce a test current which rises somewhat linearly from anywhere up to the rated load (or short-time withstand current) to the intended test duty within the breaker operation time. It is shown in [7] that the most difficult interruption may not necessarily be the highest current. Thus, test circuits have to provide a wide range of quasi–DC currents, from the rated load current (or less) to the rated short circuit breaker current of an HVDC CB. The test circuit must be able to apply the test current bidirectionally.
3. Supply rated energy to the HVDC CB and withstand TIV
4. Supply rated dielectric stress immediately after current suppression
5. Avoid damage to the HVDC CB and test circuit in case of failure - if the prospective short-circuit current from a test circuit can exceed the HVDC CB's rated short-circuit breaking current, it is necessary to limit the damage to the HVDC CB as well as the test installation in case of a failure to clear. Methods to avoid potential damage to the test breaker as well as the test installation are discussed in Chapter 4
6. Be implementable / economical – the test circuit must be technically feasible, practical and economical

The above requirements should be fulfilled whilst respecting practical breaker operation times which are currently assumed to be in the range of 2 – 8 ms.

These stresses do not have to be supplied by the same source, in which case it is referred to as a synthetic test, which is further explained in chapter 4. The modular construction of HVDC CBs may under certain conditions allow the verification of functionality and/or ratings by testing a reduced number of modules. This is referred to

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as modular testing and discussed in chapter 5. Furthermore, in some cases, different functionalities of an HVDC CB can be tested in separate tests with different test circuits, in which it is referred to as multi-part testing which is further explained in chapter 5.

Within this report a number of potential high power (quasi-) DC cources are evaluated on their ability to meet the above requirements. The discussion will focus in the technical requirements 1-5 and briefly touch upon the practical and economical aspects.

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3 TEST CIRCUITS

In this section, various possible test circuits which can potentially emulate a suitable (quasi-) DC current current for use in DC fault current breaking tests of HVDC CBs are described and qualitatively compared. Most HVDC CBs proposed by manufacturers consist of series connected modules. For the comparison an HVDC CB module rated at 80 kV is assumed, based on the modular testing approach which is further described in chapter 5.4. As the HVDC CB demonstration in Work Package 10 will be performed using an AC short-circuit generator based test circuit, further details regarding the practical implementation of an AC short-circuit generator running at reduced frequency are given in chapter 4.

3.1 CONTROLLED RECTIFIER CIRCUIT

High-power rectifier circuits in combination with high-voltage capacitors can be used for testing HVDC CBs. Assuming sufficient available power for testing and properly dimensioned circuit components, this test circuit can provide the necessary stresses required for testing HVDC CBs. Through the control of the AC side impedance, the transformer turns ratios and the DC side impedances, the desired current, voltage and energy can in theory be produced. There is a wide variety of rectifier circuits in use today, designed either for high current or high voltage testing; however, there is none as of yet designed for high power applications.

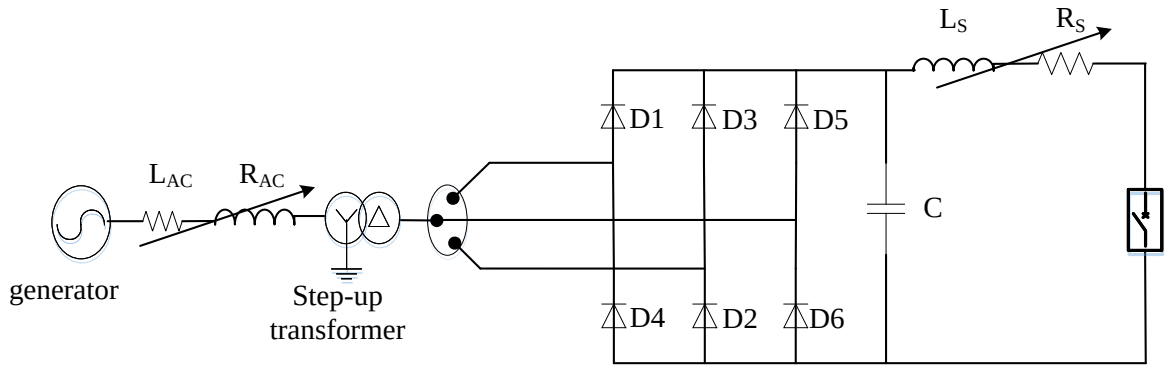

Figure 3-1: High voltage rectifier circuit for HVDC CB testing

At a low voltage, a rectifier circuit can be used for tests other than current interruption tests; for example, temperature rise tests, current withstand tests, etc. Similarly, they can be useful in the pre-conditioning of test objects such as the pre-heating of semi-conductor switches.

A synthetic test circuit based on parallel current injection has been used in laboratory experiments mainly to test load current interruption capability of HVDC CBs [8]. A prospective current up to 4.3 kA is produced by a back-

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to-back 12 pulse rectifier connected to the grid. In order to reduce the impact on the grid. A controlled DC chopper based test circuit is proposed in [9].

3.2 DISCHARGE OF HIGH-VOLTAGE CHARGED CAPACITOR METHOD

The oscillatory inductor-capacitor (L-C) test method has been demonstrated with different frequency ranges [10], [11]. The inductor-capacitor circuit is shown in Figure 3-2. Initially, the capacitor is pre-charged to a pre-determined voltage. For simplicity, the charging circuit is not shown in Figure 3-2, but could for example be a diode rectifier bridge. The capacitor is discharged through the inductor in series with the test object (TO) by closing the making switch (MS). In a practical circuit, stray inductance and resistance naturally exist. However, additional inductance is added for two purposes:

1. To limit the rate of rise of current – so that peak current is not reached before the HVDC CB opens
2. To transfer energy from the charged capacitor to the HVDC CB during current interruption.

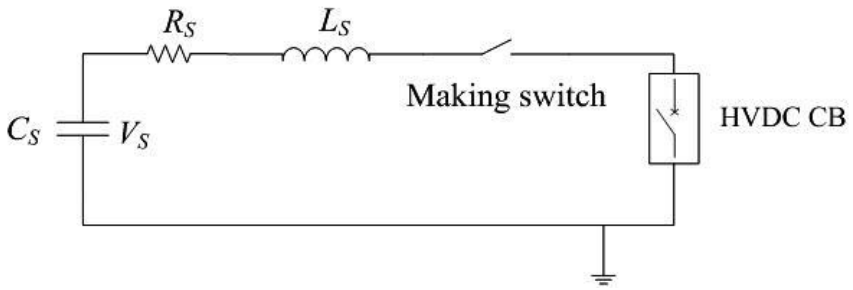

Figure 3-2: Test circuit supplied by a charged capacitor

Theoretically, with appropriate choices of charging voltage (V_s), circuit resistance (R_s) and inductance (L_s) the circuit can be tuned to replicate the DC fault current interruption reference waveforms. The main challenge of using this circuit is that, for practical values of C_S and L_S, the voltage across the capacitor decays quite fast, as shown by the dark blue line in Figure 3-3. This makes the interruption process less onerous for the HVDC CB since the difference between the counter voltage produced by the HVDC CB and the voltage across the capacitor banks is large during the current suppression period. Thus, assuming negligible resistance in the circuit, the rate of decay of current during the suppression period becomes high leading to very a shorter than realistic current suppression time as shown by the following equation

$$\frac{di}{dt_{suppression}} = \frac{V_C - V_{HVDC\ CB}}{L_s} \tag{3}$$

Where V_C is the voltage across capacitor during energy dissipation phase, $V_{HVDC\ CB}$ is the transient interruption voltage (TIV) generated by the HVDC CB during current interruption.

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In particular, for an HVDC CB having longer breaker operation time, this method becomes even more challenging for high-current interruption tests. In this case the L-C circuit should have sufficiently low frequency and produce a current higher than the desired peak interruption current within the breaker operation time so as to ensure current interruption by the HVDC CB before natural current zero. In other words, the capacitor and the inductor should be dimensioned so that the breaker operation time Δt is less (with some margin) than quarter a period of the L-C oscillation period, i.e.

$$\Delta t < \frac{T}{4} = \frac{1}{4f} \tag{4}$$

Where *f* is the resonant frequency of L-C circuit.

Another requirement is that the prospective current from the L-C circuit should rise to a value higher than the rated short-circuit breaking current of the test HVDC CB, as shown by the pink curve in Figure 3-3. [12]. All the energy that is dissipated in the HVDC CB must be stored in the capacitor at the beginning of the test since no additional energy is contributed during the test from an external source. Storing enough energy (in the order of several MJ) requires a large capacitance charged to a high voltage. For example, a 2 mF capacitor is required to test a test object having 8 ms of breaker operation time and rated voltage of 80 kV (see Table 3-1). In this case, the capacitor needs to be charged to 80 kV to supply 6 MJ of energy to the test object. Practically, the capacitor is not a single device, and will consist of a bank of smaller elements to provide the required energy, meaning it is challenging to ensure the stresses on each are relatively balanced.

Table 3-1 shows example test circuit parameters using charged capacitor method for testing an HVDC CB with breaker operation time of 8 ms, rated voltage of 80 kV and rated short-circuit breaking current of 16 kA.

Table 3-1: Example test circuit parameter using charged capacitor method

Capacitor (μF)	Inductor (mH)	Voltage (kV)	Energy (MJ)	Peak interruption current (kA)	Breaker operation time (ms)
2000	30	80	6	16	8

Note that it is not only the capacitor which should be designed for high voltage but also the inductor should be designed to withstand a voltage up to the maximum TIV of the HVDC CB.

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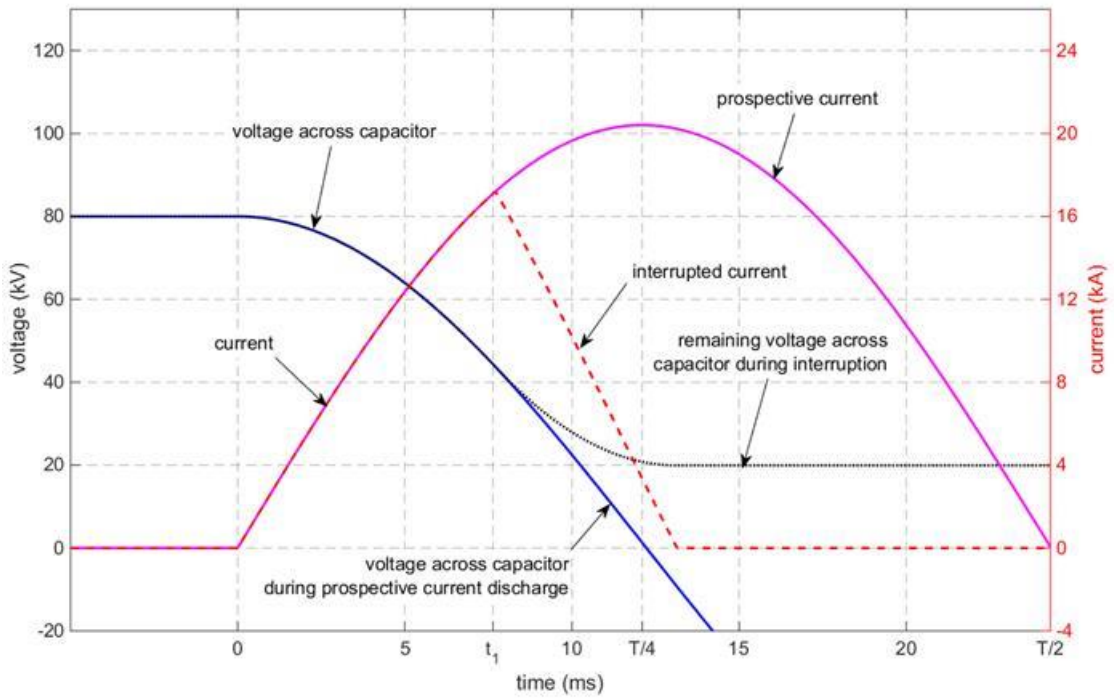

Figure 3-3: simulation result for charged capacitor test circuit for 80 kV, 16 kA current interruption

There are other ways to increase the stresses using the charged capacitor method:

1. Use a very large capacitor charged to a specified voltage up to the rated voltage of the test HVDC CB
2. Use of combination of two or more L-C circuits

In order to address the challenge of losing significant charge across the capacitor at the beginning of fault current suppression period of the interruption process, it can be charged to a higher voltage than to the calculated value shown in the Table 3-1. However, this comes at the cost of additional capacitors (to be added in series for higher voltage rating and additionally also in parallel to keep the desired capacitance value) and higher required insulation strength of the test installation.

In order to test the performance of IGBT based hybrid HVDC CBs, charged capacitor banks combined with current limiting reactors are used [13], [14]. Separate tests were carried out on internal components prior to the overall performance test. In order to test the overall performance quite large capacitor banks charged to a higher voltage are used to test a single unit of the HVDC CB. Another test circuit composed of the superposition of two L-C circuits, one with low frequency (32 Hz) and the other with a higher frequency (66 Hz) [12], [15] were also used to test a thyristor based hybrid HVDC CB. In this case the low frequency L-C circuit represents the load current under normal condition while the high frequency L-C circuit mimics the superimposed rising DC short circuit current.

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3.3 DISCHARGE OF HIGH-CURRENT CHARGED REACTOR METHOD

By discharging the magnetic energy stored in a current-charged reactor through a test object it is possible to produce quasi-DC current for the test duration [16]. There are several possible implementations of charged reactor test circuits. Figure 3-4 shows an example of a test circuit based on the charged reactor method where an AC source is used to charge the reactor. The reactor L_{AC} represents the generator side impedance. A charged capacitor or a low voltage rectifier can also be used as a charging source. In this case the entire energy stored in the reactor is absorbed by the breaker. This is the advantage of this test circuit compared to a charged capacitor or a reduced frequency AC generator based test circuit, which is explained in the next section, where some of the energy can be absorbed by the source as a result of polarity reversal in case the breaker operation time is too long.

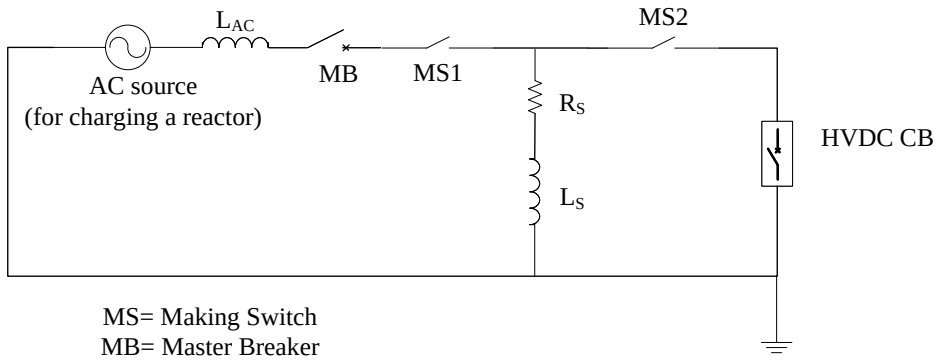

Figure 3-4: Test circuit supplied by a charged reactor

Three reactors across each of the three phases can be used for increased quasi-DC current. This can increase the quasi-DC current by a factor of three (assuming reactors having high quality factors), however, this increases the complication of the circuit by the same factor [16]. A charged reactor method for a single phase is described in this section using Figure 3-4 and Figure 3-5. Referring to Figure 3-4 the making switches (MS1 and MS2) are initially open while the master breaker (MB, basically an AC circuit breaker) is initially closed. By closing the MS1 the reactor (L_s) is charged using the AC generator. When the current reaches its crest value (at about 5 ms in Figure 3-5), the making switch 2 (MS2) is closed and, simultaneously, the master breaker is opened. The master breaker arc voltage commutates the current of the charged reactor (L_s) into the test object and interrupts the current from the AC generator at the next natural zero by the MB.

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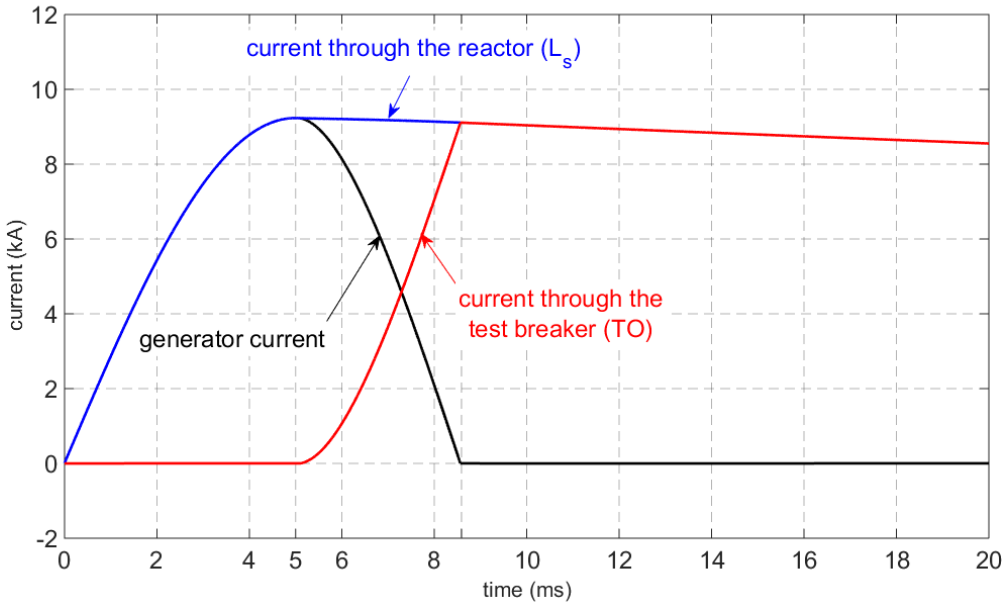

Figure 3-5: Quasi-DC current from charged reactor discharge

The making switch 2 (MS2) and the master breaker (MB) (required for isolation of the charging source), see Figure 3-4, should be interlocked (synchronized) in such a way that the MB opens and the making switch closes when the current is at the peak (at 5 ms). However, the exact timing of opening MB and closing the MS is practically challenging since these devices are mechanical.

In theory, a low voltage DC source can also be used for charging the reactor and the interruption process can be started once the current reaches steady state value. However, the components of the dc source should be dimensioned for the TIV generated by the HVDC CB.

This test circuit can produce pseudo-DC current required for the test duration since the test takes only a few milliseconds (see Figure 3-5). However, this circuit lacks an intrinsic voltage source during the interruption process as a result of which current is suppressed rapidly. Thus, a large reactor should be used to test in order to provide sufficient energy. Moreover, the current decay in such a circuit depends significantly on the circuit resistance and hence requires quite large reactors with a very high quality factor. Particularly, for HVDC CBs having relatively longer breaker operation time, the decay in current poses a challenge.

The interruption by the test HVDC CB is not on the rising edge of the current but rather at a steady state value. This may be suitable to test fault current interruption of HVDC CB technologies which use mechanical interrupters with high current withstand capability, but it may lead to excessive heating in the power electronic switches used in for example the load commutation switches of hybrid HVDC CBs.

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3.4 AC SHORT-CIRCUIT GENERATOR CIRCUIT

AC short-circuit generator(s) running at various frequencies have been used for HVDC CB testing in a number of fields. In [17] a low-frequency (10 Hz) short-circuit generator in combination with a step-up transformer was used to test a 250 kV, 8 kAN HVDC CB. The main aim of this test was to verify the DC current interruption capability of the HVDC CBs developed from a number of mechanical interrupters arranged in series and/or parallel. The total time of interruption and hence, the total energy that the HVDC CB had to absorb, was not considered in these tests.

More recently, a short-circuit generator at power frequency (50 Hz) was used to test an HVDC CB with rated short circuit breaking current up to 16 kA [18], [7]. In this case the HVDC CB was required to interrupt the AC current at its peak value as shown Figure 3-6.

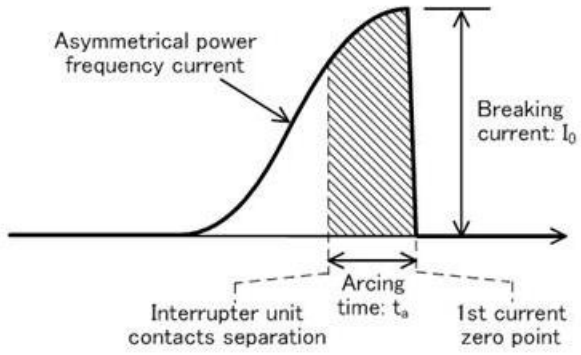

Figure 3-6: Power frequency AC current Interruption by HVDC CB at crest value of current

The tests using short-circuit generator(s) discussed in the technical literature mainly focus on producing the maximum quasi–DC current for a longer duration while the magnitude of the driving voltage of the test circuit is not of prime concern. In those tests, interruption is deemed as successful if the CB interrupts the peak AC current well before its natural current zero. However, when the AC current is at its peak, the driving voltage is zero and changes its polarity afterwards. This causes the generators to absorb energy from the system instead of supplying energy to be absorbed by the HVDC CB. This makes the current suppression time much shorter and reduces energy stresses on the breaker. Therefore, a method to ensure sufficient energy contribution from an AC short-circuit generator, by maintaining its voltage magnitude within an acceptable range for the entire test duration (breaker operation time + current suppression time), is necessary.

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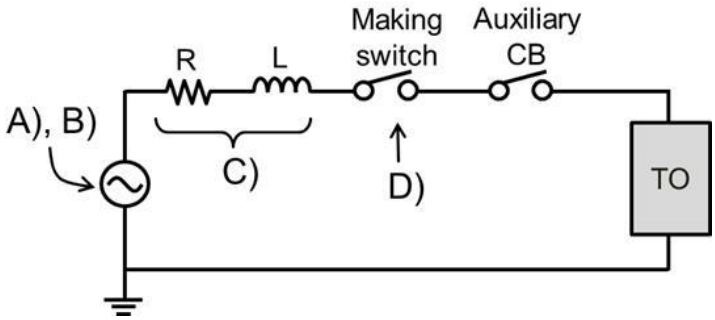

Figure 3-7: Schematic diagram of AC short circuit generator test circuit and parameters

The use of AC sources for testing HVDC CBs has been applied for low voltage HVDC CB interruption tests and is specified in the international standards for DC switchgears for railway applications (IEC 61992-2). In this section, the possibility to extend this method to high voltage HVDC CB testing is considered.

The main circuit parameters that can be controlled are as follows:

A) AC short-circuit generator source frequency;
B) AC short-circuit generator source voltage;
C) Impedance (source and additional)
D) Making phase angle

Figure 3-7 shows a schematic diagram of a generic AC short-circuit generator based test circuit and indicates the circuit factors which corresponds to the parameters respectively. Each of these parameters is adjustable within a range, with the exception of the making phase angle which is freely adjustable to a high degree of accuracy. The source voltage can be adjusted but its maximum is proportional to the generator frequency and short-circuit power available in the test lab. The generator and transformer leakage reactance exists by default, thus putting a minimum limit on the circuit impedance. However, this may be increased with additional external inductance. The minimum limit on circuit impedance and maximum limit on available source voltage limits the maximum di/dt which can be achieved.

An auxiliary breaker shown in Figure 3-7 is included in the test circuit to isolate the test object from the generator after the HVDC CB clears the fault current, thus functioning as a residual current breaker. The arcing auxiliary breaker introduces a small voltage drop due to the arc voltage which can be easily compensated for by adjusting the generator source voltage. The opening timing of the auxiliary circuit breaker is adjustable and can be timed to coincide with the current suppression period such that its arc will quench the moment the current is suppressed. This isolates the test circuit from the test object, and makes application of the recovery voltage across the HVDC CB terminals (as in a practical HVDC system) after current interruption possible. Furthermore, the auxiliary breaker must be rated to withstand the difference between the AC generator voltage and the DC dielectric stress voltage on the HVDC CB. More details on the technique to apply dielectric stress after current interruption are discussed in Chapter 4.3.

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It must be clear that the main assumption is that the short-circuit generator(s) have sufficient power and, with the use of step-up transformers can produce the desired magnitude of AC voltage at a given frequency. In fact, the required di/dt can only be realized with careful choice of making angle (θ) for the AC voltage of the generator(s) as described in:

$$\frac{di}{dt} = \frac{E_m \sin(\omega t + \theta) - Ri}{L} \tag{5}$$

The maximum rate of rise of current at the inception of the short circuit is obtained when the source voltage is at its crest. However, the moment the source voltage passes its crest value i.e. $\omega t + \theta > \pi/2$, the di/dt starts to decrease proportionally to the source voltage. In order to avoid this and have sufficient di/dt during the breaker operation time, the making angle is reduced to a value of $\theta < \pi/2$. In addition, the other important point is that it is necessary to maintain sufficient source voltage to supply energy during the current suppression process as discussed in chapter 2. This can be achieved by running the short-circuit generators at a reduced frequency. Thus, depending on the length of the breaker operation time, the making angle θ and the power frequency become optimization parameters for both sufficient rate of rise of current and sufficient energy contribution. This is illustrated in Figure 3-8 where *θ* and *f* are chosen so that the source voltage peak appears at t_5.

A more detailed discussion on the influence of the test circuit parameters on the test waveforms is given in chapter 4,.

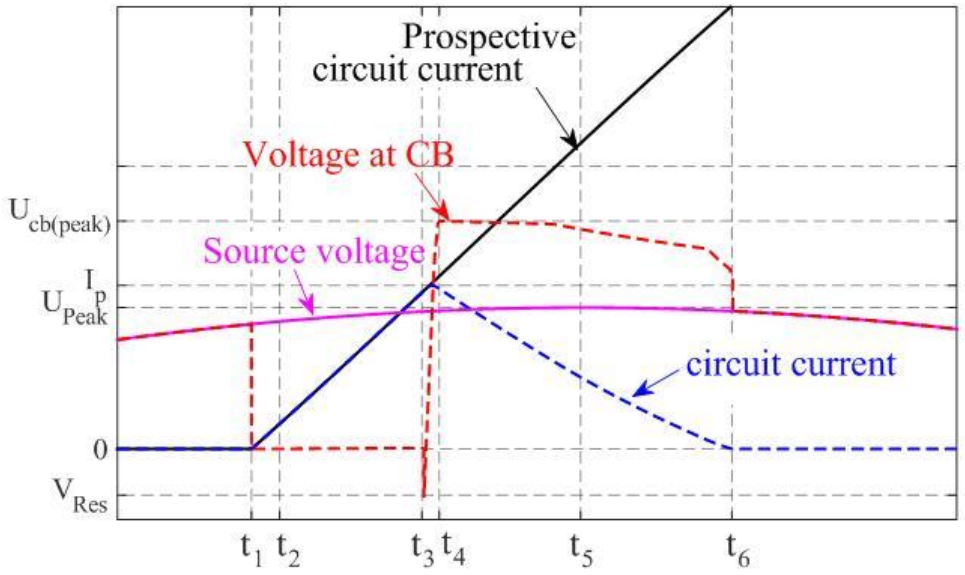

Figure 3-8: Simulated test results using low-frequency (16 2/3 Hz) short-circuit generator(s) demonstrating the choice of making angle that result in peak source voltage appear during energy absorption phase. If the breaker operation time is longer, lower making angle is chosen.

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3.5 COMPARISON

In order to investigate the performance of these methods, a simulation study was conducted on the charged capacitor, charged inductor and AC short-circuit generator method at different frequencies. Two cases have been studied, corresponding to breaker operation times of 2 ms and 8 ms, respectively. Note that these two cases represent different HVDC CB technologies and therefor should not be compared directly to each other.

3.5.1 BREAKER OPERATION TIME OF 2 MS

A hypothetical HVDC CB with rated voltage of 80 kV and a rated short-circuit breaking current of 9 kA has been considered. Breaker operation time of 2 ms is assumed in this case for comparison. The test circuits are compared by keeping the circuit parameters (circuit resistance of 0.25 Ω, inductance of 20 mH, source voltage of 80 kV, and the interrupted current of 9 kA) equal for each case. In case of the charged capacitor circuit, a capacitance of 506 µF is used. Figure 3-9 shows simulation results of test circuits when current in each case is interrupted by an HVDC CB.

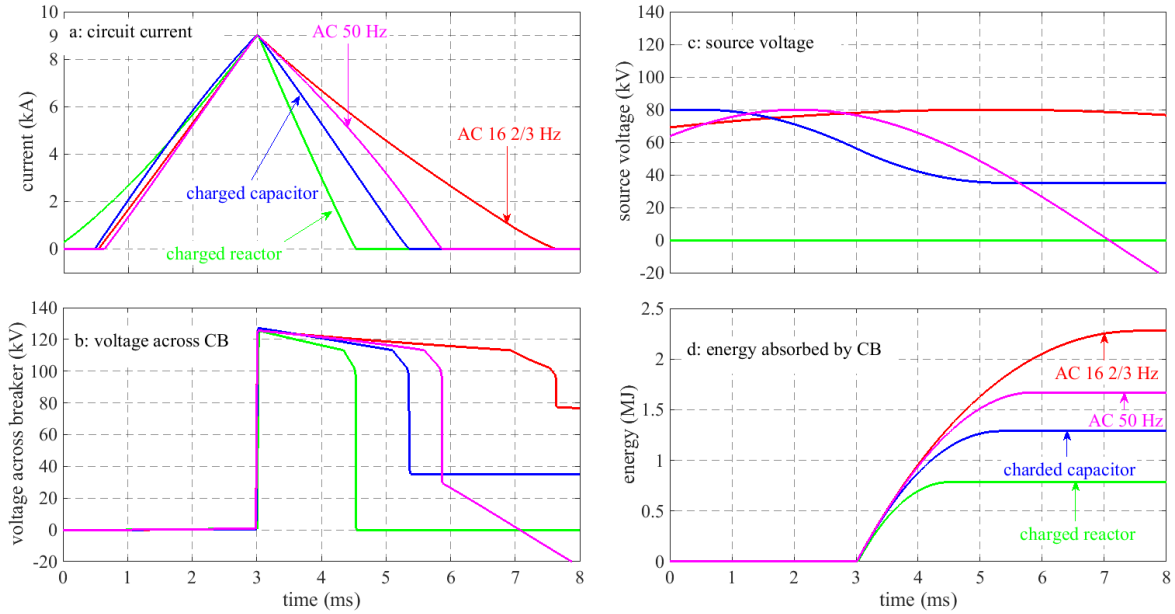

Figure 3-9: Comparison of simulation results of various test circuits (breaker operating time is 2ms).

Considering the plots in part (a) of Figure 3-9 there is a slight difference in di/dt during fault neutralization time especially for the charged reactor and the charged capacitor test circuits. However, the main difference among the various test circuits is during the energy absorption phase which results in a significant difference in time to clear the fault. This difference is due to the fact that for each of the test circuits, the magnitude of the source voltage during the energy absorption phase is different (see Figure 3-9 b). The difference is also clearly reflected in the amount of energy absorbed by the breaker for each test circuit where the maximum energy is

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achieved by the low frequency AC short-circuit generator based test circuit (2.28 MJ), followed by the AC short-circuit generator run at 50 Hz (1.67 MJ), as can be observed from Figure 3-9 (c).

Note that, for each of the circuits the energy in the system $0.5LI_P^2$ at the moment the counter voltage starts to act (see Figure 3-9 a) is identical since the magnitude of reactor (L) used for each case is kept the same (20 mH). Therefore, the extra energy to be dissipated in the arrester is contributed by the voltage source in the circuit as described by equation (2).

The charged reactor method does not have an energy source, hence only the energy stored in the reactor (0.79 MJ) is dissipated. Similarly, for charged capacitor test circuit, since a significant portion of the charge stored in the capacitor bank is already transferred to the reactor and the breaker at the beginning of the current suppression phase, the energy contribution from the capacitor (1.2 MJ) during the current suppression period is minimal. Thus, with respect to the energy requirement, given the same circuit set-up the charged reactor and charged capacitor test circuits are less capable for testing an HVDC CB regarding its energy handling capability.

None of the proposed test circuits apart from a controlled rectifier (provided it has a sufficiently high power rating) is capable by itself of testing an open-close-open reclosing cycle with full current, voltage and energy stresses during the open operations. If this type of full reclosing is required of HVDC CBs in the future and must be tested as such, parallel test circuits, regardless of the type, will have to be used, switched in sequence, to achieve this. Alternatively, testing of functionality, energy absorption rating and endurance can be split into separate tests.

The main conclusion from the simulation results of the test circuits shown in Figure 3-9 is that the ac short-circuit generator method is able to contribute the highest energy to the test object. Furthermore, lower frequency generally increases the energy contribution. Compared to charged reactor and charged capacitor test methods, 50 Hz AC generator have better performance. However, when evaluated with respect to 16 2/3 Hz AC source test circuits, 50 Hz AC source lacks sufficient energy stress on the test object. Note that a capacitance of the charged capacitor is 506 µF to match 50 Hz.

Note that: considering only the testing of current interruption or commutation capability, charged capacitor and charged reactor test circuits are also suitable candidates. For supplying sufficient energy, however, large capacitor and inductor are required.

3.5.2 BREAKER OPERATION TIME OF 8 MS

For a hypothetical HVDC CB with a breaker operation time of 8 ms, the energy requirement is more onerous. Since the dissipated energy, described in equation (2), consists of the energy stored in the system inductance, and that provided by the system (or source), in this section the test circuits are first compared by keeping the test ciruits inductance equal to study the impact of the differences in source voltages between different test

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circuits. Secondly, the impact on the test circuits is compared when they are designed to deliver the same total energy stresses.

3.5.2.1 SAME CIRCUIT INDUCTANCE

Figure 3-10 shows the simulation results of the test circuits when considering breaker operation time of 8 ms, assuming the same total circuit inductance of 35 mH for all test circuits in the simulations and a rated short circuit breaking current of 16 kA. The test circuits are compared in terms of the energy stresses they supply to the test breaker. For a charged capacitor test circuit, a 2 mF capacitor bank charged to 80 kV is discharged through a 35 mH reactor as specified above. For the AC short-circuit generator based test circuits, a peak voltage of 63.6 kV is used in the simulation. Note that a different peak source voltage than the charging voltage of the capacitor test circuit is selected, to make sure that the test current does not rise to a value more than 16 kA at the end of fault neutralization time. In other words, if the same voltage as the charged capacitor is used, a different value of current limiting reactor (circuit inductance) than specified above has to be used to adjust current to 16 kA. For the charged reactor test circuit, the breaker receives a trip order after the current is fully commutated to the test HVDC CB (see Figure 3-4 and Figure 3-5). There is decay of current due to inherent resistance in the circuit.

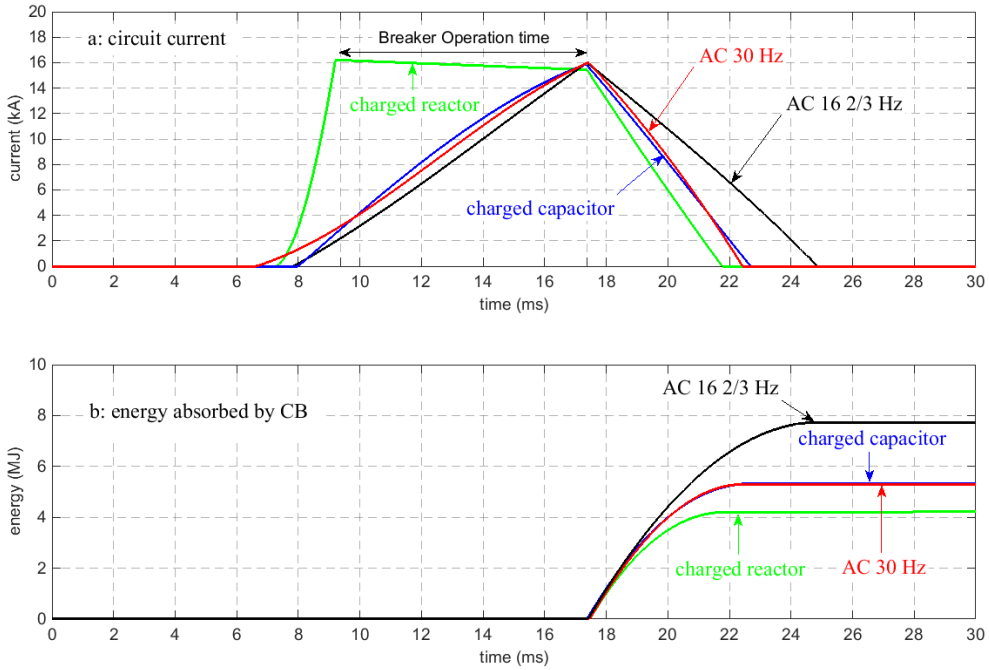

Figure 3-10: Comparison simulatation results of various test circuits (Breaker operation time of 8 ms is assumed)

It can be seen from Figure 3-10 that the test circuit at 16 2/3 Hz frequency supplies more energy to the test breaker even with low peak value of source voltage compared to the charged capacitor test circuit. This is purely due to the flexibility offered by AC short-circuit generators in choosing a making angle whereas for a charged capacitor it is always at the peak voltage that a short circuit can be applied. Note that, as will be

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discussed in subsection 4.1.2, the choice of different making angles results in different energy absorptions. In theory, the capacitance of a charged capacitor bank can be increased (to more than 2 mF) if more energy is needed as discussed in 3.2.

3.5.2.2 SAME ENERGY DISSIPATION

In the previous section the different test circuits were compared based on their performance in case the same circuit inductance was used. It could be seen that due to its ability to sustain source voltage during current suppression, the 16 2/3 Hz short-circuit generator can achieve the highest energy stresses of 7.8 MJ. In this section, the other test circuits are adapted to achieve the same energy stress, to study the impact on the test circuit parameters.

Table 3-2: Circuit parameters for charged capacitor test circuit

Capacitor (µF)	Inductor (mH)	Voltage (kV)	Energy (MJ)	Peak interruption current (kA)	Fault neutralization time (ms)
2850	41	80	7.7	16	9.4

For the charged capacitor method, a 2.85 mF capacitor needs to be charged at 80 kV and discharged through a 41 mH inductor to supply 16 kA interruption current and an energy stress of 7.7 MJ to the HVDC CB.

Table 3-3: Circuit parameters for charged reactor test circuit

Inductor (mH)	Charging voltage (50 Hz) (peak) (kV)	Energy (MJ)	Peak interruption current (kA)	Making angle (degrees)	Fault neutralization time (ms)
60	212	7.5	16	13º	9.5

For the charged reactor method, a reactor of 60 mH needs to be charged to supply an energy stress of 7.5 MJ. In order to take into account the decay in current during breaker operation time, the reactor is charged to (16.7 kA) a value higher than 16 kA. This is assuming a very high quality factor reactor (Q=75), otherwise it needs to be charged to a larger current for reactors having lower quality factor. Note that the reactor is charged using AC source running at 50 Hz. For this a source voltage of 212 kV (peak value) is needed assuming a source having internal inductance of 5 mH.

Table 3-4: Circuit parameters for reduced frequency AC short-circuit generators at 30 Hz and 16 2/3 Hz

Frequency (Hz)	Inductor (mH)	Voltage (peak) (kV)	Energy (MJ)	Peak interruption current (kA)	Making angle (degrees)	Fault neutralization time (ms)
16 2/3	35	63.6	7.75	16	42º	9.4
30	48	87	7.75	16	13º	11.15
50	110	282	7.66	16	9º	8.6

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Table 3-4 shows circuit parameters for AC short-circuit generators running at different frequencies (16 2/3, 30 and 50 Hz). Circuit components and parameters are dimensioned to supply a 16 kA current and 7.8 MJ energy. As the frequency increases, larger reactor sizes are needed to compensate for the rapidly dropping source voltage. An increase in reactance necessitates an increase in the source voltage because of the impedance increase due to frequency. Looking at the circuit parameters of test circuit at 50 Hz, a reactor of 110 mH and a supply voltage (peak) of 282 kV is required to produce the test current. Note that at 16 kA, energy of about 14.1 MJ is stored in the reactor. However, of this energy, only 7.66 MJ is absorbed by the breaker. The rest of the energy is fed back to the generator when the polarity of the source voltage changes in the AC cycle. Another important point to note while using a 50 Hz AC source is that the theoretically achievable asymmetric current flows only for a maximum of 20 ms. Of this time, current peak is reached in the first 10 ms. This entails the need to interrupt current before 10 ms (before current peak) is reached and puts a natural limit on the ability to test HVDC CBs with longer breaker operation times.

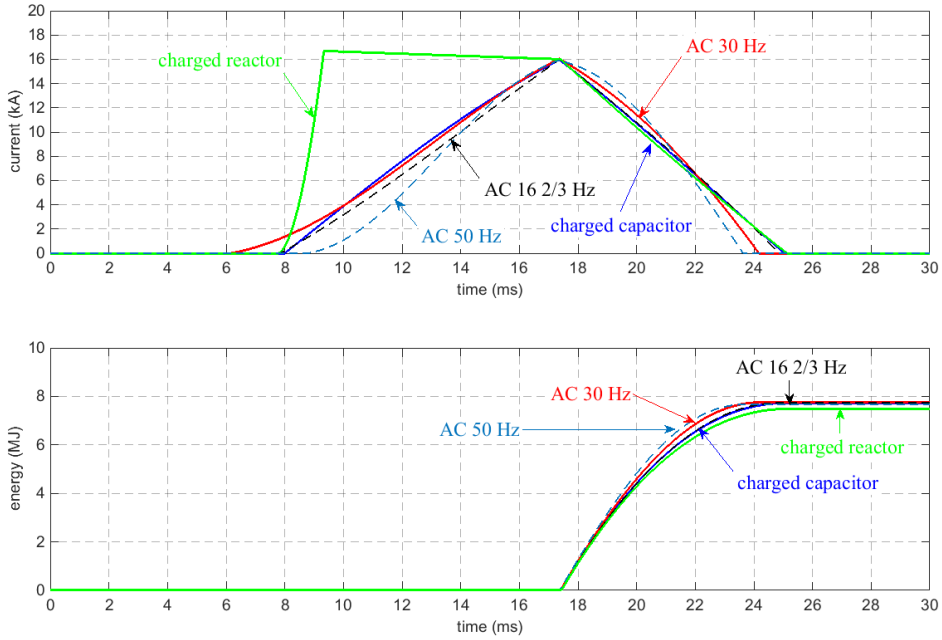

Figure 3-11: Current and energy stresses produced by various test circuits. The circuit parameters and component sizes are designed to match the energy stress supplied by low frequency AC short-circuit generator at 16 2/3 Hz.

3.5.3 SUMMARY

The test methods examined in the previous sections are summarised in Table 3-5 and compared against the test circuit requirements discussed in Chapter 2. Considering the already established use of AC short-circuit generators for testing AC CBs at existing test facilities and the flexibility it provides for adjusting test parameters, the short-circuit generator method is considered to be suitable for testing HVDC CBs. Therefore, a test circuit based on a short-circuit generator is used for demonstration of HVDC CB performance in the PROMOTiON project.

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Table 3-5: Summary of test methods and their applications

Test circuit requirement	Recitfier	Charged capacitor	Charged reactor	AC short circuit generator
Pre-condition HVDC CB	Current profiles and stresses can be accurately controlled to follow a target waveform.	Separate circuit required	Separate circuit and/or source required	Separate circuit or source required
Produce test current	Current profiles and stresses can be accurately controlled to follow a target waveform.	Very high di/dt can be achieved	Difficult to control di/dt. Quasi DC current can be obtained in case very fast switching cannot be achieved. Hence the method may not be suitable for testing HVDC CBs with power electronics in the normal current path.	The existence of minimum inductance in the circuit due to generator and transformer reactance put maximum limit on di/dt
Supply rated energy to the HVDC CB and withstand TIV	Current, voltage and energy profiles and stresses can be accurately controlled to follow a target waveform. However, large required power supply may be prohibitively expensive to realize	Requires large capacitance, with associated volume and cost.	Requires large reactance with very high quality factor, with associated impact on charging circuit, volume and cost.	Very high voltage (full-pole voltage) may exceed the insulation coordination of test installation or multi-part, multi-unit tests to be applied.
Supply rated dielectric stress	Voltage stresses can be accurately controlled to follow a target waveform	Some DC charge remaining after suppression. Very large capacitance required to make this sufficient for testing	Must be realised by separate source/circuit.	After suppression, AC voltage stress is applied by the generator. Controlled DC stress must be realised by separate source/circuit
Avoid damage to the HVDC CB and test circuit	Must be realised by additional circuit provisions	Must be realised by additional circuit provisions	The peak current is the same as rated interruption current	Must be realised by additional circuit provisions
Be implementable / economical	High investment cost and complex control	Can utilise existing test facilities in some cases	Accurate switching of charging circuit is required; High quality factor reactor is required; Challenging to achieve high currents	Utilises existing test facilities, with minimal additional investment cost required. Within a reasonable range, can provide full testing to prototype-level HVDC CB
Test extra functionality such as reclosing, soft-closing, etc.	Current, voltage and energy profiles and stresses can be accurately controlled to follow a target waveform	Separate circuit and/or source required	Separate circuit and/or source required	Separate circuit and/or source required
Application	Low to medium voltage testing	Interruption-only tests very low energy	Low-medium current and energy	Full current, high energy testing.

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From the comparison, the following can be concluded with respect to the requirements for test circuits designed for testing DC fault current breaking:

- Pre-condition the HVDC CB – Except for the case of the rectifier circuit, all test methods will require additional sources or circuit adjustments to emulate the pre-fault load current stress
- Produce a test current – The charged reactor method offers little control over the di/dt during the breaker operation time which may render it unsuitable for current breaking testing. The AC short-circuit generator method offers flexible control over the di/dt but is limited in achievable di/dt by the unavoidable internal inductances of the generators and required transformers. However, this needs to be evaluated for the particular laboratory as to what can be achieved. Very high di/dt can be achieved using a charged capacitor method based circuit.
- Supply rated energy to the HVDC CB and withstand TIV – Both the charged capacitor and charged reactor based test circuits require large and high volume installations in order to supply sufficient energy during the current suppression period. Short circuit generators offer flexible control over the amount of energy dissipated. For HVDC CBs with long breaker operation times, a reduced frequency must be used to avoid excessive decay in sinusoidal source voltage and provide sufficient energy.
- Supply rated dielectric stress – The charged capacitor, charged reactor and AC short-circuit generator based test circuits all require additional sources or circuit provisions to supply adequate DC voltage stress after interruption.
- Avoid damage to the HVDC CB and test circuit - The rectifier circuit, charged capacitor, and AC short-circuit generator based test circuits all require additional sources or circuit provisions to protect the test object and the test circuit from damage
- Be implementable / economical – The charged capacitor and reactor methods may due to their relative simplicity, be implementable but costly at high ratings. AC short-circuit generators are very costly but already a commonly used test source for AC equipment and available at several short-circuit laboratories worldwide, therefore constituting a flexible and cost-effective test method. Although theoretically possible to build a controlled rectifier circuit, the associated cost for higher current, voltage and energy ratings is likely to be prohibitively high, and their use is belived to be restricted to lower energy testing applications.
- Test extra functionality - The charged capacitor, charged reactor and AC short-circuit generator based test circuits all require additional sources or circuit provisions to test additional functionality

All test methods have the technical possibility to test HVDC CBs but may outperform each other in certain aspects. Some aspects such as post suppression dielectric stress must in all cases be realized through separate sources or provisions. Therefore, based on the specific HVDC CB requirements, it may be necessary to utilise alternative test methods. This may occur when the energy dissipation is particularly high, for example, and short-circuit generators may not be able to apply the required energy. In this case alternatives such as synthetic and multi-part, or a combination of, may be applied. These are discussed in chapter 4 and 5. In the appendix, a table is included which shows the circuits ability to verify any of the other stresses discussed in D5.4.

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4 AC SHORT CIRCUIT GENERATOR BASED TEST CIRCUITS

The demonstration of HVDC CBs in Work Package 10 will be performed using an AC short-circuit generator based test circuit. As discussed in the previous chapter, AC short circuit generators offer some merits over other test circuits based on their flexibility of control and ability to supply large amounts of energy. However, additional sources or circuit provisions must be made to meet the requirements of a test circuit discussed in Chapter 2. This chapter will discuss the parameters that enable the flexibility of control, some limitations in application and the additional provisions that can be made to enable protection and post suppression DC dielectric stress.

4.1 TEST CIRCUIT PARAMETERS

Four parameters must be set in AC short-circuit generators, namely frequency, circuit inductance, source voltage magnitude, and making phase angle. This section qualitatively describes the impact of these parameters except for circuit inductance, one by one, around the test stress targets shown in Figure 2-3.

4.1.1 IMPACT OF FREQUENCY (CONSTANT PEAK CURRENT)

In this section, the influence of generator frequency on interruption performance is demonstrated. Peak current is kept constant through small adjustments to source voltage, inductance and making phase. Generator frequencies of 16 2/3 Hz, 30 Hz and 50 Hz are investigated. Theoretically, a reduction in frequency results in an extended half-cycle period, which allows a larger amount of energy to be transferred from the source to the test object (assuming frequency can be changed independently of voltage). However, generator output voltage is proportional to frequency and to the available short-circuit power.

Table 4-1: Impact of AC Short-circuit generator frequency assuming fault neutralization time of 10 ms

Parameter	Target (A)	Frequency [Hz]		
		16 2/3	30	50
V_s [kV]	-	80	100	100
R [ohm]	-	0.01	0.01	0.01
L_s [mH]	-	58.0	65.0	50.0
Making phase [deg.]	-	79.6	78.2	9.4
Peak Current [kA]	12.6	12.6	12.7	12.7
Peak TRV [kV]	125.0	125.0	125.0	125.0
Dissipation energy [MJ]	4.4	5.6	4.9	3.0
Energy dissipation time [ms]	7.3	6.9	5.8	3.7

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Table 4-1 and Figure 4-1 show the simulation results of the impact of AC short-circuit generator frequency. Results demonstrate that in case of 16 2/3 Hz and 30 Hz, interrupting current and MOSA dissipation energy can fulfil the requirement of target A. However, in case of 50 Hz, both requirements cannot be fulfilled. Therefore, for the target A, frequency range of less than 30 Hz may be applicable.

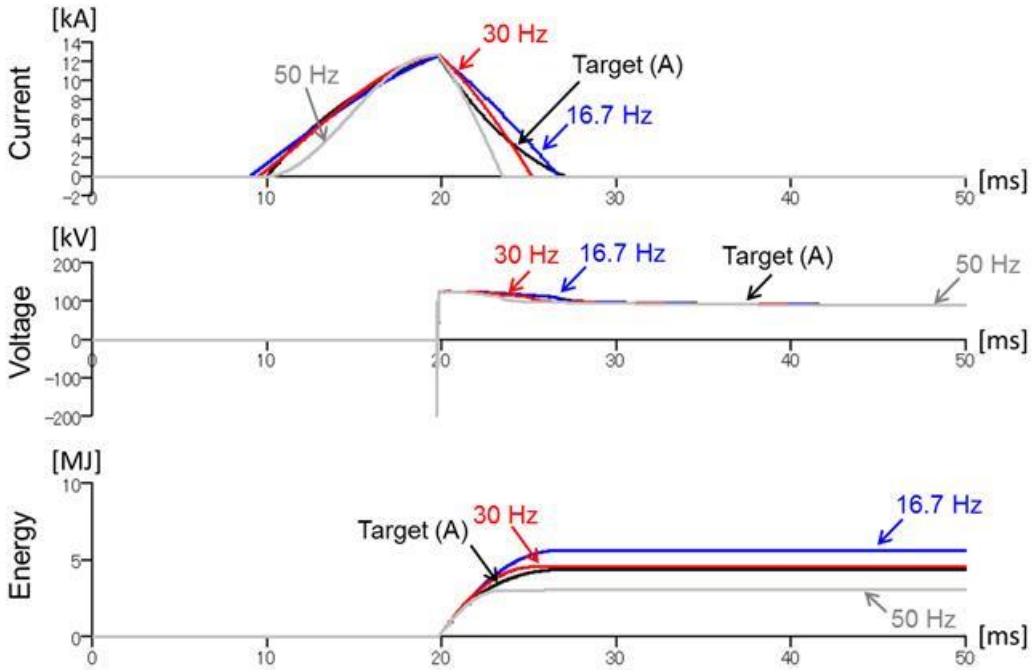

Figure 4-1: Simulation results of impact of AC short circuit generator frequency

The difference is caused by the duration of the source voltage waveform with respect to the total fault current interruption time, and its ability to supply energy during the current suppression period.

4.1.2 IMPACT OF MAKING PHASE ANGLE (CONSTANT PEAK CURRENT)

In this section, the influence of making phase angle on interruption performance is investigated. Results are shown in Figure 4-2. Three making phase angles are investigated – 12, 42 and 72 degrees. It is demonstrated that a smaller making phase angle results in a larger energy transfer to the HVDC CB; a larger making phase angle results in a lower energy transfer (and thus energy dissipation in the MOSA). This also influences the energy dissipation time.

For the target waveforms, 42 degrees is most appropriate. There is only a small error in both energy dissipation time and energy dissipation magnitude, as shown in Table 4-2. These simulation results show that making phase can be used to give fine control over the HVDC CB energy dissipation, as required.

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Table 4-2: Impact of making phase angle (AC short-circuit generator frequency: 30 Hz)

Parameter	Target (A)	Frequency: 30 Hz		
Making phase [deg.]	**N/A**	**12**	**42**	**72**
V_s [kV]	-	80	80	80
R [ohm]	-	0.01	0.01	0.01
L_s [mH]	-	52.0	55.0	45.0
Peak Current [kA]	12.6	12.5	12.6	12.3
Peak TRV [kV]	125.0	125.0	125.0	125.0
Dissipation energy [MJ]	4.4	5.9	4.6	2.8
Energy dissipation time [ms]	7.3	6.8	5.6	3.7

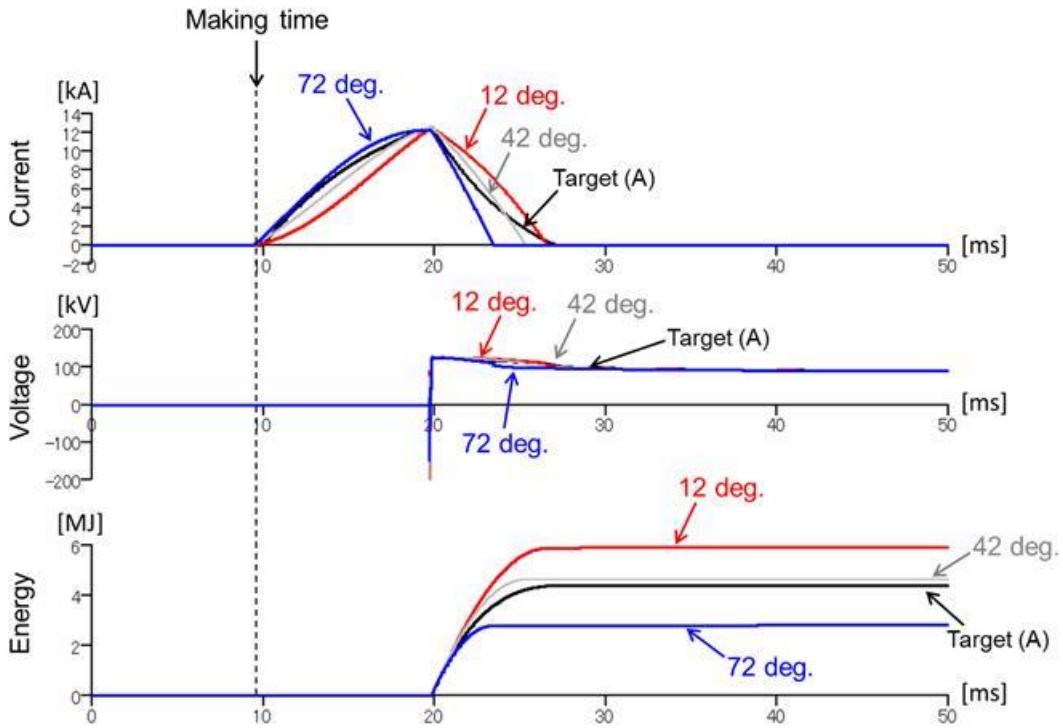

Figure 4-2: Simulation results of impact of making phase for the condition of source voltage 80 kV, frequency 30 Hz

4.1.3 IMPACT OF SOURCE VOLTAGE MAGNITUDE

Large number of transformers are needed to compensate for the decrease in output voltage due to running short-circuit generators at reduced power frequency. This requires very high current at the generator terminals, which may, together with the long arc duration at reduced power frequency, challenge the protective master breakers. In order to mitigate these stresses, the application of relatively higher frequency is explored. For instance, Figure 4-3 depicts a comparison of results when using AC short-circuit generators running at 30 Hz. In

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this case a breaker operation time of 2 ms and current interruption of 9 kA is assumed. From Figure 4-3 it can be seen that by slightly increasing the peak voltage of AC source at 30 Hz, the energy stress delivered to the HVDC CB can be increased.

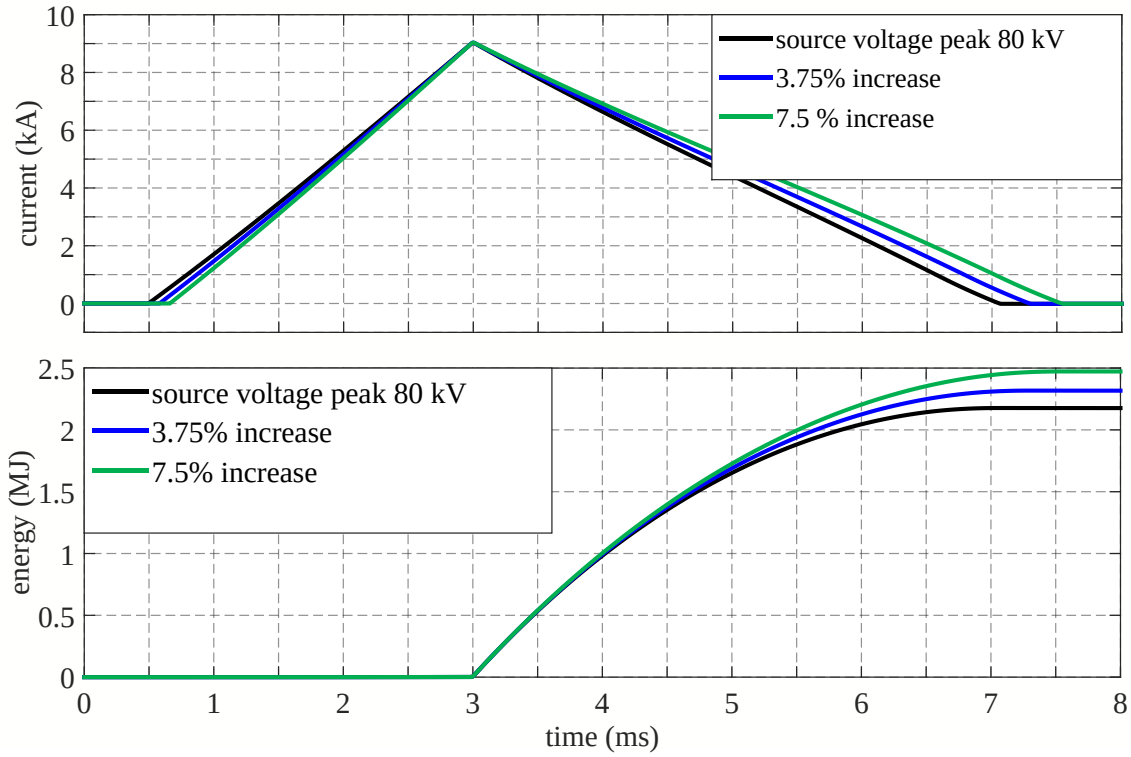

Figure 4-3: Comparison of simulation test results using AC short circuit generator running at 30Hz and AC voltage peak increased – breaker operation time is 2 ms

Figure 4-4 shows simulation results considering HVDC CBs with 8 ms breaker operation time. In this case a total of 10 ms fault neutralization time, of which 8 ms is breaker operation time, is assumed. When simulating at different voltage magnitudes the circuit inductance is adjusted in order to obtain a breaking current of 16 kA at the end of fault neutralization time. The generator frequency and the making angle are kept the same for all simulation cases to 30 Hz and 18^0, respectively. Thus, by adjusting the driving voltage magnitude and circuit inductance, the energy stresses on the test breaker can be varied. At this frequency (30 Hz), low making angle (18^o) is needed to ensure sufficient loop duration for current and voltage.

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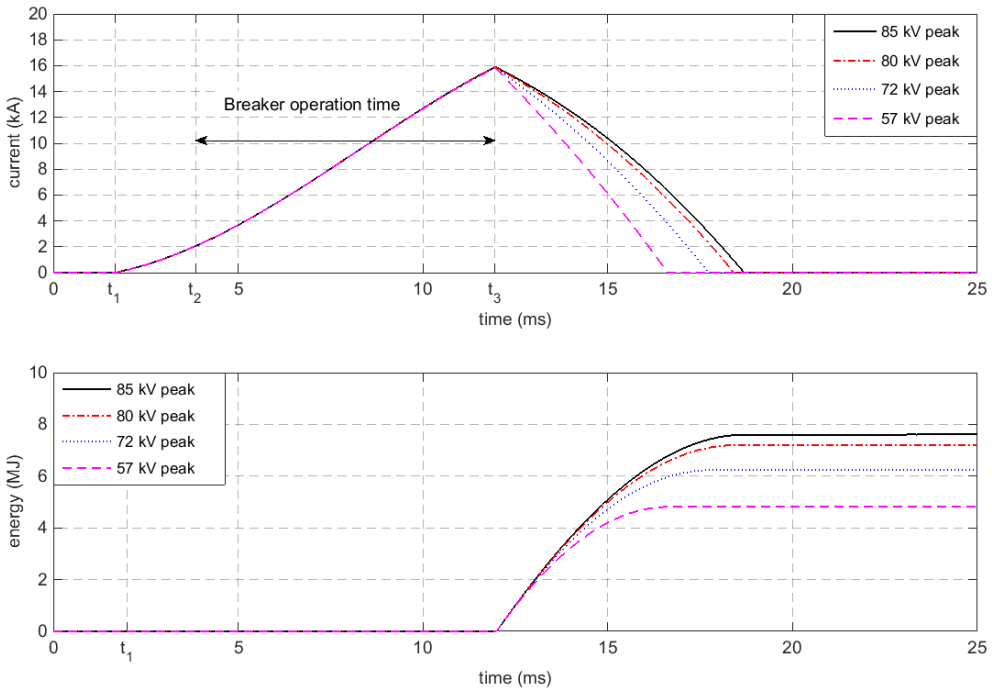

Figure 4-4: Comparison of simulation test results using AC short circuit generator at 30 Hz. Top graph shows interrupted currents for different values of driving voltage magnitudes. Bottom graph: energy absorbed during current interruption – breaker operation time is 8 ms

4.1.4 PRACTICAL LIMITATIONS FOR LONG BREAKER OPERATION TIMES

Typically, AC short-circuit generators have a lower bound on operating frequency. This inherently places a limit on the ability to adequately test HVDC CBs with long breaker operation times. HVDC CBs having breaker operation time longer than half a period of the test circuit frequency cannot be tested. For example, for a test circuit having a frequency of 16 2/3 Hz, the maximum theoretical current rise time that can be achieved is 30 ms (if making angle is practically zero). Figure 4-5 shows simulation results of the prospective current and the source voltage of 16 2/3 Hz AC generator based test circuit. Depending on the breaker operation time, the breaking current can be adjusted by putting additional impedance in the circuit.

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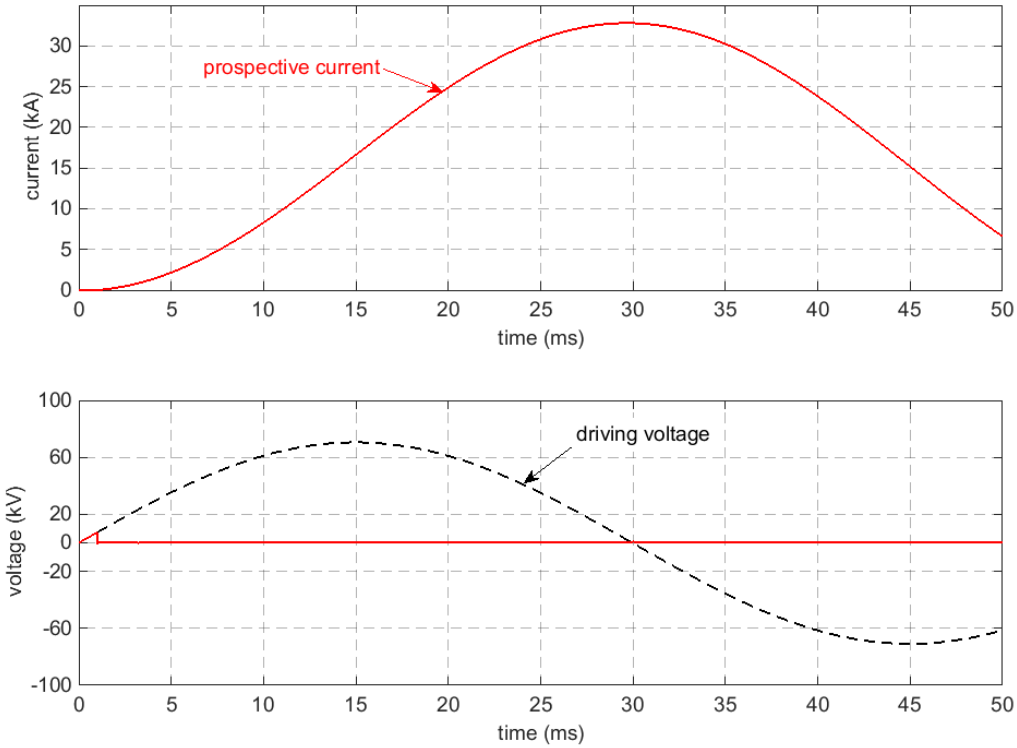

Figure 4-5: Prospective current and driving voltage with maximum assymetry at 16 2/3 Hz

As described in previous section, an HVDC CB can be made to interrupt current at the crest value of the prospective current. However, after this moment the generator starts to absorb the energy in the circuit and this will affect the energy absorption of the HVDC CB. Therefore, the reduced frequency AC short-circuit generator method is more effective for testing HVDC CBs having breaker operation time shorter than the half period of the circuit frequency. In case the breaker operation time exceeds the limits imposed by the generator frequency, alternative testing methods as described in the next chapters may be considered to apply sufficient voltage and energy stress.

Another critical issue in using short-circuit generators is the accurate control of the making angle: the instance on the voltage waveform when the short-circuit current is initiated has an impact on the rate of rise of current and the energy absorbed by the HVDC CB. A very slight deviation from the desired making angle could result in higher or lower interrupted current, thus resulting in different energy absorption than desired by a test. Figure 4-6 shows the impact of variation of the making angle on the rate of rise of current. If the same current has to be interrupted (16 kA shown by dashed horizontal line), different fault neutralization periods result. Keeping the breaker operation time the same for all the cases, the breaker has to receive a trip order depending on the actual making angle during a test.

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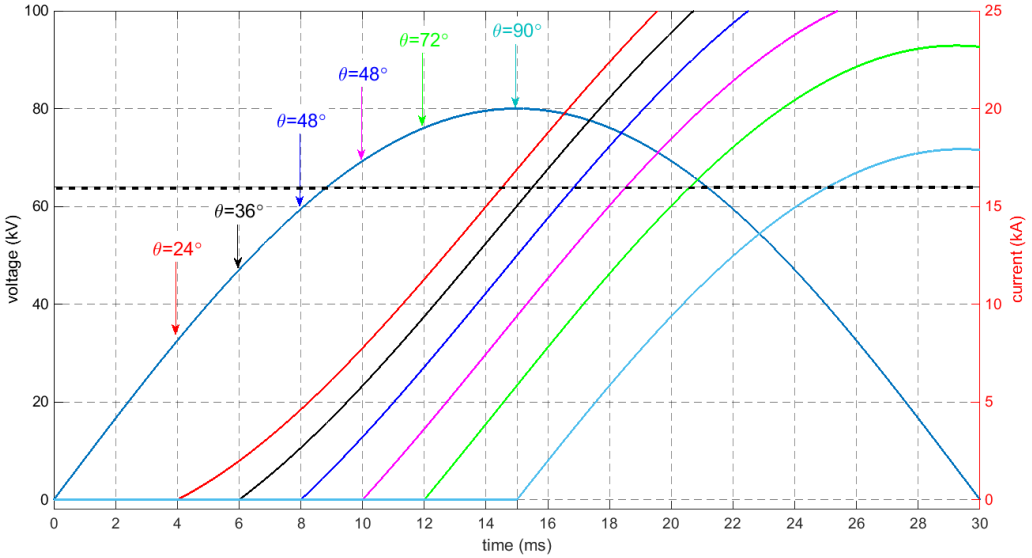

Figure 4-6: Impact of the making angle on rate of rise of current (16 2/3 Hz)

However, accurate prediction of a making angle can be very challenging. Especially, if there is a discharge of the making switch because of a pre-strike, there will be significant challenge to obtain a valid test (a test with desired stresses). One possible way to reduce the impact of pre-strike is to locate the making switch on the low voltage side of the generator step-up transformers.

Figure 4-7 shows the energy absorbed by the HVDC CB when interrupting 16 kA current in the same circuit but with different making angles. It can be seen from the figure that even if the same circuit inductance and the same source voltage is used, considerably different amounts of energy are absorbed by an HVDC CB under different making angles.

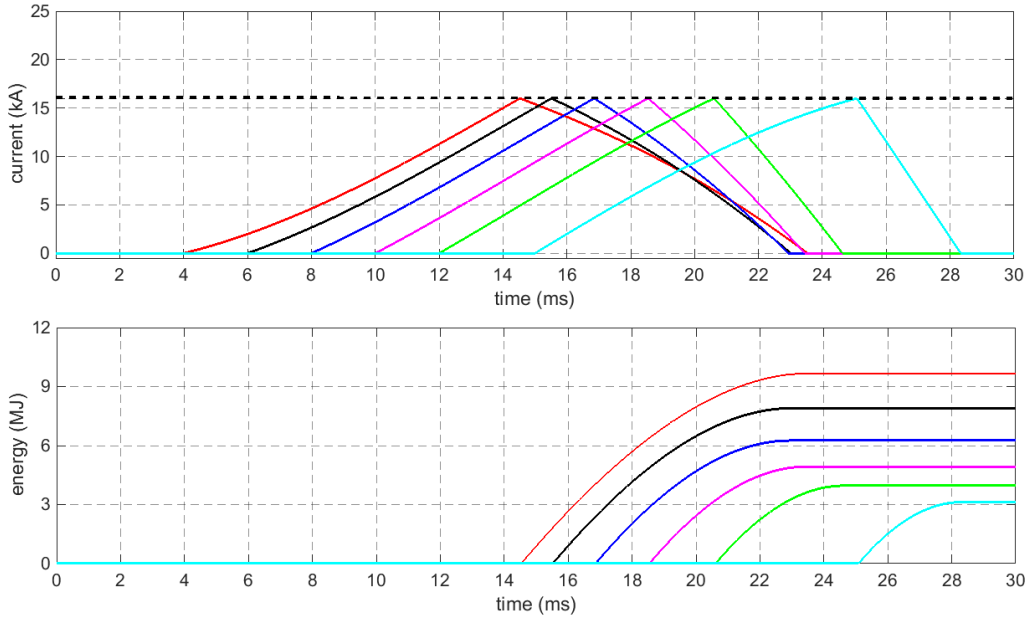

Figure 4-7: Impact of making angle on energy absorbed by the HVDC CB

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Therefore, a test installation should have a making switch that allows fine control over the making angle. In addition, in order to produce a valid test, the relay communication between the test circuit and HVDC CB should take into account the actual making angle during a test.

There are other practical limitations some of which are described below:

- **Sufficient short-circuit power**: In order to adequately test the HVDC CB's energy absorption capability as well as its recovered insulation strength, the source voltage should maintain a sufficiently high magnitude throughout the current suppression period. Depending on making angle and frequency, the source voltage will start dropping during interruption period. It must, therefore, be ensured that the test frequency is low enough that the value of the source voltage throughout the current suppression period is sufficiently high to deliver the required energy dissipation. However, reducing frequency reduces the generator voltage proportionally and available power at a square of reduction ratio. Therefore, besides the capability of running at reduced power frequency, a test installation needs to have sufficient short-circuit power available for testing when running at reduced frequency.
- **Minimum circuit inductance:** several generators and transformers are required to obtain sufficient source voltage. The generators and transformers have inherent reactance which puts an upper bound on the achievable rate of rise of current. This becomes a critical issue when testing HVDC CBs with short breaker operation time. This upper limit may not cause limitations in testing HVDC CBs with long breaker operation times.
- **Auxiliary AC circuit breaker:** As described in the previous subsection, an additional AC circuit breaker with high voltage withstand capability is needed to separate the generator from the test HVDC CB.
- **Testing of re-closure capability of HVDC CBs:** reclose capability becomes very challenging when using AC short circuit generators for testing of HVDC CBs. When re-closure time is short (few tens of milliseconds), the test circuit using AC generators at reduced power frequency is impossible unless separate power sources are used.

The test parameters including source voltage, source inductance and source frequency are all interdependent. Choosing their values is not straightforward and depends for a large part on the purpose of the test and on simulation studies.

4.2 METHODS TO PROTECT THE TEST OBJECT AND TEST CIRCUIT

The purpose of testing is to verify functionality and ratings of power equipment. This inherently implies that if a test object did not fullfill the required functionality or ratings, it fails the test. When this happens, a potentially large amount of energy from the short circuit generators can flow in an uncontrolled way which can damage both the test object and the test circuit components. Measures should be taken to protect the capital-intensive equipment of the test circuit, as well as to minimize the damage to the test object to be able to retrace the cause of failure.

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Figure 4-8 shows an AC short circuit generator based test circuit consisting of reduced frequency AC generator with a test object (TO), the HVDC CB, shown inside dashed box. The circuit contains three protective measures which will be discussed one by one:

- The master breaker (MB)
- The triggered spark-gap
- The auxiliary breaker (AB1)

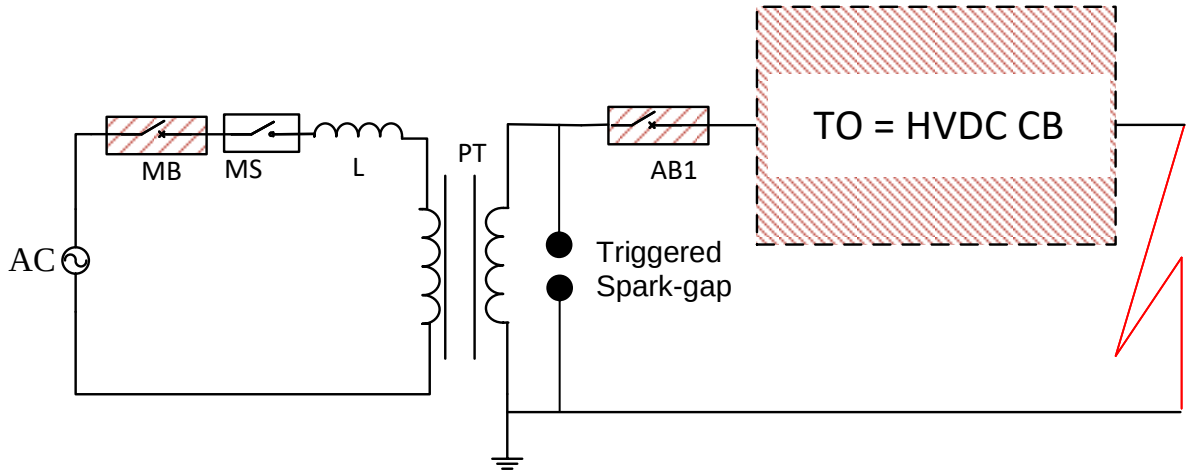

Figure 4-8: Protective measures in test circuit using reduced frequency AC generator

4.2.1 MASTER BREAKER

The master breaker (MB) is located at the low voltage side of the ste-up transformers next to the AC short-circuit generators. Its purpose is to protect the generators from overcurrents and is triggered at a pre-defined time after the making switch is closed. For HVDC CB testing it is intended to interrupt the current at the first current zero after the short circuit is triggered. This will protect the the HVDC CB from subsequent overcurrent in the next cycles, but will not be able to prevent the full prospective test current to flow for at least half a cycle.

4.2.2 AUXILIARY BREAKER

The auxiliary breaker fulfils two functions. It protects the HVDC CB's residual current breaker from overvoltage stress, and it isolates the HVDC CB from the test current source, enabling both overcurrent protection as well as the application of post suppression DC voltage stress.

If the HVDC CB succeeds in interrupting, it should be subjected to a constant DC voltage stress after the current is completely cleared (at t_6 in Figure 3-8). This is shown in the simulation results of D5.3 that after a faulted line is taken out of service in multi-terminal HVDC environment, the HVDC CB is subjected to the system voltage in open position. Therefore, it is necessary to test the dielectric withstand of the HVDC CB after interruption since in practice the system voltage will automatically recover after the fault is cleared. Methods by which to achieve

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this DC voltage stress are discussed in section 4.3. HVDC CBs have a series connected residual current breaker which is needed to interrupt leakage current through surge arresters after the fault current is suppressed. However, when testing HVDC CBs using an AC short-circuit generator, the residual current breaker cannot be used for the purpose of isolating the generator from the HVDC CB since the stress is not realistic because of the polarity reversal of generator voltage which does not happen in a practical system. This is shown in Figure 4-9 as the difference between the black and red lines after the moment of current suppression (t = 18.5 ms). Thus, the test installation has to provide an additional AC circuit breaker serving the purpose of the residual current breaker but with a sufficiently high voltage withstand rating. This breaker is called the auxiliary breaker designated AB1 in Figure 4-8. The auxiliary breaker is set to open during the current commutation period and will arc until the HVDC CB has suppressed the current to zero. At this point the arc will extinguish and separate the HVDC CB from the AC short-circuit current source.

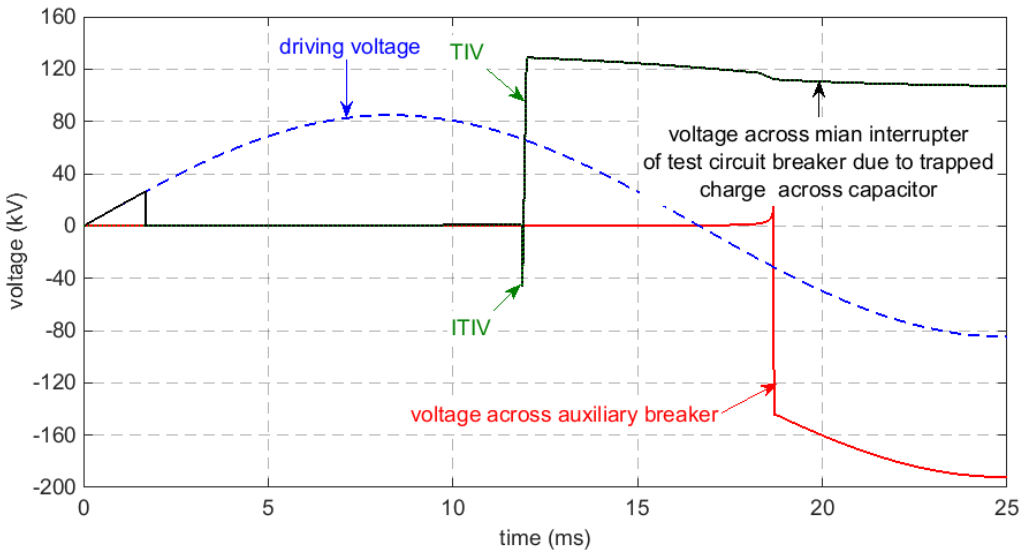

Figure 4-9: Driving source voltage (85 kV, peak), transient interruption voltage (TIV) and voltage across auxiliary breaker during current interruption. – breaker operation time is 2 ms

4.2.3 TRIGGERED SPARK-GAP

In case the HVDC CB fails to break the DC fault current, an uncontrolled situation can arise in which the impedance of the test object is not defined. It could be low or high, and hence result either in the flow of the prospective test current, or potentially in a high voltage. Both cases are potentially dangerous, the first because the HVDC CB may not be able to withstand the prospective peak current (especially in case of power electronic components), and the second because the test circuit may not be able to withstand the high voltage. Both problems can be solved by realising a by-pass for the test current close to the HVDC CB. This can be achieved by a triggered spark-gap.

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The spark-gap can be set to passively avoid overvoltages by adjusting the electrode separation to ensure a breakdown through air will occur at the protective voltage level by taking into account the breakdown strength of air. This protective voltage level should be set sufficiently higher than the TIV of the breaker to avoid any nuisance 'tripping'.

In addition, the spark-gap can be 'triggered' by an external input signal. By using a level detector, the sparkgap can be triggered whenever the current through the HVDC CB exceeds the current level at which it should have interrupted, thus indicating a failure to clear. By triggering the spark-gap, a parallel path to the test object is created. Due to the voltage of the arc in the opened auxiliary breaker in the test object path, the current is commutated into the by-pass path. By doing so, the test object is spared from damage due to a prospective test current, and the contact wear of the auxiliary breaker is limited.

4.3 METHODS FOR THE APPLICATION OF POST SUPPRESSION DC VOLTAGE STRESS

In a practical system, the HVDC CBs are subjected to the DC system voltage stress after current suppression until the residual current breaker opens. Therefore, during the test, it is necessary to provide such a stress immediately after the short-circuit current suppression. Practically, the method to apply, and the timing of, this stress is challenging. Two of the possible methods to supply dielectric stress after current interruption are discussed in this section.

4.3.1 CHARGE TRAPPING

Some HVDC CB concepts, for example the active injection HVDC CB shown in Figure 4-10 have capacitors and inductors as part of the HVDC CB. Typically, when this capacitor is connected in parallel to the surge arrestor, it remains charged during the entire energy absorption period ($t_5 = t_4 - t_5$, in Figure 4-11) to a value equal to the TIV of the breaker and as long as the high speed making switch (HMS) is always connected in parallel with main interrupter after the making switch for counter current injection is closed. This means, if a separate dielectric stress source is used, there will be interaction between the capacitor of the breaker and this additional dielectric stress source even if the short-circuit generators are disconnected.

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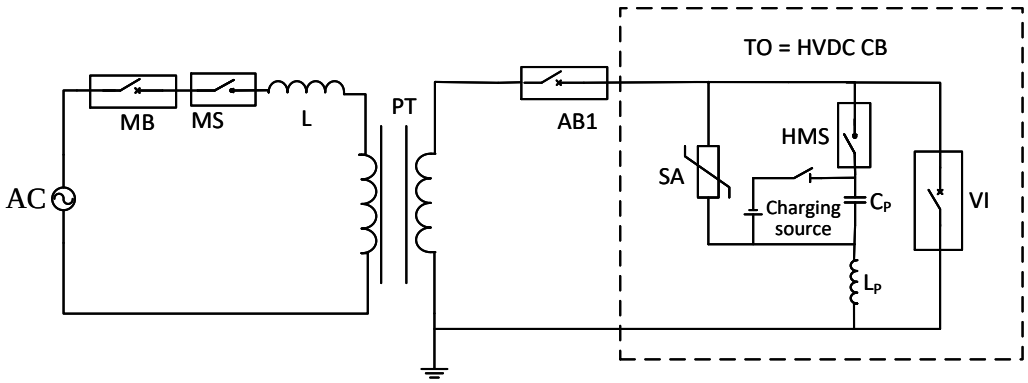

Figure 4-10: configuration of active injection HVDC CB using short-circuit AC generators

Figure 4-11 depicts simulation results of operation of an active injection HVDC CB in a test circuit supplied by a reduced frequency (16 2/3 Hz) AC source (see Figure 4-10). At t_1 a short circuit is applied and this is subsequently followed by a rapidly rising short-circuit current. At t_2 a trip signal is sent to main interrupter to open its contacts. This is followed by arc current between the parting contacts of the main interrupter. At t_3 the main interrupter reaches sufficient separation to withstand the transient interruption voltage (TIV) and as a result the making switch in the L_P-C_P branch is closed to inject counter current through the main interrupter. Since the L_p and C_p are dimensioned to create a counter current higher than the short-circuit current supplied by the generator (system in practice), the resultant current through the main interrupter is forced to cross zero, and hence, creating a chance to extinguish the arc current between its contacts. If the main interrupter fails to extinguish the arc on the first zero crossing, there will be subsequent zero crossings as a result of oscillation at high frequency of L_P-C_P, and therefore, creating more chances for arc extinguishing. Following a current interruption in the main interrupter, the short-circuit current commutates to the L_P-C_P branch and charges the capacitor. The capacitor is charged until its voltage reaches the protection level (TIV) of the surge arrester at t_4. From this moment on the short-circuit current is fully commutated to the surge arrester and since the TIV is designed to be higher than the driving voltage, the short-circuit current is suppressed to zero at time t_5. At this point the capacitor remains charged.

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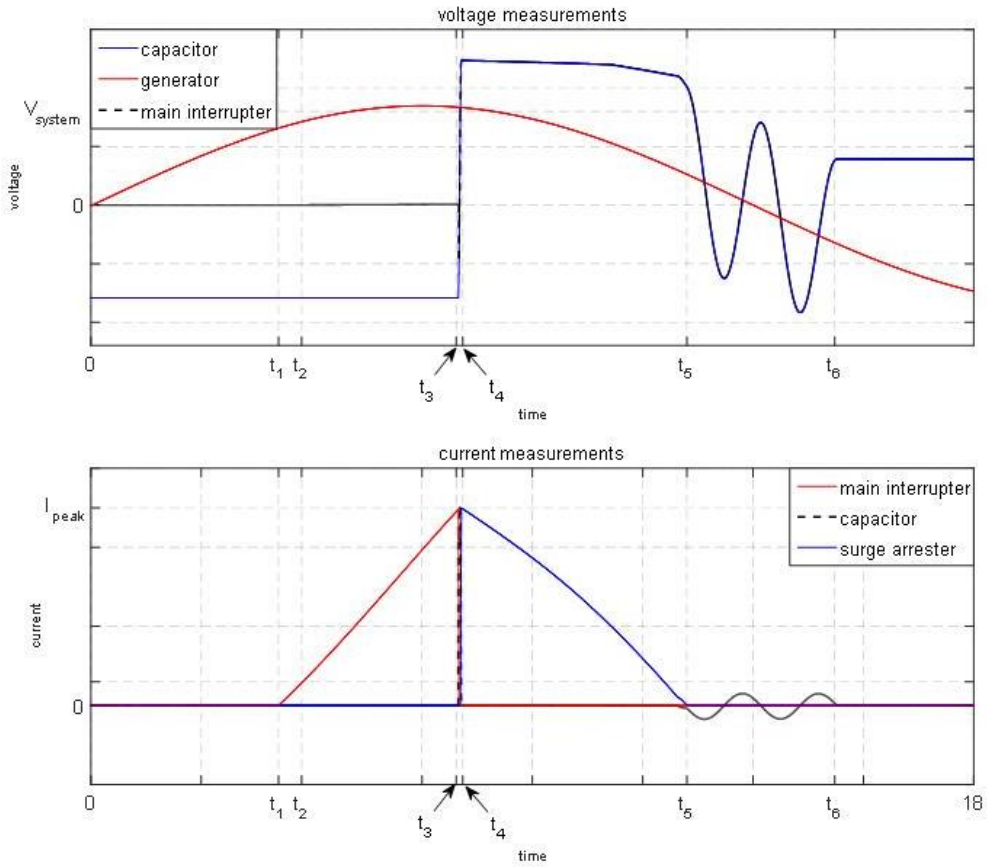

Figure 4-11: Simulation results when auxiliary breaker AB1 disconnects the generator and the TO

An AC circuit breaker (auxiliary breaker) is needed in series with the test breaker to separate the source side from the test breaker immediately after fault current suppression. Without this auxiliary breaker, there will be an oscillation between the charged capacitor of the HVDC CB and the AC generator (as shown in Figure 4-11 between t_5 and t_6) and the test breaker will not be subjected to DC voltage stress after current interruption. One of the drawbacks of using AC generators for testing HVDC CBs is that the auxiliary breaker is subjected to very high voltages right after interruption. The difference of the voltage due to the trapped charge across the capacitor of the HVDC CB (considering active injection HVDC CB) and the voltage of the generator appear across the auxiliary breaker. Since the voltage of the AC generator changes its polarity (see Figure 4-9) while the voltage due to the trapped charge across capacitor remains the same, the sum of the magnitudes of these two voltages appears across the auxiliary breaker. Figure 4-9 shows this situation where the driving voltage of the generator, the transient interruption voltage and voltage across the auxiliary breaker for the case when generator voltage having peak value of 85 kV is used. It can be seen from this figure that the voltage across the auxiliary breaker jumps to a value equal to the difference between the TIV and the driving source voltage.

Note that, the capacitor and the surge arrester are connected in parallel and hence, the voltage across the capacitor is determined by the surge arrester voltage. When the surge arrester voltage slightly reduces as a result of the decrease in short-circuit current (because of the inherent I-V characteristics), the capacitor C_p discharges to the surge arrester. Once the short circuit current is suppressed to zero or to residual current level,

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the surge arrester does not play a significant role. Rather, the L_P-C_P branch starts interacting with the driving source which results in the oscillation that can be seen between t_5 and t_6 in Figure 4-11 if no measure is taken to avoid it. In practice the HVDC CB has a residual current breaker which operates after the short-circuit current is interrupted. The speed and time of operation of the residual breaker is not clearly specified yet and could be in the order of 100 milliseconds.

Another important observation from the simulation result shown in Figure 4-11 is that the test circuit cannot maintain the dielectric stress after current interruption. Depending on the speed of operation of the residual breaker, there might be trapped charge across the capacitor C_p which provides dielectric stress. A method on how to make use of the capacitor C_p to supply dielectric stress after short-circuit current interruption is discussed below.

As explained in the previous section, the capacitor C_p is charged to a voltage level equal to the protection level of the surge arrester if the main interrupter succeeds in extinguishing the arc after counter current injection. If the auxiliary breaker AB1 is tripped in advance, it opens at the moment of current suppression and the source side is disconnected from the TO side the moment the short-circuit current is interrupted by the TO. This makes it possible to use the voltage across the capacitor C_p as a source of dielectric stress on the main interrupter. Figure 4-12 shows a simulation result when AB1 isolates the source from the TO at t_5. It can be observed from Figure 4-12 bottom graph that the TO interrupts the short circuit current at t_5. If AB1 is pre-ordered to trip just before this time, it can isolate the source (generator) from the test object at t_5. This results in a trapped charge across the C_p and as a result the voltage across C_p provides dielectric stress to the main interrupter after the short-circuit current is successfully interrupted. The voltage across the capacitor is slightly decaying as it is discharging through the surge arrester and parasitic resistances.

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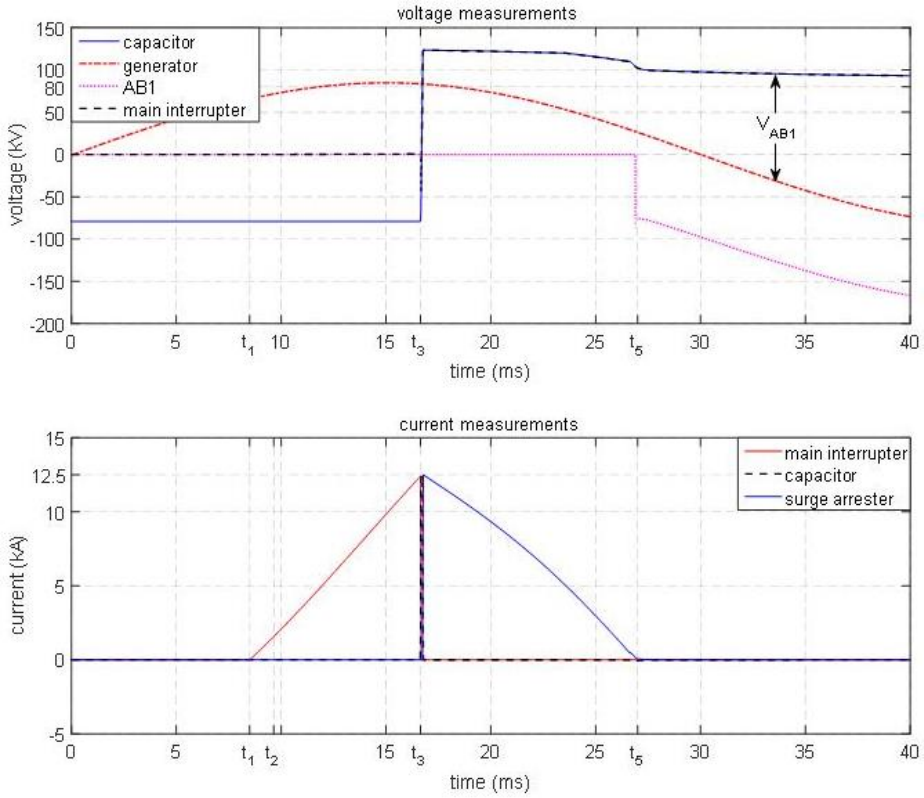

Figure 4-12: Simulation result when AB1 isolates the generator side from TO side by the time a short-circuit current is suppressed to zero

Some practical challenges are inevitable when using this method. The first is the speed of the auxiliary breaker AB1. In order to gain sufficient dielectric strength, the trip order must be sent to AB1 well in advance and this results in continuous arcing until the current is suppressed to the residual value by the TO. This results in wear of the auxiliary breaker and reduces the test current due to the series arc voltage. To compensate for the reduction of test current due to arcing in the AB1, the magnitude of driving voltage can be slightly increased, depending on the extinguishing medium used. The second challenge is the voltage across AB1 which is shown by the dotted magenta curve in Figure 4-12 top graph. It can be seen that AB1 must be able to withstand a voltage as high as 2.5 times the rated voltage of the HVDC CB.

The other major challenge (rather risk) is the fact that AB1 is subjected to long arcing in case the TO fails to interrupt. This can damage AB1 especially because the arc duration is longer due to reduced frequency source. Concurrently, the prospective peak fault current may well exceed the short-circuit current withstand rating of the test object. This is alleviated by adding the level-detector triggered spark-gap by-pass discussed in section 4.2.3.

For other types of HVDC CBs such as hybrid types, a separate source such as a charged capacitor can be used to supply dielectric stress. However, this shall be accurately timed probably based on circuit current measurements such as current zero crossing, as discussed in the next section.

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4.3.2 EXTERNAL DC TEST VOLTAGE SOURCE

Compared to other test circuits, such as charged high-voltage capacitor circuits, reduced frequency AC generators offer more flexibility. The making angle and frequency can be optimized for sufficient di/dt during a fault, for breaker operation time as well as for sufficient driving voltage during the energy dissipation period. However, since the driving voltage is supplied by the AC generator, it is difficult to provide sufficient dielectric stress (which is a constant DC voltage in practice) following the current suppresion process. Nevertheless, a test circuit must be designed to be able to provide sufficient stress following current interruption. Theoretically, this can be achieved by a separate second source for dielectric stress as shown in Figure 4-13, but practically the instant as well as the method of connecting the second source poses several challenges.

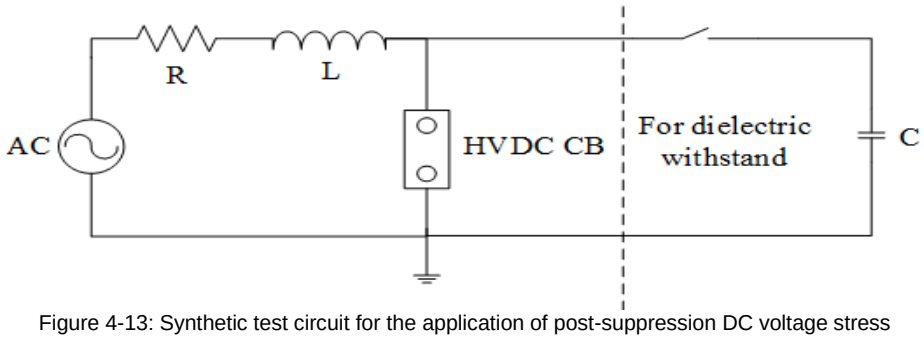

Figure 4-13: Synthetic test circuit for the application of post-suppression DC voltage stress

In testing AC circuit breakers using synthetic method, the injection of the second source is accurately timed in reference to the natural zero crossing of a short-circuit current. For HVDC CBs, however, the surge arrester must first suppress the short-circuit current to zero or below certain leakage current. Unlike the zero crossing in AC systems which can be known in advance, the exact time at which the current is suppressed to zero (leakage current) in DC current interruption depends on several factors such as characteristics of the surge arrester, the magnitude of the driving voltage, the total system inductance, etc., which can be approximated by the following equation [19]:

$$i_s = \frac{L}{R}\ln\left(1 + \frac{R}{U_{CB} - U_C} I_p\right) \quad (6)$$

Where, t_s is the total time required by the surge arrester to suppress the peak fault current (I_p) to zero (a small leakage current). U_{CB} is the TIV generated by an HVDC CB during current interruption and U_C is the instantaneous value of the driving voltage (generator back emf in this case). L and R are the total circuit inductance and resistance respectively. A high-speed level detector or a naturally commutated power electronic switch may be used to achieve accurate timing.

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5 MODULAR & MULTI-PART TESTING

Due to the limitations of testing facilities, it may be challenging to perform full pole testing on HVDC CBs, such as those rated at 320 kV or higher in which case one single test source is unlikely to be able to satisfy all test circuit requirements directly. In order to perform reasonable and economical tests, practical testing methods such as unit testing, synthetic testing and multi-part testing can be considered. In this case, it is considered that unit testing, like that prescribed in the international standards of ACCB testing and similar to modular testing as described in the international standards for VSC valve testing, may be applied to HVDC CBs composed of several units connected in series and/or in parallel. This effectively reduces the test object, assuming the stresses are distributed predictably, resulting in prorating of the test object's capabilities. Synthetic testing can be applied to supply different types of stresses by different sources, typically sequenctially separated. Finally, multi-part testing may be applied to functional units or components (according to the terminology discussed in D5.3) of an HVDC CB to verify ratings and functionality of an HVDC CB on a subpart level. The latter may be combined with synthetic testing, and requires a thorough analysis of the stresses which each part may experience during DC urrent interruption operations.

5.1 TESTING METHODOLOGIES

Based on the short-circuit generator method, the flow chart shown in Figure 5-1 demonstrates the process used to decide the appropriate testing method. First, it will be evaluated if full duty can be applied directly. If this is not possible, synthetic test methods may be applied. These are described in more detail in Section 5.2. In the case that it is difficult to apply full stress with synthetic methods, multi-part and unit test methods can be used. These are described in more detail in Sections 5.3 and 5.4.

The approach given here allows flexibility, in the case of high energy dissipation. Due to limitation of the testing facilities with a direct test, these practical methods may be applied. In the following sections, more detail of synthetic, multi-part and unit testing is given, in the context of HVDC CB testing.

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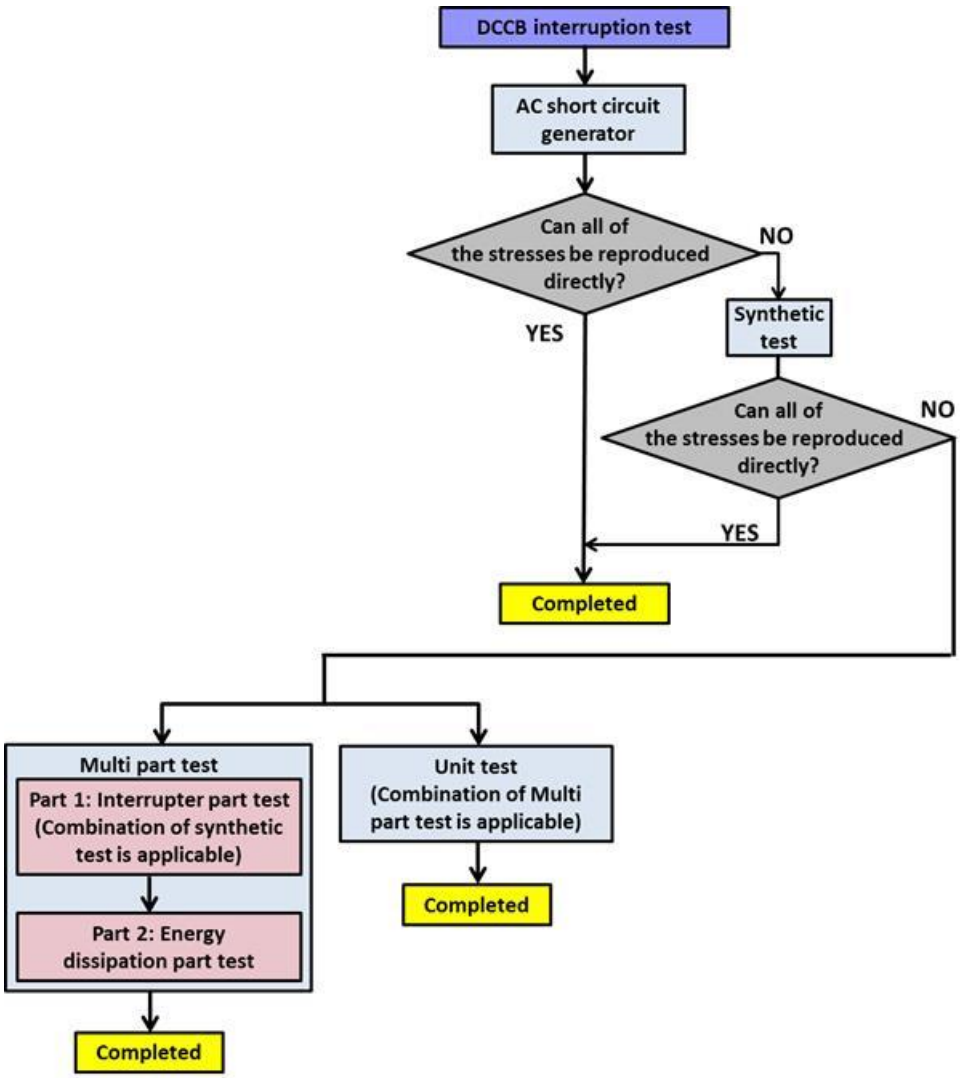

Figure 5-1: HVDC CB testing methodologies

5.2 SYNTHETIC TESTING

Due to restricted availability of testing facilities with a direct test capability, a synthetic testing method with an additional power source besides the short-circuit generator is often used for short-circuit breaking tests with EHV-AC circuit breakers. A similar approach was adopted in section 4.3.2 to achieve post-suppression DC voltage stress. It is envisaged that in some high-energy dissipation cases, it may not be possible to reproduce full interruption and energy dissipation stresses in a single test. In this case, synthetic testing may also be applied. In this case, the synthetic test circuit provides supplementary energy to the main test circuit (short-circuit generator, for example).

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5.2.1 PROPOSED CIRCUIT AND OPERATION

In this section, a synthetic method of compensating insufficient stress (similar to that used in equivalent testing of AC circuit breakers) is presented. In the case of HVDC CB testing, supplying large amounts of energy from a single source can be challenging, for which synthetic testing may be a solution. Figure 5-2 shows the proposed test circuit, where a voltage source is added to supplement the energy dissipation in the MOSA. The synthetic source consists of a pre-charged capacitor, spark gap and reactor. Pre-charged voltage is higher voltage than the clamping voltage of MOSA to ensure conduction [of the MOSA] when the circuit is operated.

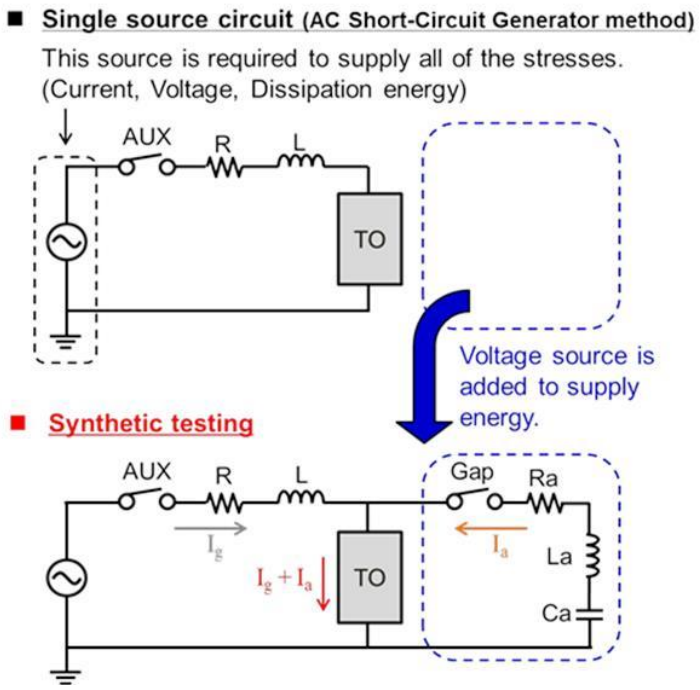

Figure 5-2: Synthetic testing method concept

Illustrative waveforms of the synthetic test are shown in Figure 5-3Figure 5-3: Illustrative synthetic testing waveforms. Black lines show the target; grey lines are those without synthetic circuit operation, which is supplied from the current source (I_g); orange lines show the contribution from the voltage source (I_a); red dotted lines show the contribution from the synthetic source (I_g+I_a) The detailed explanation is as below:

i) The synthetic testing starts from AC short-circuit generator method. Current interruption and MOSA operation is same as Section 3.4 “AC short circuit generator method” (I_g). However, the current source is unable to supply the full energy, which results in a premature current zero. (See and compare the black and grey line in Figure 5-3)

ii) During the MOSA operation time, a gap is triggered and the capacitor C_a is discharged.
As a result, charge from the capacitor C_a is injected into the MOSA, which prolongs the MOSA dissipation time. This means that MOSA dissipation energy is increased.

iii) The auxiliary breaker isolates the test object from the current source after current zero, which causes the recovery DC recovery voltage being applied to the TO.

iv) This results in full energy being dissipated.

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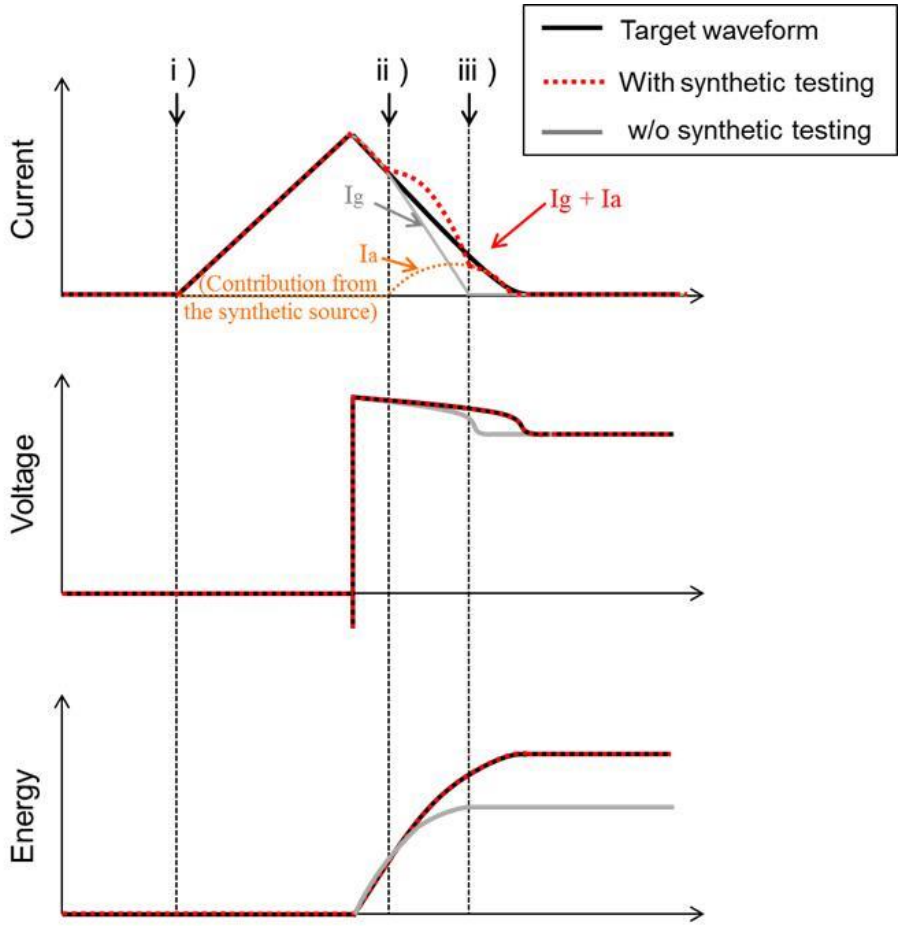

Figure 5-3: Illustrative synthetic testing waveforms

5.2.2 SIMULATION RESULTS

The simulation result of synthetic testing, reproducing target B of Figure 2-3 is shown Figure 5-4 and the list of parameters is shown in Table 5-1. The short-circuit generator frequency was set to 30 Hz and 80 kV peak. The target waveforms are shown in black; without synthetic circuit operation in grey and with synthetic circuit operation in red. The capacitor and current source currents are superimposed to give the total current through the TO (red current trace), which prolongs the energy dissipation time and increases the total energy dissipation. The results show, this method can be used to reproduce the waveforms given in Target B successfully.

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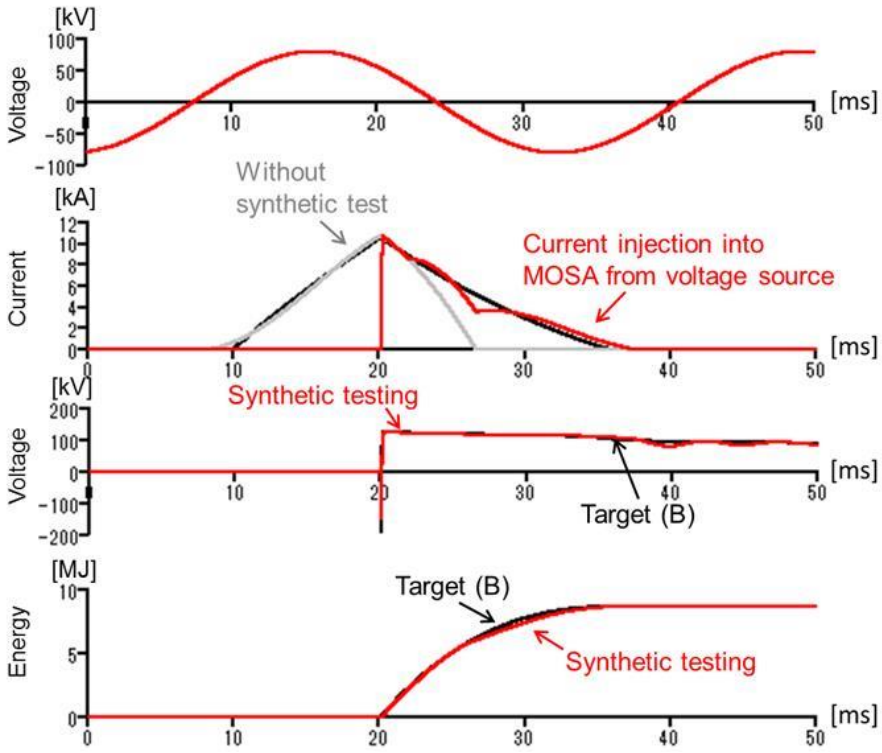

Figure 5-4: Simulation results comparing the synthetic test circuit with target B (30 Hz)

Table 5-1: Synthetic Test Circuit Simulation Parameters

Parameter	**Synthetic Test**	**Target B**
C_a[μF]	300	-
V_{ca}θ[kV]	200	-
L_a[mH]	60.0	-
R_a[Ω]	10.0	-
Frequency of current source[Hz]	30	-
Peak Current[kA]	10.6	10.5
Energy Dissipated[MJ]	8.7	8.7
Energy dissipation time [ms]	18.0	16.0

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5.3 MULTI-PART TESTING

If all requirements for test HVDC CB cannot be met simultaneously, the test may be carried out in two successive parts. This is described as multi-part testing, specified in international standard for AC circuit breaker testing (IEC 62271-100).

When test facilities' capabilities restrict reproduction of all stresses at the same time, a multi-part approach can be an economical and reasonable method for HVDC CBs, also. In this approach, different functionalities of the HVDC CB are verified in separate tests. For example, current commutation and energy absorption maybe demonstrated in two different tests, enabling a lower generator voltage to be used (when compared to that required for a full test).

If there is no correlation between the performance of interrupter and the MOSA energy dissipation performance each part test can be operated completely independently (with a small overlap) not continuously. Test circuits applicable for each part of the test can be applied separately (i.e. for interruption and energy dissipation), as shown in Figure 5-5. The two test parts (interruption and energy dissipation) are described in the following sections.

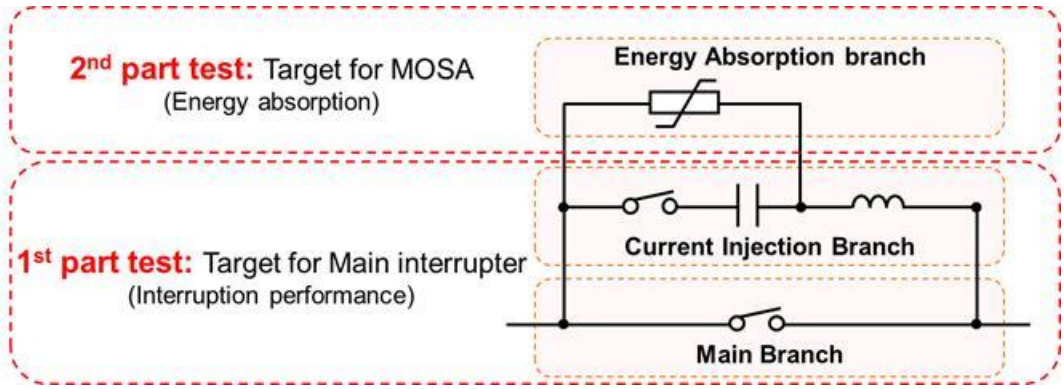

Figure 5-5: Concept of multi-part testing for HVDC CB

For hybrid HVDC CBs, DC bus arrangements in which several feeders share one main breaker through several disconnectors and commutation switches are possible. In this case, separate testing i.e. functional testing, of the components in these parallel paths is necessary.

5.3.1 1ST PART: INTERRUPTION PERFORMANCE

It is important to reproduce the TIV across the HVDC CB, for all test methods. As the multi-part method results in shorter energy dissipation time, a synthetic circuit is used (as shown in Figure 5-6: left, short circuit generator; right, synthetic circuit to extend voltage application time). This artificially extends the TIV period to accurately evaluate the breaker's performance. Although the MOSA dissipating energy duty is out of scope in this part, a full scale MOSA should still be implemented to ensure accurate TIV.

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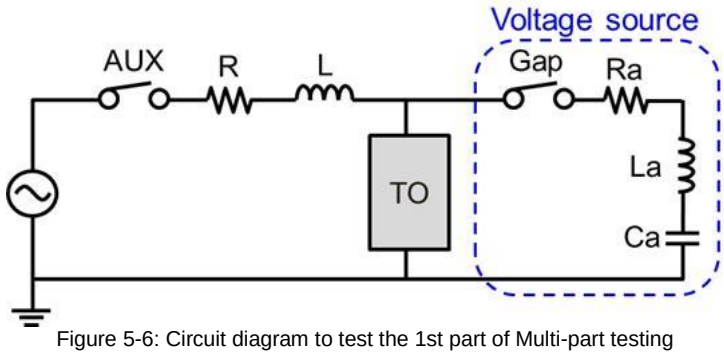

Figure 5-6: Circuit diagram to test the 1st part of Multi-part testing

Simulation results are shown in Figure 5-7 and parameter is listed in Table 5-2. Source voltage is reduced to 50 kV for this example case, when compared to the fully synthetic case in Figure 5-4. This demonstrates the reduced requirements on the testing facilities that are possible through multi-part testing. The results demonstrate that the synthetic circuit can reproduce the TIV magnitude and length successfully, reproducing that from the real system target waveform. Energy dissipation is lower than the target, as expected (which is evaluated during the second part).

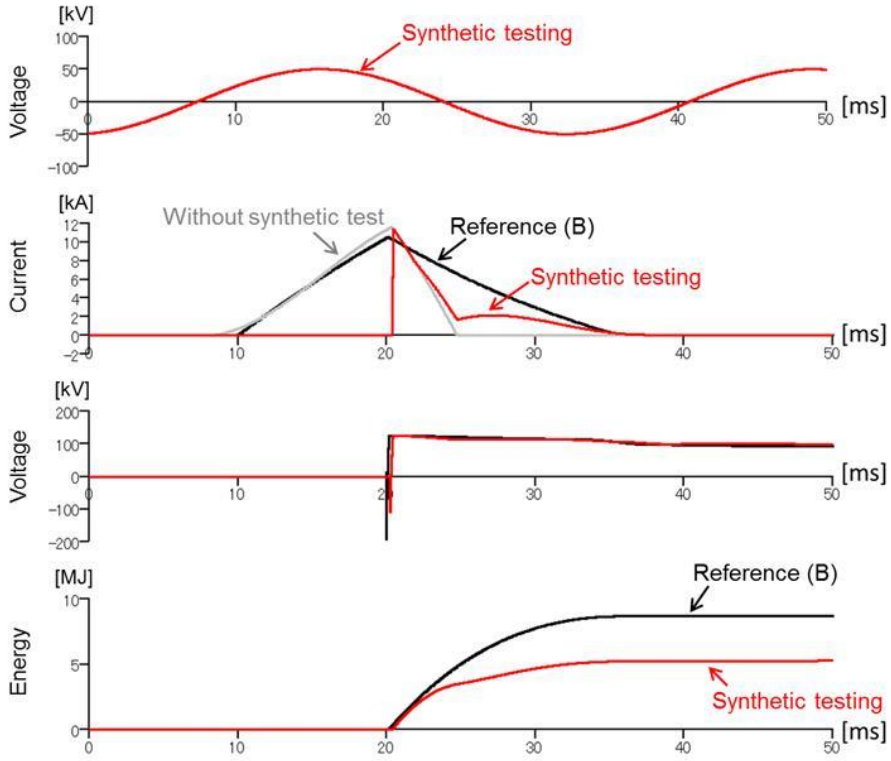

Figure 5-7: 1st part (interruption performance) (30 Hz)

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Table 5-2: Synthetic Test Circuit Parameters of 1st part of the Multi-part testing

Parameter	Synthetic Test	Target B
Vs(kVpeak)	**50**	
C_a[μF]	300	-
V_{ca}[kV]	160	-
L_a[mH]	50.0	-
R_a[Ω]	10.0	-
Frequency of current source [Hz]	30	-
Peak Current[kA]	11.3	10.5
Energy Dissipated[MJ]	5.2	8.7
Energy dissipation time [ms]	18.3	16.0

5.3.2 2ND PART: MOSA ENERGY DISSIPATION PERFORMANCE VERIFICATION TEST

In the 2nd part of the multi-part testing, the MOSA energy dissipation performance is tested. Energy is supplied to the MOSA by AC short circuit generator – see Figure 5-8. This can be at commercial or reduced frequency, as required. The test can be operated completely independently from 1st part test, as long as the interrupter part does not effect on MOSA energy dissipation performance.

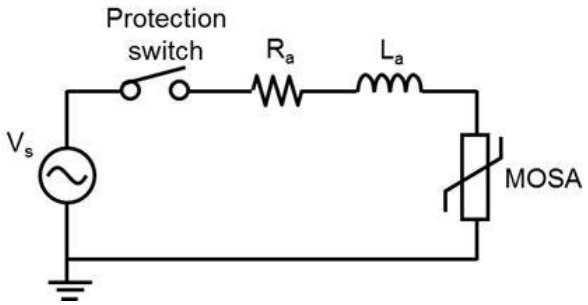

Figure 5-8: Circuit diagram for 2nd part MOSA (energy dissipation performance)

The 2nd part test should provide equivalent energy stress to the MOSA, as expected during operation. That is, it should provide the same magnitude of energy, over the same duration as Figure 2-2. Using the circuit shown in Figure 5-8, the source impedance can be adjusted to control the magnitude of current flowing to the MOSA. The protection switch is used to control the duration of this current flow (to the nearest current zero, i.e. half-cycle). By controlling these two variables, the equivalent energy can be supplied to the MOSA.

Figure 5-9 shows the simulation results of the 2nd part of multi-part testing, where a 50Hz generator is used to supply energy. The parameter list is shown in Table 5-3. An 80 kV HVDC CB MOSA, with an energy dissipation capability of 8.7 MJ is assumed. The simulation results demonstrate how combinations of current magnitude

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(controlled by series inductance) and duration can be used to control the total energy dissipation and time duration.

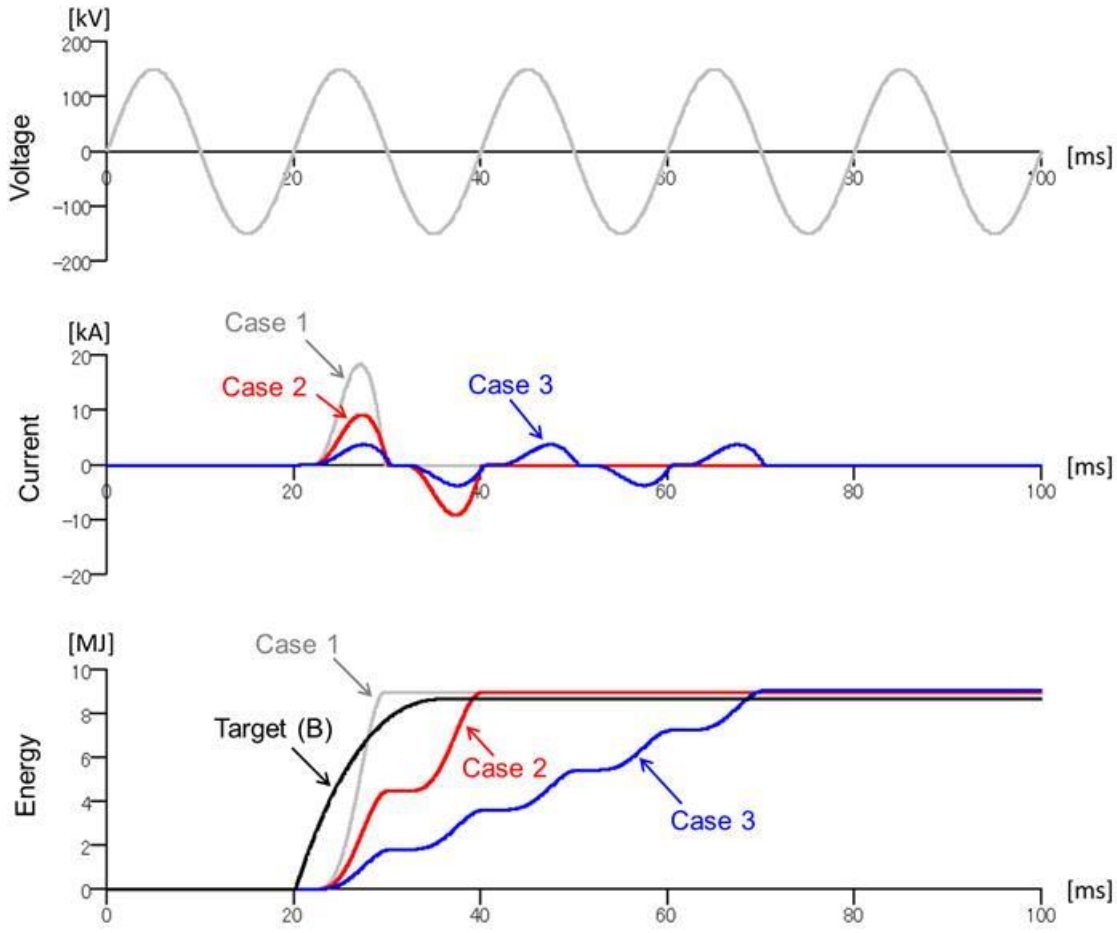

Figure 5-9: 2nd part for MOSA (energy dissipation performance)

Table 5-3: 2nd part of the Multi-part testing

Parameter	**Target**	**Case 1**	**Case 2**	**Case 3**
Source frequency [Hz]	-	50	50	50
Source voltage [kVpeak]	-	150	150	150
Peak Current[kA]	-	18.4	6.1	3.7
L_a[mH]	-	6.5	25.0	44.0
R_a[Ω]	-	0.01	0.01	0.01
Energy Dissipation [MJ]	8.7	9.0	8.9	9.1
Energy dissipation time [ms]	16.0	10.0	20.0	50

It remains to be verified if this method sufficiently replicates the high energy stress on the surge arrestors during DC current interruption.

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5.4 UNIT TESTING

In this section, unit testing for HVDC CBs is discussed, using the AC short-circuit generator method. A rated voltage of 320 kV and four units connected in series are assumed.

5.4.1 UNIT TESTING [BASIC APPROACH]

Within D5.3, all simulations were performed at full system voltage – i.e. 320 kV. However, in WP10 the HVDC CBs will be tested at the prototype level in the range of 80–100 kV. Thus, the assumed performance requirements, shall be scaled to the lower voltage and energy levels. The scaling up from prototype to full-pole voltage level typically involves series connection of modules or components, as shown in Figure 5-10, and thus, the main current through the HVDC CB remains the same. However, voltage and energy dissipation are reduced proportionally as shown in Figure 5-11.

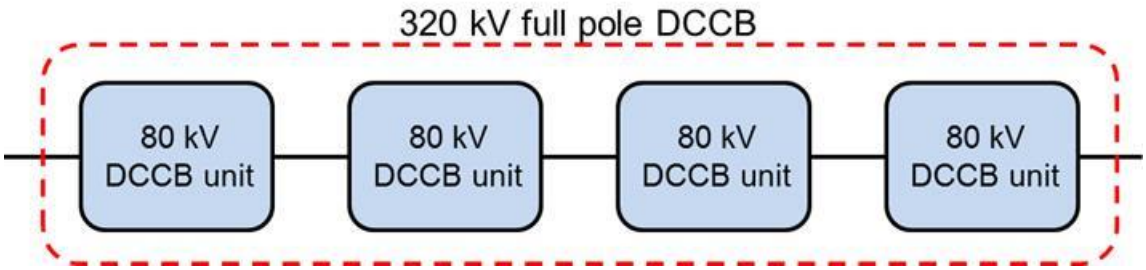

Figure 5-10: HVDC CB modular arrangement for full-pole voltage

Figure 5-11 shows target waveforms (current, voltage and energy) for a single HVDC CB unit as compared to full-pole HVDC CB. Note that magnitude of the current remains the same for a single unit and full pole HVDC CB. However, the voltage and energy are scaled down proportional to the number of modules used to make up the full-pole HVDC CB assuming equal distribution of voltage. The latter assumption is reasonable in case the modules do not have common surge arrestors as the voltage across each module is determined by the TIV of the units' surge arrestors. Slight differences in timing of current interruption between different units can result in different amounts of energy being absorped by different modules which needs to be accounted for the prorating of the energy stresses to be supplied to a single module. In case the HVDC CB does not consist of the series connection of identical units, but contains elements common to all, i.e. full-pole, then when using a unit testing approach, the impedance of the full pole loop of the omitted units must be taken into account in the test set-up. More in general, the actual construction of the HVDC CB (live or dead tank, one or multiple support structures, etc.) must be considered to determine if modular testing is feasible and meaningful.

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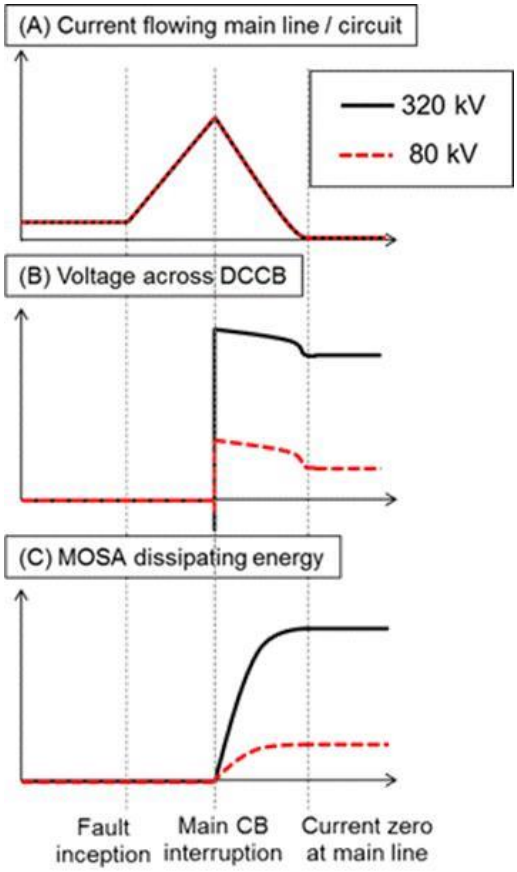

Figure 5-11: Diagram showing a prorating of stresses (current, voltage and energy) from full-pole breaker to a single unit (80kV)

The test methods should be designed to match the assumed HVDC CB stresses as much as possible. To do this, time-domain target waveforms for current, dissipated energy and voltage are used, when comparing candidate test methods. Each of the test methods can then be judged on how readily they can match each of these target waveforms.

Figure 5-12 shows a simplified circuit that is used to generate the target waveforms for the prototype HVDC CB. With appropriate choice of source voltage, series resistance (R_{ref}) and inductance (L_{ref}) based on operation times, target waveforms can be scaled for various technologies of HVDC CBs as desired.

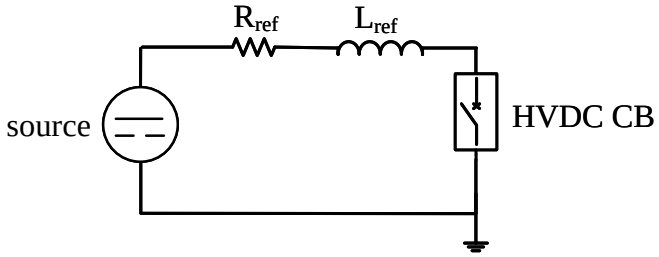

Figure 5-12: key parameters of a test circuit that should be scaled for testing of HVDC CB prototype

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For energy absorption capability, the range of tests can be carried out by varying the magnitude of the driving source voltage and current limiting reactor. Similarly, current interruption from nominal (or even lower current) to the maximum current interruption capability shall be performed. This is important to verify the characteristics and the design of the surge arresters for HVDC CB application.

This test is performed in the same way as that described in Section 3.4. Test circuit parameters (voltage, making phase, etc.) may be adjusted to control the key waveforms, as previously demonstrated.

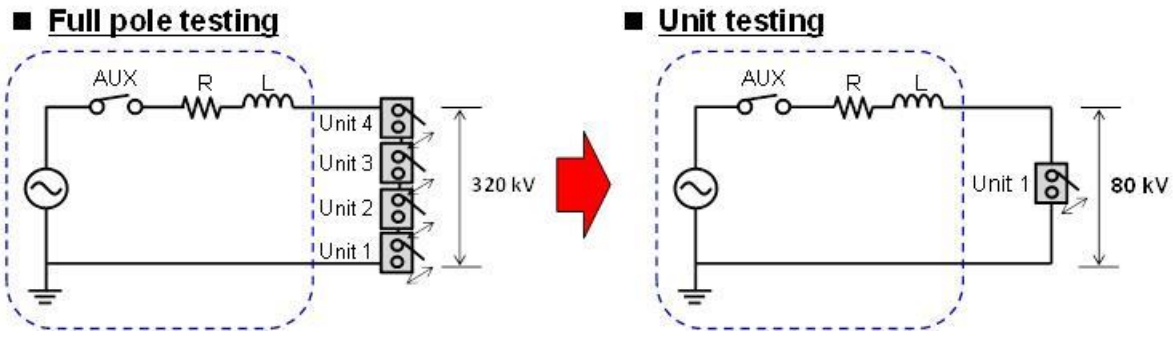

Figure 5-13: Concept of unit testing using AC generator method

5.4.2 UNIT TESTING [WITH SYNTHETIC TEST]

In the case of the unit test also, the synthetic test shown in Section 5.3.2 is applicable (Figure 5-14). By applying a combination of the synthetic test and unit test, it is possible to increase the total energy dissipation.

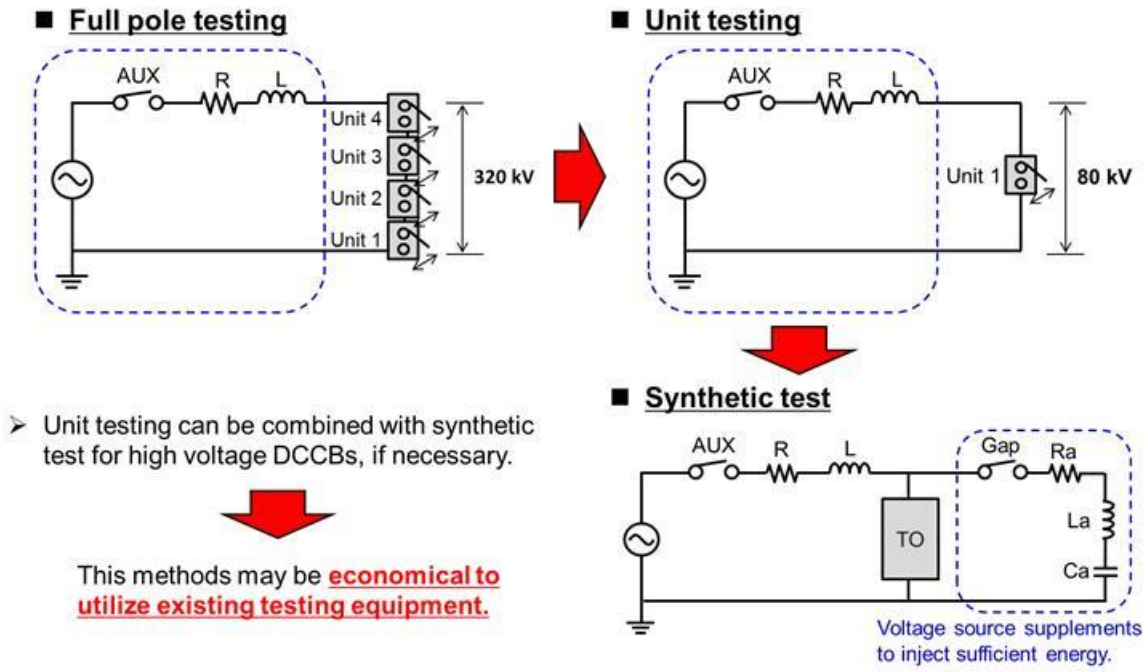

Figure 5-14: Concept of Unit testing with synthetic testing

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5.4.3 UNIT TEST APPLYING A MULTI-PART TEST

When it is difficult to reproduce all the stresses which are required for a breaker unit by only a single test using AC short circuit generators, the combination of unit test and multi-part test can be considered. In this case also, by separating the test into 1st part test (which verifies interruption performance of one interrupter unit) and 2nd part test (which verifies energy dissipation performance of MOSA) all stresses are reproduced equivalently and applied to the test breaker. This is similar to the principles demonstrated in Section 5.3.

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6 CONCLUSION

Based on the stresses which are exerted onto HVDC circuit breakers during DC fault current breaking operations, requirements for test circuits in which DC short-circuit current breaking capability is to be verified, have been presented. Four hypothetical test circuits based on a controlled rectifier, a charged capacitor, a charged inductor, and an AC short-circuit generator operated at reduced frequency, have been qualitatively discussed and compared to the test circuit requirements.

It is concluded that only a controlled rectifier circuit could directly synthesize all necessary stresses but is likely to be prohibitively expensive and complex at the required power ratings and functionality. Depending on the charging circuit, the charged reactor method may prove to be unsuitable for testing hybrid HVDC circuit breakers. Both the charged capacitor and AC short-circuit generators are capable of producing a suitable DC short-circuit test current. However, AC short-circuit generators offer the possibility to deliver high energy stresses, which may be unpractical to achieve using a charged capacitor circuit, due to the large required capacitance. The latter is especially relevant for testing HVDC circuit breakers with long breaker operation times.

It is shown that AC short-circuit generators operated at reduced frequency offer flexible control of the rate of rise of test current, and the amount of energy delivered to the HVDC circuit breaker by carefully chosing the generator frequency, the test circuit impedance, the generator source voltage magnitude, and the making angle. The AC characteristic implies that an inherent limitation exists on testing HVDC circuit breakers with long breaker operation times, as the entire fault neutralisation time must be less than the longest possible half wave period of the applied test current.

A method to protect the test object and the test circuit from damage in case the HVDC circuit breaker fails to operate correctly, has been presented. A high-speed level-detector triggered spark-gap, combined with an auxiliary breaker can by-pass the prospective test current and isolate the test object from the test source.

Apart from the controlled rectifier circuit, none of the discussed test sources is capable of supplying DC voltage stress after interruption without additional measures. In case of AC short circuit generators, it is shown that for HVDC circuit breakers with active current injection, it is possible to achieve DC voltage stress by trapping charge in the injection capacitor, or otherwise by injecting a DC voltage stress from an external DC voltage source.

Finally, it is recognized that no practical test circuit can supply the required stresses to directly test EHV full-pole HVDC circuit breakers. Some suggestions for verifying performance of a modular part of a breaker i.e. unit testing, or separately verifying different functionalities i.e. multi-part testing and realising different stresses from different test sources i.e. synthetic testing are discussed.

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7 APPENDIX

Although the main objective of this document is to compare test circuits used for DC current interruption tests, the following table summarizes whether these test circuits can be used other types of tests prescribed in D5.4.

Table 7-1: Comparison of test circuits for type test program of HVDC CB

TEST CIRCUITS	**HVDC CB TESTS**					
	Operational tests		Dielectric tests		Making and breaking tests	Repeated operation (e.g. reclosing)
	Short-time Current withstand	temperature rise	Lightning	DC withstand		
RECTIFIER	Suitable[1]	Suitable	Not suitable	Suitable	Suitable	Suitable
CHARGED CAPACITOR	Partially Suitable[2]	Not suitable	Not suitable	Suitable	Suitable	Not suitable
CHARGED REACTOR	Partially suitable	Not suitable	Not suitable	Not suitable	Suitable only for breaking	Not suitable
AC SHORT-CIRCUIT GENERATOR	Partially suitable	Not suitable	Not suitable	Not suitable	Suitable	Partially suitable (only for longer reclosing time)

[1] Can be designed with availability of components
[2] Can be used with additional circuits

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