Design, Modeling and Control of Hybrid DC Circuit Breaker Based on Fast Thyristors

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***Abstract*--This paper presents a systematic study on designing hybrid direct current (DC) circuit breaker (CB) based on fast thyristors. As an illustration, the DC CB main parameters are calculated for a 120kV, 1.5kA test breaker with interrupting current of 10kA. The studies indicate that the opening time of 2.3ms can be achieved only if fast thyristors are employed. It is further illustrated that there is a design tradeoff between minimum interrupting current capability and discharge time for the internal capacitors (reclosing speed). The DC CB control system for opening and closing is presented based on different levels of protection and the self-protection. The DC CB is modelled in PSCAD and simulation results are used to evaluate the breaker performance under different operating conditions. It is concluded that the model represents well the DC CB and can be employed for DC grid protection studies. It is further shown that opening time becomes longer as interrupting current reduces, and it is very long in case of load current interruption.**

***Index Terms*-- DC grids, Protection, Hybrid DC circuit breaker, Fast thyristor.**

I. Introduction

THE increasing interest in remote renewable energy resources and more reliable transmission systems lead to an emerging demand for multi-terminal high voltage direct current (HVDC) systems and DC grids [1]. The DC grid concept requires new methods for DC fault detection and DC fault isolation [4]-[2]. Fast and low-loss DC circuit breakers are essential technology to facilitate reliable DC grids.

High voltage DC Circuit Breakers have recently been developed and prototype tested at voltages around 100kV [4]-[7]. There are three main groups of DC CB: mechanical DC CBs [8],[9] which have operating time of around 7-10 ms, IGBT-based hybrid DC CBs [4] with operating time around 2-3 ms, and thyristor based hybrid DC CBs [6],[10], [11] which operate within 2-5 ms.

The mechanical DC CB has been modeled in [9], and simulation results have shown good accuracy. The IGBT-based hybrid DC CB is modelled in [12], and the model has proven to be adequate for DC grid development studies [13].

A prototype of thyristor DC CB has been tested at 120 kV, 6 kA in Twenties EU project recently, but only a single test is reported in [6]. Except for the patent disclosure document [11], not much information on the technology and the model has been reported. The component stresses, design methods or control system are not disclosed.

The main breaking branch in this technology uses thyristors and the operating principle is substantially different from IGBTs in [4]. In particular, thyristor has no turn-off capability and therefore circuit design should ensure reverse voltage of adequate duration at each turn off. Since multiple branches are used, it is important to understand the DC CB control circuit. Furthermore, considering that commutation between branches is conditional on capacitor voltages [6], it is expected that the opening speed will be dependent on the magnitude of the interrupting current.

This paper aims at understanding design principles, modeling and control for fast thyristor-based hybrid DC CB. A model will be developed on PSCAD which should represent essential properties of this technology in the timescale of few milliseconds, and for wide range of operating conditions. It should also indicate possible interaction with the DC grid in open, closed or transient states. The study also aims understanding the need for self-protection in this technology.

The design principles of the DC CB are described firstly in section 2. Section 3 presents self-protection of this DC CB based on fault current magnitude and semiconductors temperature. Section 4 describes the opening and closing control sequences. Simulation results and model verification are given in section 5 and the conclusion is drawn in section 6.

II. Design of thyristor-based Hybrid DC CB

A. DC CB Topology

Fig. 1 shows the structure of thyristor-based DC CB [6]. It consists of three principal branches; normal current branch, main breaker branch and energy absorption branch.

The DC CB test system has voltage rating of 120 KV, current rating I_{DCN}=1.5 kA, peak interrupting current I_{fpk} =10 kA and the fault interruption time is desired to be T_{int}≈2.5 ms in accordance with the prototype performance in [6].

B. Normal current branch

The normal current branch is composed of an ultra-fast disconnector (UFD) S_1, a load commutation switch (LCS) and a surge arrester SA_{T1}.

A typical trip sequence and corresponding current and voltage curves are illustrated in Fig. 2. The important time instants are labeled on the time axis, including T_{int} definition.

A DC fault is applied at t_0 and a trip order is generated at t_1. The LCS is opened immediately and the thyristor valves Tr_1

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and Tr_{11} are fired simultaneously. This transfers the fault current to the first time-delaying sub-branch.

An open command is sent to the UFD S_1 once its current falls below the residual chopping current. The UFD S_1 is assumed to have closed resistance of 1 mΩ, residual chopping current I_{res_UFD}=2 A and mechanical time delay T_{mec}=2 ms [14].

The current rating of the LCS should be higher than rated current of 1.5kA. The voltage rating for valve LCS should be higher than the clamping voltage of surge arrester SA_{11}. A matrix configuration of 3x3 IGBTs is usually selected for LCS to reduce the ON resistance (and hence the power loss) and to increase both current and voltage ratings [15]. One suitable IGBT for LCS could be the module 5SNA 2000K450300 (4500 V and 2000 A). Therefore, the current and voltage ratings of LCS are obtained respectively as 6 kA and 13.5 kV. Each IGBT is equipped with an RCD snubber circuit to limit dv/dt. It is noted that LCS cost is modest because of low voltage rating, and rating can be increased readily.

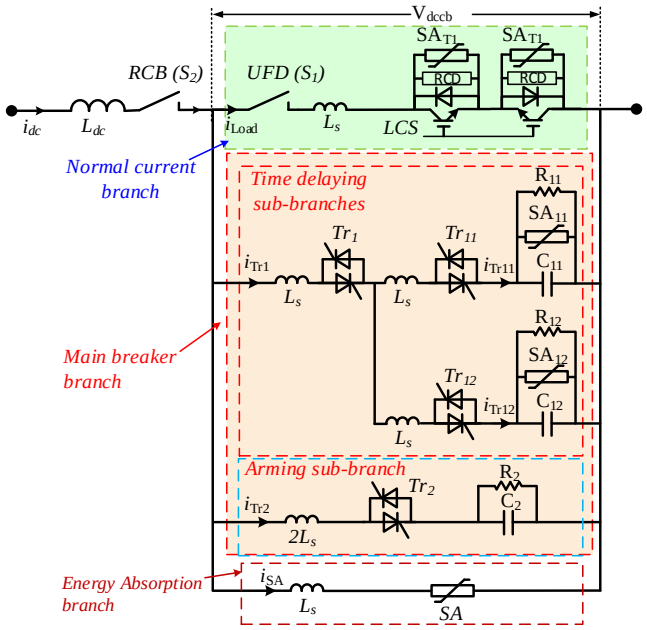

Fig. 1. Structure of thyristor-based hybrid DC CB

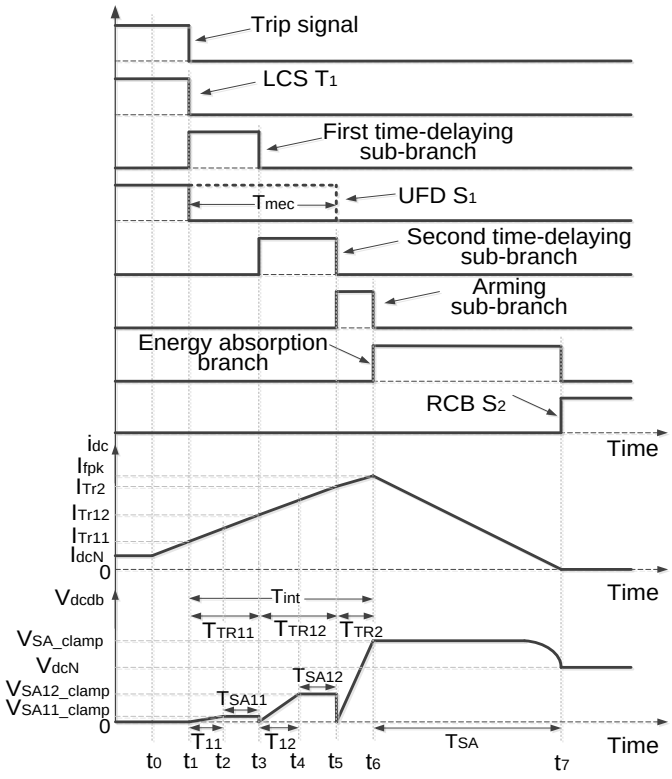

Fig. 2. Trip sequence of thyristor-based hybrid DC CB and corresponding current and voltage curves.

The surge arrester SA_{T1} is required to keep the voltage across LCS at a safe level below its rated value. Therefore, the clamping voltage of SA_{T1} is selected as V_{SAT1_clamp}=11 kV.

A stray inductance L_s=30 μH is included in this branch. The stray inductance is also included in the other branches but with higher value because of more components, longer harness and larger mechanical structure [16]. The commutating loop overall stray inductance is around 100 μH [17].

C. Main breaker branch

1) Operating sequence

The main breaker branch is composed of the two time-delaying and the arming sub-branches. The first time-delaying sub-branch takes over fault current from LCS/S_1 by firing Tr_1 and Tr_{11}. This charges C_{11} and keeps the voltage across S_1 low enough while it is opening. When the sub-branch capacitor C_{11} charges to close to clamping voltage of surge arrester SA_{11} (V_{SA11_clamp}), the thyristor valves Tr_1 and Tr_{12} are fired. This commutates fault current to the second time-delaying sub-branch.

When the UFD S_1 is fully opened and the voltage across capacitor C_{12} rises up to V_{SA12_clamp}, the thyristor valve Tr_2 is fired. The arming branch builds up further the TIV (Transient Interruption Voltage) and then transfers the fault current to the energy absorption branch.

Each sub-branch has two conducting intervals:

1. While capacitor is charging, voltage is rising,
2. When voltage reaches clipping voltage of the local arrester, voltage stays constant, as seen in Fig. 2.

2) Thyristor valves Tr_1, Tr_{11}, Tr_{12} and Tr_2

Each thyristor valve is composed of series connected modules which are selected based on rated voltage, surge non-repetitive current (I_{TSM}) and extinction time (T_q).

The number of series thyristors (N) in T_{r2} is selected as:

$$N * V_{Tr\_rated} \geq 1.5 * TIV_{\max} \quad (1)$$

where V_{Tr_rated} is the rated voltage of thyristor module and TIV_{max} is the maximum TIV which is equal to the clamping voltage of the arrester in the energy absorption branch.

The extinction time T_q of the thyristor has significant impact on the fault interruption time and the size of the capacitors. Two types of thyristor modules could potentially be used; phase control and fast thyristors. Phase control thyristors have high current and voltage ratings and are always used with converters of HVDC ratings. They however have long extinction time, in the order of several hundreds

microseconds which would require large size of the capacitors banks. It will be shown later that the required fault interruption time (T_{int}=2.5 ms) can only be achieved if fast thyristors with extinction time of several tens microseconds are selected.

The main breaker branch thyristors conduct for few ms. Therefore the surge non-repetitive current (I_{TSM}), which is defined on a 10 ms half-sine, is most relevant for selecting thyristors. Note that I_{TSM} is non-repetitive and results in high thyristor temperature, which should be considered when repeated open/close DC CB operations are required.

One suitable fast thyristor module could be 5STF 28H2060 with rated voltage 2000 V, average on-state current of 2667 A, peak non-repetitive surge current of 46.5 kA and extinction time of T_q=60 μs. This is one of the largest available fast thyristors. According to (1), the valve Tr_2 would be composed of 135 fast thyristor modules, which will bring challenges of voltage sharing and simultaneous control. Considering that the maximum voltage across valves Tr_{11}/Tr_{12} (equivalent to V_{SA12_clamp} as discussed later) is 44% of TIV_{max}, this determines sharing of number of thyristors. Therefore, valve Tr_1 is selected a stack of 75 while each valve Tr_{11}/Tr_{12} have 60 thyristor modules.

3) Surge arresters SA_{11} and SA_{12}

The voltage rating of the surge arrester SA_{11} should be well below the voltage rating of the surge arrester SA_{T1} to ensure the fault current commutates to the first sub-branch. Therefore the clamping voltage of SA_{11} is selected V_{SA11_clamp}=7 kV. This value keeps the current in S_1 below I_{res_UFD} even if the voltage of SA_{11} hits the clamping voltage before the contacts of S_1 have begun separation. The design assumes that T_{r12} is fired as soon as V_{11} reaches SA_{11} clamping voltage and therefore conduction time of SA_{11} is minimal. The energy requirement is small E_{SA11}≤11 kJ.

The clamping voltage of the SA_{12} is selected between the clamping voltage of SA_{11} and the energy absorption surge arrester SA. The design in this paper will be optimized to reduce the interruption time. As studied in the next section, higher V_{SA12_clamp} leads to lower capacitor in the arming branch and therefore faster operating time. Too high value however will result in too long charging time and higher costs. The recommended tradeoff is: V_{SA12_clamp} = 80 kV.

4) Capacitors C_{11}, C_{12} and C_2

A minimum value of the capacitance C_{11} is determined based on the opening speed and voltage dielectric breakdown strength of UFD. If the UFD withstands DC nominal voltage plus 50% overvoltage and the contacts fully separate linearly in T_{mec}=2 ms, the voltage slope across the contacts would be 90,000 kV/s. Therefore, neglecting parasitic inductances, C_{11} can be calculated to ensure that dv_{C11}/dt<90V/μs:

$$C_{11}\frac{dv_{C11}(t)}{dt}=i_{Tr11}(t)-\frac{v_{C11}(t)}{R_{11}}-i_{SA11}, t_1<t<t_2 \tag{2}$$

where $i_{SA11}=f(v_{C11}(t))^q$ is the current of the SA_{11} and all other labels are defined in Fig. 1 and Fig. 2. The maximum dv_{C11}/dt happens at the initial instant $t=t_1$ when v_{C11}=0 and therefore the last two terms in (2) are neglected. Considering conservatively that highest current magnitude at t_1 is I_{Tr11}=8 kA, a capacitance C_{11}>100 μF satisfies the voltage slope requirement. With this capacitance the charging time of C_{11} is:

$$T_{TR11}=\frac{V_{SA11\_clamp}C_{11}}{I_{TR11}} \tag{3}$$

which gives around 80μs at rated conditions. It is noted that the conduction time of the two time-delaying branches is given by the mechanical time of UFD: T_{TR11}+T_{TR12}=2 ms. As discussed below, the second time-delaying branch has conducting time T_{TR12}=1.5 ms and therefore the required time of first sub-branch is T_{TR11}=0.5 ms. To ensure that capacitor voltage V_{c11} reaches V_{SA11_clamp} in 0.5 ms a value C_{11}=500 μF is obtained. The voltage rating of C_{11} is selected as: V_{C11_rated}=1.5*V_{SA11_clamp}.

The value of capacitance C_{12} is determined based on

1. The voltage derivative as in (2), and
2. The extinction time of the Tr_{11} thyristor module, which is a more demanding condition.

As seen in Fig. 2, firing valve Tr_{12} brings the thyristor valve Tr_{11} under reverse recovery process and keeps it so long as v_{c12}<V_{SAT1_clamp}. This condition should last longer than the thyristor extinction time T_q.

If the currents through R_{12} and SA_{12} and reverse recovery thyristor current are neglected, with reference to Fig. 2 the voltage v_{C12} can be expressed in two separate intervals:

$$\frac{dv_{C12}(t)}{dt}\approx\frac{i_{Tr12}(t)}{C_{12}},\begin{cases} t_3<t<t_3+T_q, & 0<v_{C12}<V_{SA11\_clamp} \\ t_3+T_q<t<t_4, & V_{SA11\_clamp}<v_{C12}<V_{SA12\_clamp}\end{cases} \tag{4}$$

Considering the first time interval, which is essential for reverse recovery of T_{r11}, and the extreme peak fault current at t_3 I_{Tr12}≈8.5 kA, with 50% margin 1.5*T_q=90 μs, a capacitance of C_{12}>110 μF is obtained. Simulations on PSCAD with all parasitic parameters indicates that C_{12}=190 μF is required. The voltage rating of capacitor C_{12} is: V_{C12_rated}=1.5*V_{SA12_clamp}. The C_{12} charging time to voltage V_{SA12_clamp} =80kV with I_{Tr12}=8.5 kA is obtained as 1.5ms using (3).

Capacitor C_2 charges outside the UFD operating time and therefore it impacts the total operating time. Considering that it provides reverse voltage across T_{r12}, the design equation in interval t_4<t<t_4+T_q is:

$$C_2=\frac{1.5T_qI_{Tr2}}{V_{SA12\_clamp}} \tag{5}$$

Assuming I_{Tr2}≈9.5 kA, this equation gives C_2>11 μF and PSCAD simulation with all parasitic components recommends C_2=13 μF with rated voltage 1.5*V_{SA_clamp}. Using similar formula as in (3) the C_2 charging time to voltage V_{SA_clamp}=180 kV, with current I_{Tr2}, is obtained as 0.24 ms.

The above formulae (3) and (5), indicate that higher V_{SA12_clamp} will give lower T_{TR2} and faster overall DC CB operation. This implies increase in T_{TR12} requiring reduction in T_{TR11} which can be achieved by reducing C_{11}. Nevertheless any further increase in V_{SA12_clamp} over 80kV would bring only 10-20 μs improvement in the opening speed, while voltage rating and cost of C_{12} and S_{A12} increases substantially.

The capacitor C_{12} (190 μF, 120 kV) is the largest component in terms of size and weight. Some size reduction can be achieved if a third time-delaying branch is introduced. As an example, if the C_{12} voltage is limited to 30 kV, then a third smaller capacitor will be required C_{13} (40 μF, 100 kV), while the arming branch will also be smaller C_2 (11 μF, 180 kV). However such design would require another thyristor valve T_{r13} and surge arrester and the overall cost would be higher.

5) Discharging resistors R_{11}, R_{12} and R_2

The resistances R_{11}, R_{12} and R_2 are required to discharge corresponding capacitors and prepare DC CB for the next opening sequence. A low resistance value is desired to enable fast capacitor discharge with the view of fast reclosing cycle.

However a too low resistance will prevent capacitor voltage rise above a certain level, and this may prevent commutation to the next branch. Therefore, at low currents capacitor voltage may not rise sufficiently and DC CB may fail to open. The critical value of resistance can be calculated using (2), assuming that voltage reaches $v_{C11}=K_{SA}V_{SA11\_clamp}$ (differential term in (2) becomes zero)

$$\frac{K_{SA}V_{SA11\_clamp}}{R_{11}} + i_{SA11} = I_{Tr11} \tag{6}$$

where $K_{SA}V_{SA11\_clamp}$ ($K_{SA}=0.8$) is the threshold voltage for initiating commutation to the next branch.

Taking that the required minimal interrupting (load) current is $i_{dc}=i_{Tr11}=100$ A and the arrester current is $i_{SA11}=10$ A at voltage $0.8*V_{SA11\_clamp}$ (according to arrester IV characteristics), the value $R_{11}>66$ Ω is obtained. A similar calculation gives $R_{12}>1$ kΩ and $R_2>21$ kΩ. Assuming that all three branches have the same discharging time, PSCAD tuning gives: $R_{11}=0.75$ kΩ and $R_{12}=2.0$ kΩ, $R_2=30$ kΩ. With these resistances, it can be calculated that the capacitors will fully discharge in 1.5 s, which is long time and means that the DC CB is disabled in this interval.

A common reclosing time with overhead lines at 400 kV is 200-300 ms. If we design DC CB taking 200 ms as capacitor discharge time a resistance $R_2=3.8$ kΩ is obtained. With this resistance, DC CB cannot interrupt current below 1.0 kA. Therefore there is a trade-off between reclosing time and minimal interrupting current. This problem can be eliminated altogether if additional semiconductor switches are introduced to connect/disconnect discharge resistors (not used in [11]). In such case DC CB could interrupt very low currents and small resistors can be used for very fast discharge.

The peak power dissipation in R_{11} is 65 kW at voltage $V_{SA11\_clamp}=7$ kV. The energy dissipation in R_{11} in one cycle is:

$$E_{R11} \approx \frac{V_{C11\_clamp}^2}{3R_{11}}T_{11} + \frac{V_{C11\_clamp}^2}{R_{11}}T_{SA11} + \frac{C_{11}V_{C11\_clamp}^2}{2} \tag{7}$$

The first two terms of E_{R11} are negligible compared to the third term. Considering the design values, $E_{R11}\leq 12.5$ kJ is obtained.

Similarly, the peak power dissipation in R_{12} and R_2 are respectively 3.2 MW and 1.1 MW. Considering the design values, $E_{R12}\leq 610$ kJ and $E_{R2}\leq 210$ kJ are obtained.

D. Energy absorption branch SA

The energy absorption branch includes a number of series and parallel surge arresters.

Once the capacitor C_2 charges above V_{SA_clamp}, the fault current commutates to the energy absorption branch. The SA clamping voltage is commonly selected to be 1.5 times of the nominal DC line voltage ($V_{SA\_clamp}=180$ kV), which ensures sufficiently fast reduction in the line current.

The energy absorption branch conducts for duration T_{SA} while the line current decays gradually from peak fault current I_{fpk} to zero. Assuming that the V_{SA} stays constant at V_{SA_clamp} for T_{SA} interval, T_{SA} is obtained:

$$T_{SA} = I_{fpk}L_{dc}/0.5V_{dc} \tag{8}$$

The energy dissipation in the main SA can be approximated by integrating its power across T_{SA} as:

$$E_{SA} = \int_{t_6}^{t_7} v_{SA}i_{SA}dt \approx 1.5I_{fpk}^2L_{dc} \tag{9}$$

Assuming $I_{fpk}=10$ kA and $L_{dc}=100$ mH the SA energy is 15MJ, and therefore SA capacity is selected as $E_{SA}=22.5$ MJ.

E. Residual current breaker S_2 and series inductor L_{dc}

The residual current breaker (RCB) S_2 is a low-rated vacuum switch with closed resistance of around 5mΩ, residual chopping current $I_{res\_RCB}=10$ A and mechanical delay $T_{res}=30$ ms.

The series inductor L_{dc} is used to limit the rate of rise of fault current. A minimum value for L_{dc} is given by

$$L_{dc} = \frac{V_{dc}}{\left(\Delta i_f/\Delta t\right)} > \frac{V_{dc}}{\left(\left(I_{fpk}-I_{dcN}\right)/T_{\text{int}}\right)} \tag{10}$$

Assuming rated values, $L_{dc}>35$ mH is obtained. To avoid converter blocking, and also to satisfy DC grid protection discrimination requirements, a larger value of $L_{dc}=100$ mH is selected. Table I summarizes the design with fast thyristors.

Table I
Design parameters of fast thyristor-based hybrid DCCB

Branch	V_{SA_clamp} and E_{SA}	Capacitors	Resistors
LCS (T_1): 3x3 IGBTs	$V_{SAT1\_clamp}=11$ kV $E_{SAT1\_rated}=6$ kJ	---	---
Tr_1: 75x1 Tr_{11}: 60x1 Thyristors	$V_{SA11\_clamp}=7$ kV $E_{SA11\_rated}=15$ kJ	$C_{11}=500$ μF 10.5 kV	$R_{11}=0.75$ kΩ 100 kW,18 kJ
Tr_{12}: 60x1 Thyristors	$V_{SA12\_clamp}=80$ kV $E_{SA12\_rated}=300$ kJ	$C_{12}=190$ μF 120 kV	$R_{12}=2.0$ kΩ 4.8MW, 0.9MJ
Tr_2: 135x1 thyristors	$V_{SA2\_clamp}=180$ kV $E_{SA2\_rated}=21$ MJ	$C_2=13$ μF 270 kV	$R_2=30$ kΩ 1.6MW, 300kJ
$L_{dc}=0.1$H	LCS S_1: ($T_{mec}=2$ ms, $I_{res\_UFD}=0.002$ kA) RCB S_2: ($T_{res}=30$ ms, $I_{res\_RCB}=0.01$ kA)		

F. Design with phase control thyristors

For completeness and comparison, Table II summarizes the design with phase control thyristors ABB 5STP 48Y7200 (7200V, 4840A, $T_q=700$μs). The size of capacitors C_{12}, C_2 and corresponding discharging resistors are much higher which results in unfavorable volume and weight. Because of larger

T_q, the fault interruption time with the same peak interrupting current of 10 kA is over 15 ms.

These results lead to recommendation that fast thyristors should be used in the main breaker branch.

Table II
Design parameters of phase thyristor-based hybrid DCCB

Branch	V_{SA_clamp} and E_{SA}	Capacitors	Resistors
LCS (T_1): 3x3 IGBTs	V_{SAT1_clamp}=11 kV E_{SAT1_rated}=6 kJ	---	---
Tr_1: 19x1,Tr_{11}: 19x1 Thyristors	V_{SA11_clamp}=7 kV E_{SA11_rated}=15 kJ	C_{11}=500 μF 10.5 kV	R_{11}=15 kΩ 4.8 kW, 18 kJ
Tr_{12}: 19x1 Thyristors	V_{SA12_clamp}=80 kV E_{SA12_rated}=380 kJ	C_{12}=1200μF 120 kV	R_{12}=6.0 kΩ 1.6 MW, 5.7 J
Tr_2: 38x1 thyristors	V_{SA2_clamp}=180 kV E_{SA2_rated}=38 MJ	C_2=250 μF 270 kV	R_2=30 kΩ 1.6 MW, 6 MJ
L_{dc}=0.15H	LCS S_1: (T_{mec}=2 ms, I_{res_UFD}=0.002 kA) RCB S_2: (T_{res}=30 ms, I_{res_RCB}=0.01 kA)		

III. DC CB Self Protection

A. Self-protection requirements

If current was allowed to exceed rated peak interruption current or rated load current, component damage would occur and interruption may not succeed [12]. Therefore DC CB self-protection will be considered in models since it can interfere with grid protection systems. The DC CB self-protection may be activated for DC faults in case that DC grid protection fails to send trip signal, in the following cases:

1. If normal branch current approaches rated breaking current (IGBT turn-off capability). This may happen for undetected low-impedance fault.
2. If temperature of semiconductors in normal branch approaches maximum allowed temperature. This may happen for undetected high-impedance fault.
3. If current in the main breaker branch approaches rated breaking current. Too high current would impact reverse voltage and reduce reverse recovery time which may result in DC CB failing to open.

B. Self-protection based on fault current

The self-protection should monitor the line current and trip the DC CB if the current approaches I_{trip_sp}. The trip level I_{trip_sp} is calculated internally considering DC CB operating time T_{int} and self-protection current I_{pk_sp} which is selected not higher than the peak interrupting current ($I_{pk\_sp} \le I_{fpk}$),

$$I_{trip\_sp} = I_{pk\_sp} - T_{int} V_{dc} / L_{dc} \tag{11}$$

Tripping the DC CB at I_{trip_sp} guarantees that the current in the main breaker branch will not exceed the maximum interrupting current considering all internal delays.

The foremost limit on the peak current is the reverse recovery time for thyristors. It will be shown in the simulation section that the designed DC CB in Table I cannot interrupt the fault current higher than 11.7 kA, even though the thyrsitor temperature is well below the thermal limit.

C. Self-protection based on semiconductor temperature

The self-protection should calculate the junction temperature of IGBTs in LCS and trip the DC CB if destruction is expected (temperature exceeds 120 ºC).

The junction temperatures of the IGBT/thyristor switches are calculated based on the thermal model shown in Fig. 3. The thermal impedance Z_{thJC} (between junction and case) is composed of four parallel first order filters. The gains (R_i) and time constants (τ_i) are given in the datasheets of the switches.

The parameter K_{CH} represents the case-heatsink thermal impedance. It is selected as K_{CH}=1.25 for LCS which conducts normal load current and uses water cooling. For the thyristor switches that conduct transient fault current and use air cooling system, it is selected as K_{CH}=1.0.

The environment temperature is represented by T_0. It is selected as 40ºC for LCS with water cooling system and 35ºC for thyristor valves with air cooling system.

The power loss P_{loss} for the IGBTs and thyristors is:

$$\begin{aligned} P_{loss\_IGBT}(t) &= V_{CE0\_IGBT} \cdot i_{IGBT}(t) + R_{ON\_IGBT} \cdot i_{IGBT}^2(t) \\ P_{loss\_Tr}(t) &= V_{CE0\_Tr} \cdot i_{Tr}(t) + R_{ON\_Tr} \cdot i_{Tr}^2(t) \end{aligned} \tag{12}$$

where R_{on} and V_{CE0} are respectively the ON resistance and forward drop voltage of each IGBT/thyristor switch.

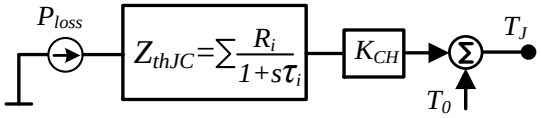

Fig. 3. Thermal model an IGBT/thyristor module

IV. Control of Hybrid DC CB

A. Opening Sequence

The opening sequence starts when the DC CB is in normal operation (LCS and UFD are closed), all capacitors in the main breaker branch are discharged and a trip order (from grid protection or self-protection) is received. The opening sequence that is used in the model is summarized in Table III.

The coefficient $K_{SA} \le 0.8$ enables the DC CB to trip low load current as briefly discussed in section II.C.

Table III
Opening sequence of thyristor-based hybrid DC CB

	Inputs	Action
1	(Is trip order received?) & (All capacitors are discharged?)	Open LCS
2	Is LCS opened?	Fire Tr_1 & Tr_{11}
3	(Is LCS opened?) & ($i_{Load} < I_{res\_UFD}$?)	Open UFD S_1
4	($V_{C11} > K_{SA} * V_{SA11\_calmp}$?)&($T_{Tr11} \ge T_{mec}/4$)	Fire Tr_1 & Tr_{12}
5	(Is UFD S_1 fully opened?) & ($V_{C12} > K_{SA} * V_{SA12\_calmp}$?)	Fire Tr_2
6	$i_{dc} < I_{res\_RCB}$?	Open RCB S_2

B. Closing Sequence

The DC CB can commence closing if it is in open state (LCS and UFD are open), the capacitors C_{12} and C_2 are discharged and a grid order is received. Note that the C_{11} can be either charged or discharged as Tr_1 and Tr_{11} can be turned on even if C_{11} is fully charged. The closing sequence is initiated if grid-level protection sends signal as summarized in

Table IV. If the DC CB had been opened on self-protection, the closing will be disabled.

Table IV
Closing sequence of thyristor-based hybrid DC CB

	Inputs	Action
1	(Is closing order received?) & (Are C_{12} & C_2 discharged?)	Close RCB S_2
2	Is RCB S_2 fully closed?	fire Tr_1 & Tr_{11}
3	(V_{C11} > 0.5*V_{SA11_calmp}?)	Close UFD S_1
3	Is UFD S_1 fully closed?	Close LCS

V. Simulation Results

A. Test system

A test system including a fixed DC voltage 120kV, a DC CB and a purely resistive load 80Ω (all in series) is developed in PSCAD. The system with all parasitic inductances as in Fig. 1 is simulated with parameters given in Table I. The following range of tests is simulated to fully evaluate performance:

- Opening on self-protection at rated current,
- Closing on grid order,
- Opening on grid order with different L_{dc},
- Opening at low currents (fault or load current),
- Opening at currents exceeding rated value,

Only some of the tests results are shown here for brevity.

B. Opening at rated current, by self-protection

A DC fault is applied at t=0.5 s. The trip level I_{trip_sp} is calculated internally based on (11) to have I_{pk_sp}=I_{fpk}=10 kA. Fig. 4 shows the control signals for all switches of the DC CB. Signal Tr_1 is logical OR of signals Tr_{11} and Tr_{12} and therefore is not shown in the figure for brevity. Fig. 5 shows the currents in all branches. The peak fault current is 10 kA and the fault interruption time is 2.3 ms. The RCB S_2 opens T_{res}=30 ms after the current is extinguished.

Fig. 6 shows the DC CB voltages for the same fault. It is seen that the capacitors voltages (v_{C11}, v_{C12} and v_{C2}) rise up to their threshold limit (respectively V_{SA11_clamp}, V_{SA12_clamp} and V_{SA_clamp}) and begin to discharge into their resistors when the fault current commutates to the next branch. The breaker voltage V_{DCCB} rises up first to V_{SA_clamp} and then drops to V_{dcN} (120kV) when the DC CB current becomes zero.

Fig. 7 shows the junction temperature of IGBT valve LCS, and thyristor valves Tr_1 and Tr_2 as the most stressed switches. It is seen that the temperatures are well below the limit 120 ºC. This implies that this DC CB could potentially conduct and interrupt much higher fault current.

The dissipated energies in the surge arresters SA_{T1}, SA_{11}, SA_{12} and the main SA are measured respectively 4.3 kJ, 11 kJ, 210 kJ and 15.3 MJ which are well lower than their rated values that are given in Table I.

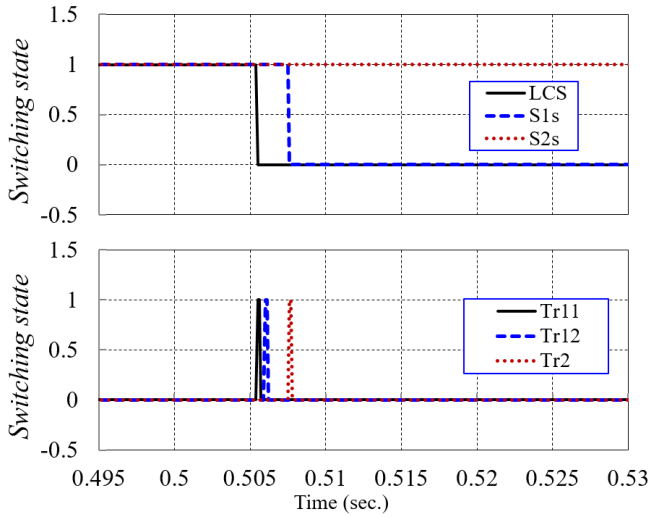

Fig. 4. Switching states (Opening at rated current)

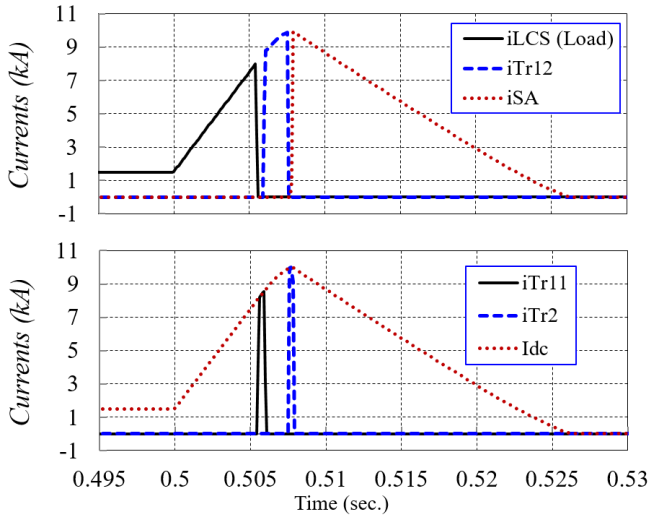

Fig. 5. Branches currents (Opening at rated current)

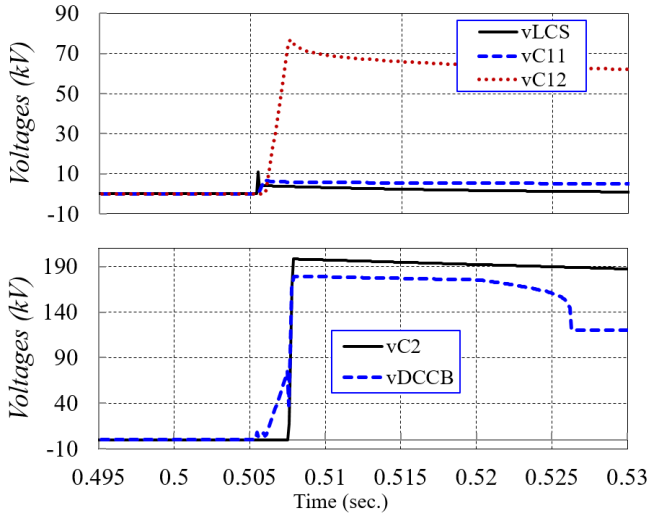

Fig. 6. Capacitors and DC CB Voltages (Opening at rated current)

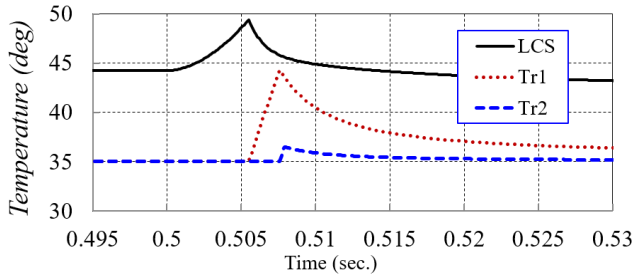

Fig. 7. Junction temperature (Opening at rated current)

Fig. 8 shows the results for the same test case with phase-control thyristors DC CB considering parameter in Table II. It is seen that the fault interruption time is over 15 ms.

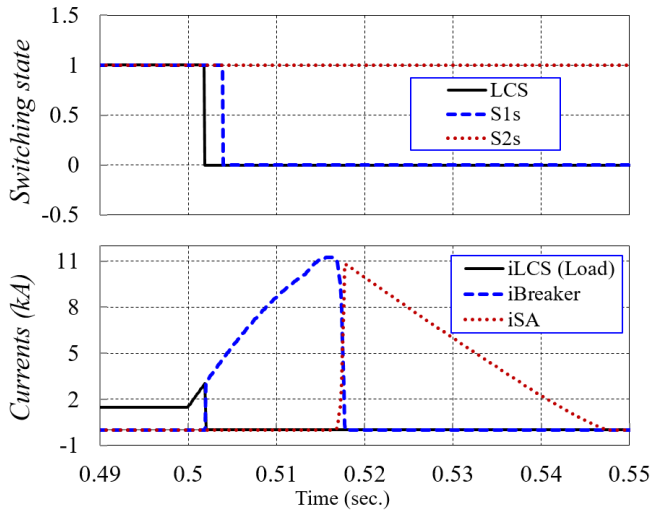

Fig. 8. Switching signals and DC current with DC CB with phase-control thyristors(Opening at rated current)

C. Redesign for 26kA peak interrupting current

In order to examine maximum interrupting current with the given thyristors, the design is revised and temperatures of valve are monitored. For example, the DC CB with C_{11}=500 µF, C_{12}=850 µF, and C_2=38 µF can interrupt peak fault current I_{pk_sp}=26 kA while the junction temperature of IGBT valve LCS and thyristor valve Tr_1 will rise respectively to 92 ºC and 98 ºC. The fault interruption time for this fault current with L_{dc}=100 mH is 3.5 ms. Note that adequate surge arresters and resistors have to be selected. This design indicates possible advantage of thyristor-based DC CB over IGBT-based hybrid DC CB to increase the peak fault current if all other requirements (surge arresters, capacitors and resistors) are provided. Sufficient cooling time should be allowed before next operating sequence begins.

D. Closing on grid order

A closing order under normal operating condition (fault cleared) is issued at t=2 s, and Fig. 9 shows the DC CB switching states, currents and voltages. It is seen that capacitor C_{11} takes load current and voltage v_{C11} builds up until it reaches SA_{11} clipping voltage (7kV). This low voltage enables closing S_1 at zero current while LCS is exposed to an acceptable voltage stress. Once S_1 is closed (after 2ms) LCS is closed and normal current branch takes full load current.

E. Opening on grid order with different L_{dc}

Two simulation tests with two extreme L_{dc} values are performed to investigate the impact of L_{dc} on the DC CB. It is expected that the grid operators may change L_{dc} at some stage to satisfy DC grid protection strategy as DC grid evolves. With this DC CB topology there is concern that passive components (capacitors) can interfere with L_{dc}.

Fig. 10 and Fig. 11 show the branches' currents of the DC CB with two extreme L_{dc} of 500 mH and 40 mH, respectively. The DC fault is applied at t=0.5 s and the grid protection sends trip order when the fault current hits 3 kA (2pu) for both cases.

It is seen that the DC CB works well with these two extreme L_{dc}. The fault interruption time with the high L_{dc} is 3.3 ms while with low L_{dc} it is 2.2 ms. Note that the fault interruption time is around 2.5 ms for this test (trip at 3kA) with L_{dc}=100 mH. The peak interrupting current is higher with the smaller L_{dc} but with shorter opening time as expected.

The dissipated energy in the energy absorption surge arrester SA could be very high if both I_{fpk} and L_{dc} are large, according to (9). For example, L_{dc}=0.5 H and I_{fpk}=10 kA gives approximate dissipated energy in the main SA of 75 MJ.

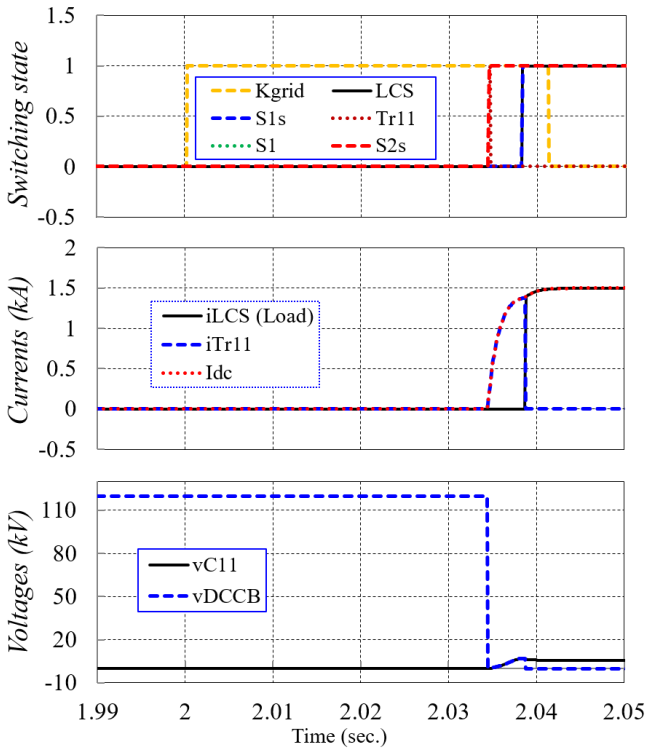

Fig. 9. Switching states, currents and voltages (Closing on grid order)

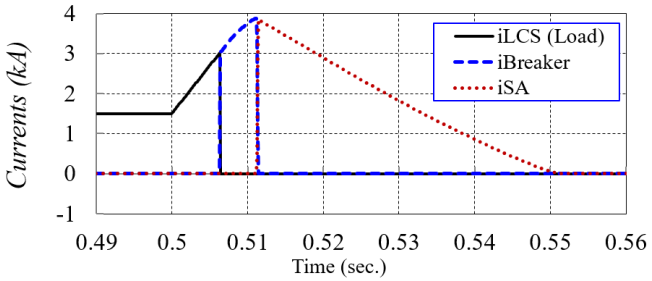

Fig. 10. Branches' currents (Opening on grid order with L_{dc}=0.5H)

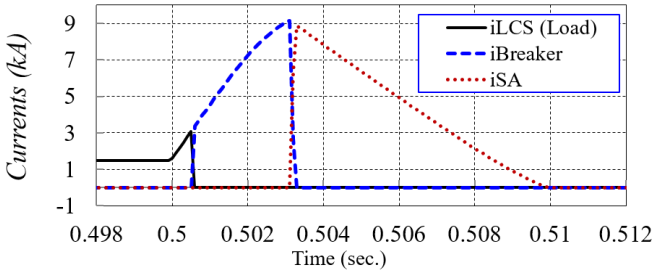

Fig. 11. Branches' currents (Opening on grid order with L_{dc}=0.04 mH)

F. Opening at peak fault current higher than rated

Table V shows the measured reverse recovery time for different peak interrupting currents (I_{fpk}). It is seen that the circuit reverse recovery time is longer than T_q=60 μs if I_{fpk}≤11.7 kA. Because of faster charging of the capacitors, reverse recovery time is shorter than T_q for I_{fpk}≥12 kA and in this case DC CB fails to interrupt fault current

Table V
Reverse voltage time vs peak interrupting current

I_{fpk} (kA)	8	10	11	11.7	**12**
Reverse recovery time (μs)	135	95	70	61	**50**

G. Opening at low load current

The grid operators might need to open the DC CB at load currents (no fault). In such case the current is not rising (or rises very little) during the opening time. This represents worst condition for capacitor charging resulting in long DC CB operating time. Table VI summarizes the interruption time T_{int} for different load current levels. It shows that the T_{int} increases significantly if the load current is reduced. For completeness, two cases of tripping under lower fault are also shown, indicating trend towards longer fault clearing time for lower currents.

Fig. 12 shows the DC CB currents for opening the load current of 0.1 kA. It is seen that the current commutates to the second time-delaying and arming sub-branches respectively at around t=0.531 s and t=0.9 s. The energy absorption surge arrester current i_{SA} consist of a very low intensity current pulse.

Table VI
Current interruption time vs load and trip current level

Trip current (kA)	6	5.4					
Load level (kA)			2.0	1.5	0.5	0.2	0.1
T_{int} (ms)	3.1	5.5	12	16	57	180	470

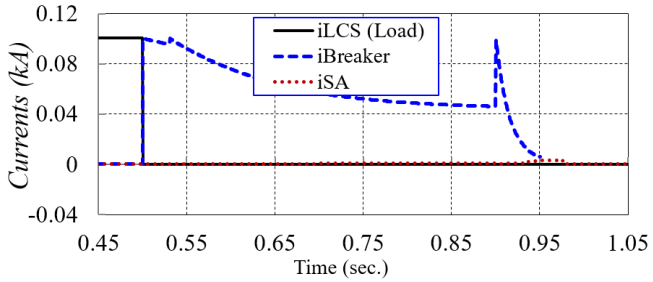

Fig. 12. Branches' currents (Opening at load current of 0.1 kA)

VI. Conclusion

A fast thyristor-based hybrid DC CB design is presented and illustrated on a 120 kV test system with 10kA interrupting current. The DC CB is modelled on PSCAD including DC CB controller for opening, closing and self-protection.

It is concluded that only fast thyristors enable opening time of 2.3ms, while with phase-control thyristors opening time is over 15ms. The thyristor reverse recovery time is shown to be most important limiting factor for the operating speed.

The studies show that there is an important trade-off between the minimal interrupting current and reclosing time because of the need to discharge all resistors before the next opening cycle can commence.

PSCAD simulation results conclude that the model shows good responses for opening and closing on grid order. If larger series reactor is used the opening time is prolonged.

The tests with low interrupting current indicate that opening time is significantly larger if load current is interrupted (no fault condition).

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BIOGRAPHIES

Aliakbar Jamshidi Far obtained his B.Sc., M.Sc., and Ph.D. degrees in Control Engineering from Sharif University of Technology, Iran University of Science and Technology, and Amirkabir University of Technology in 1992, 1996, and 2008 respectively. He has been as an assistant professor with Iranian Research Organization for Science and Technology (IROST) since 2008. He is currently a research fellow with the University of Aberdeen, Scotland. His research interests include the modeling and control of HVDC.

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