

Summary of WP 5

Test environment for HVDC circuit breakers

PROMOTioN – Progress on Meshed HVDC Offshore Transmission Networks
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1 INTRODUCTION

In order to realize multi-terminal, meshed HVDC networks (MTDC), considerable research and development, both on component as well as system level, is underway. One of the essential building blocks of the future multi-terminal HVDC grids, currently drawing significant research interest, is the HVDC circuit breaker. Several manufacturers have proposed and developed HVDC circuit breaker technologies and built prototypes. The behaviour of these prototypes has been verified internally through a range of development tests in the manufacturer's own labs. Testing of HVDC circuit breakers is fundamentally different from that of AC circuit breakers as both voltage across and current through the circuit breaker exist at the same time, leading to an energy absorption requirement. One of the goals of PROMOTioN is to demonstrate the performances of the proposed HVDC circuit breaker technologies with full power testing at an independent short-circuit laboratory.

Before commissioning HVDC circuit breakers in practical applications, adequate verification of its ratings and functionality through testing is crucial. Meaningful demonstration of HVDC circuit breaker technology is achieved when the applied tests accurately reflect realistic fault conditions, e.g. in multi-terminal HVDC networks. Hence, to accelerate the realization of the envisaged MTDC networks, test facilities sufficiently representing a practical DC system under various conditions need to be designed and developed. So far there are no clearly specified and quantified requirements of HVDC circuit breakers let alone a standardized method to test these devices.

The goal of Work Package 5 was to, based on fault analysis of multi-terminal HVDC networks, develop suitable test requirements and a test programme, as well as to realize a test circuit based on AC short-circuit generators. The stresses observed on the models of the circuit breakers during current interruption under various conditions were used as guide to design and realize practical test circuits for HVDC circuit breakers in a high-power laboratory.

2 HVDC NETWORK FAULT ANALYSIS

Identifying the factors determining the fault currents in meshed multi-terminal HVDC networks was the goal of task 5.1. Existing technical literature on HVDC network fault behaviour and analytical fault analysis techniques were reviewed and simulation studies on a benchmark study network shown in Figure 1 were carried out. Fault analysis has been carried out by means of PSCAD simulations on a multi-terminal HVDC benchmark study network fed by half bridge modular multi-level voltage source converters to study the various fault current contributions and their characteristics. The effects of network topology, series reactors, fault location, converter blocking logic, AC network strength and line type on the rate of rise and the magnitude of the fault current have been analysed qualitatively.

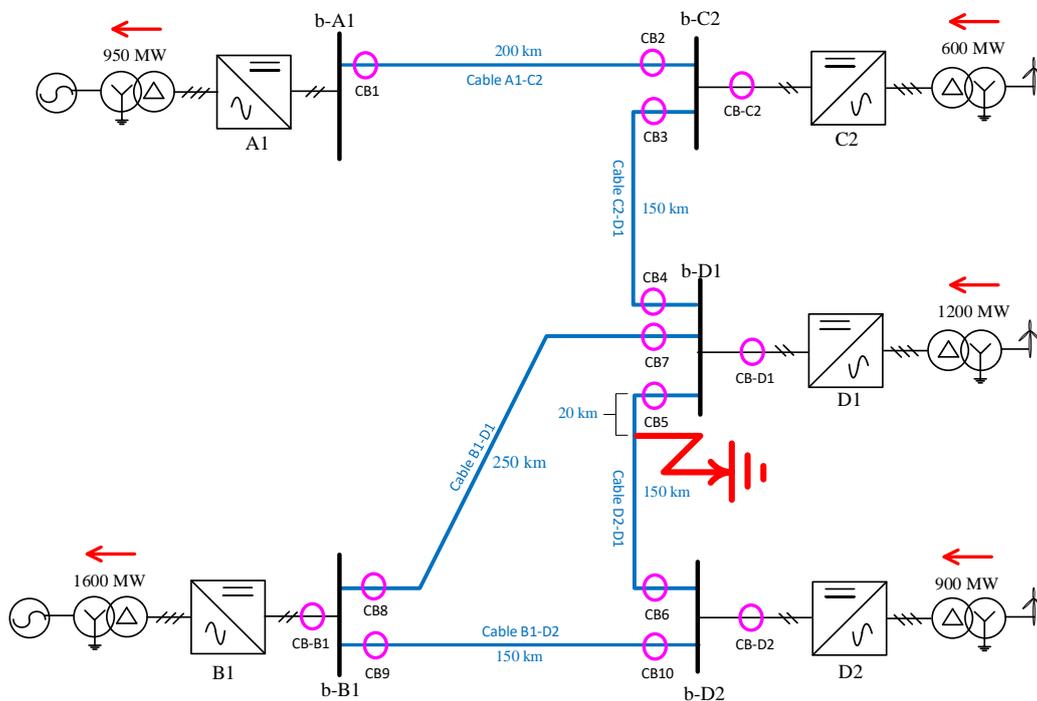


Figure 1 - Five terminal meshed HVDC benchmark network based on CIGRE WG B4-57

Based on the simulation results shown in deliverable 5.2 the following concluding remarks were made:

- C1 A fault is characterised by a breakdown of the insulation system, which results in a voltage transient which travels along the cable away from the fault location and invokes, first, the discharge of any charged capacitances resulting in a current limited only by any series impedance in the cable. These discharges result in the first transients that last only for few milliseconds. Then, the AC sources start feeding the short circuit current limited by AC side impedance and DC side resistance.
- C2 At impedance boundaries, a part of the negative voltage wave is transmitted and the rest is reflected. At HB MMC VSC terminals, the voltage transient triggers the discharge of the submodule capacitors leading to a (near linear) rise in current limited only by the converter arm reactor.

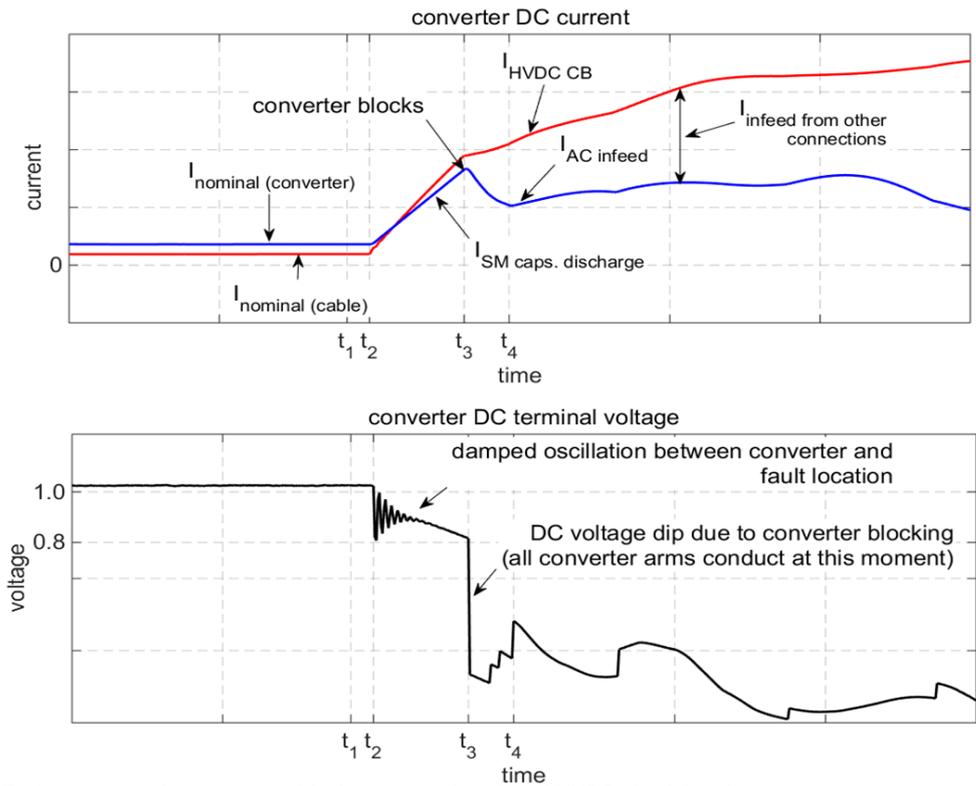


Figure 2 – Fault response of converter and fault current at location of HVDC circuit breaker

C3 In order to protect internal circuitry, an HB MMC VSC converter blocks, as shown in Figure 3, based on a logic combination combining arm and output overcurrent and DC under-voltage thresholds, turning the converter essentially into an uncontrolled diode rectifier. Prior to blocking, the increasing DC output current of the converter has no impact on the AC current, so all energy is supplied by the submodule capacitors.

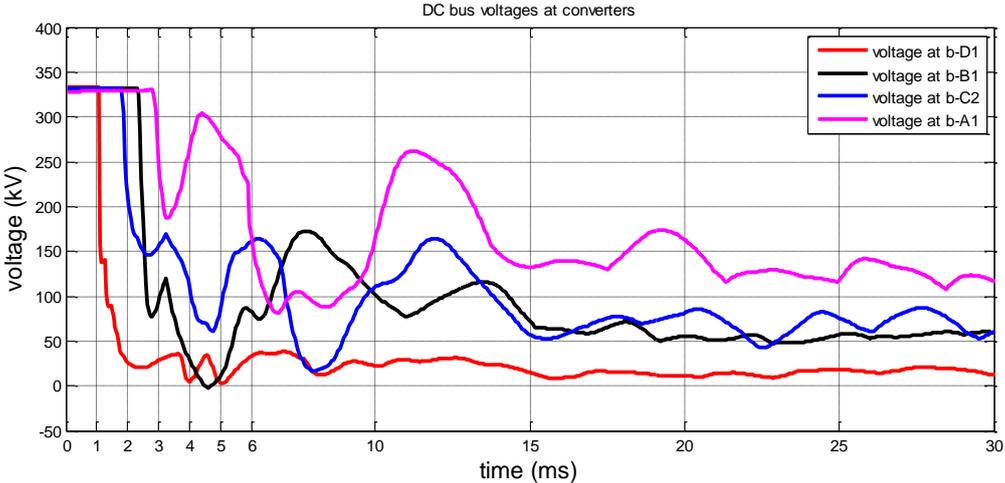


Figure 3 – Converter terminal voltages after occurrence of a fault (no series inductors)

C4 Due to the different arrival times of the voltage transient at various points in the network (shown in Figure 3), converters at different distances block at different times.

C5 After blocking, the DC output current of the converter is determined by the DC resistance between the fault, the converter resistance, the converter transformer impedance and the AC network strength.

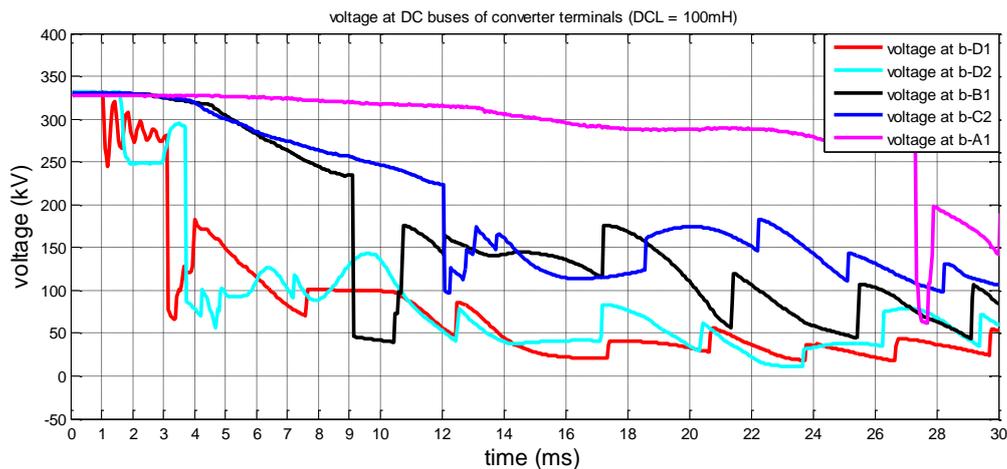


Figure 4 - Converter terminal voltages after occurrence of a fault (series inductor = 100 mH)

- C6 The insertion of series reactors at the ends of cables reduces/limits the rate of rise of fault currents. The higher the inductance of the reactor, the slower the rate of rise of current. This spreads out the arrival times of the voltage transients as shown in Figure 4.
- C7 Due to the insertion of series reactors, the time until converter blocking is increased and the converters are enabled to regulate their terminal voltage. The higher the inductance of the reactor, the smaller the voltage drop at the converter terminal before it blocks.
- C8 As long as a converter can regulate its output voltage (in the presence of series reactors), the discharge of adjacent feeders is very limited.
- C9 The moment a converter blocks, the terminal voltage collapses inducing discharge of adjacent cables
- C10 Rate of rise of current in adjacent cables is suppressed because of multiple series reactors in the fault current path.
- C11 The rate of rise of fault current through a HVDC circuit breaker increases with increasing numbers of adjacent cables (or converter stations) being connected to its bus.
- C12 The phenomenon of reflecting waves causes periodic voltage swings at the cable ends of both positive and negative polarity.
- C13 Depending on the length of the cable and the location of the fault, the reflection of a positive voltage transient may increase the average voltage at the cable end and reduce the rate of rise of fault current.
- C14 Due to the reactive nature of overhead lines, their presence in a DC network has a similar effect to that of a series reactor and decreases the rate of rise of fault current.

It is noted that these qualitative descriptions may be used to predict the worst case fault condition in a given HVDC network. The worst case conditions are always network specific and must under all circumstances be less severe than the maximum ratings of a HVDC circuit breaker. From the analysis it followed that the value of the series reactor may be adjusted in order to change the stresses or demands placed on converter stations and/or prospective HVDC circuit breakers. A detailed description of these fault current contributions is given in deliverable 5.1.

3 STRESSES ON HVDC CIRCUIT BREAKERS

In order to study the stresses on HVDC circuit breakers during DC fault current interruption, the detailed operation principle of three different technologies of HVDC circuit breakers; namely, active current injection HVDC circuit breaker, shown in Figure 6, and two types of hybrid power electronic HVDC circuit breakers, an IGBT based version of which is shown in Figure 5, were modelled in PSCAD. The models were available in deliverable 5.2. The models of these circuit breakers were inserted in the benchmark study grid which was defined in deliverable 5.1 and simulation results were analysed in detail in deliverable 5.3.

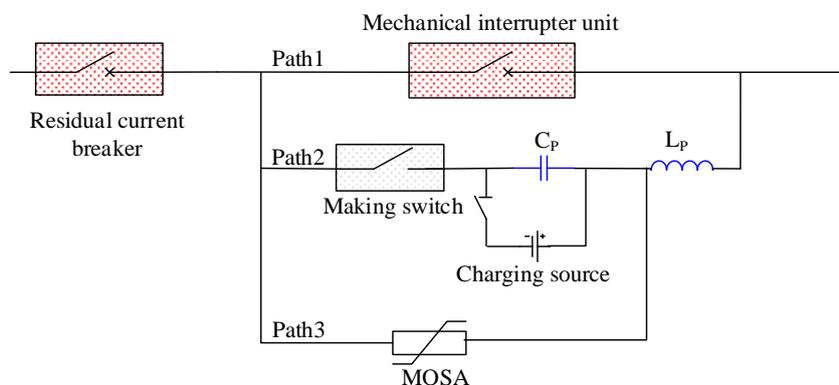


Figure 5 – Model of mechanical HVDC circuit breaker with active current injection

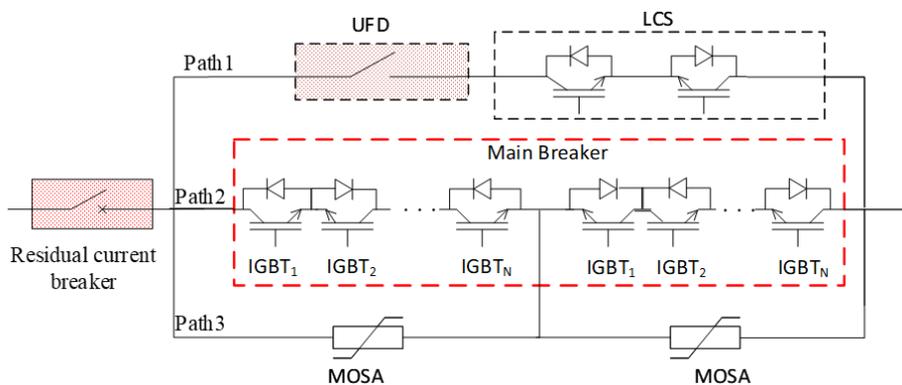


Figure 6 – Model of hybrid HVDC circuit breaker

For all the considered HVDC circuit breakers, it is necessary to have a series DC current limiting reactor as shown in the generic circuit breaker structure in Figure 7. However, assuming fast enough protection system, the size of the reactor used along with each circuit breaker technology depends mainly on the operation time (the time from trip order until the circuit breaker can withstand a transient interruption voltage (TIV)) of the circuit breaker. In general, the DC current limiting reactor is chosen to,

- Limit the magnitude of the fault current occurring in the protection zone of the circuit breaker to within the interruption capability of the circuit breaker during fault current neutralization time.
- Ensure continued controlled operation of the healthy part of the system by avoiding the voltage collapse of the entire DC grid during the fault neutralization time. In doing so the series

DC current limiting reactor also provides more time for the protection system to detect and locate the fault.

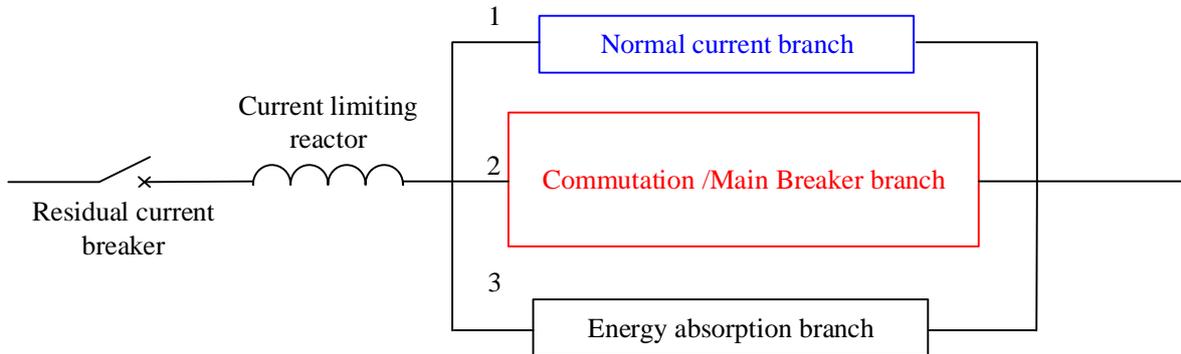


Figure 7 - Generic HVDC circuit breaker structure

Accordingly, 150 mH DC reactor is used in series with the active current injection HVDC circuit breaker and a breaker operation time of 8 ms is assumed. A peak current of about 12 kA is interrupted and an amount of energy of about 25 MJ is absorbed by the breaker. In this case the converters at the ends of the faulted cable block as either of these converters cannot continue its controlled operation during relatively longer fault neutralization time. It must be noted that the maximum interrupted current and the corresponding energy absorbed by a circuit breaker are highly dependent of the system architecture and associated parameters.

For the hybrid HVDC circuit breakers, a breaker operation time of 2 ms is assumed. Due to the shorter breaker operation time, a 100 mH DC current limiting reactor is used in series with the hybrid HVDC circuit breakers. Hence, a peak current of about 8.5 kA is interrupted and an amount of energy of circa 10 MJ is absorbed by hybrid circuit breakers. With the assumed relay time, the fault can be cleared before any of the converters in the system block.

For all the circuit breakers, it is observed that the system voltage starts to recover even before the fault current is completely cleared. Thus, from the system perspective, the most important phase of the current interruption process is, therefore, the fault neutralization time. However, this poses an additional burden to the HVDC circuit breaker as it must dissipate more energy including the electrical energy supplied by the system due to the recovered system voltage.

4 HVDC CIRCUIT BREAKER TEST REQUIREMENTS

In general, to stress the HVDC circuit breakers as in service, a test circuit should provide sufficient current, voltage and energy. The specific details are mainly dependent on the system under consideration. However, the most important functionalities of an HVDC circuit breaker which must be tested are;

1. Capability to create a local current zero without restrike/breakdown of mechanical switches/interrupters or thermal overload of power electronic components at rated DC fault current
2. Generation of sufficient counter voltage to initiate fault current suppression
3. Capability of energy absorption components to absorb energy during fault current suppression wave trace as in service. Depending on the rated test sequence, this capability must be demonstrated several times within a defined sequence.
4. Capability to withstand the rated DC voltage after the current interruption process
5. The breaker operation time: the minimum time at which the circuit breaker reaches the TIV withstand level after trip order
6. The maximum current interruption: The maximum current the breaker can interrupt within the breaker operation time
7. The maximum energy that the circuit breaker can absorb
8. The number and frequency of operation: the number of interruption operations that the circuit breaker can perform before thermal run away occurs in its surge arresters. The interruption interval needs to be defined, e.g. like auto reclosure in AC circuit breakers

To date, there is no international standard describing the requirements, applicable tests and test procedures of HVDC circuit breakers. A general guideline for lists of tests that shall be applied to HVDC circuit breakers for its operation and performance verification has been developed. Since there is no international standard for HVDC circuit breakers, the guideline is compiled using AC circuit breaker standards, CIGRE technical brochures, VSC converter valve standard and Chinese draft standard for HVDC circuit breakers as references, as shown in Figure 8.

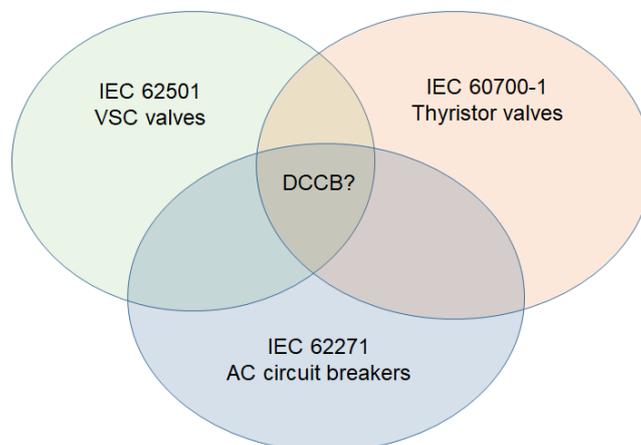


Figure 8 - Relevant existing standards

For the purpose of harmonizing the definitions and terminologies related to HVDC circuit breaker operation, the terms and definitions developed by CIGRE JWG A3/B4-34 have been presented, as shown in Figure 9. Wave trace related terminologies and timing definitions during operation of HVDC circuit breaker are presented in a generic manner. Timing definitions are further divided into protection system related, circuit breaker related and system related definitions.

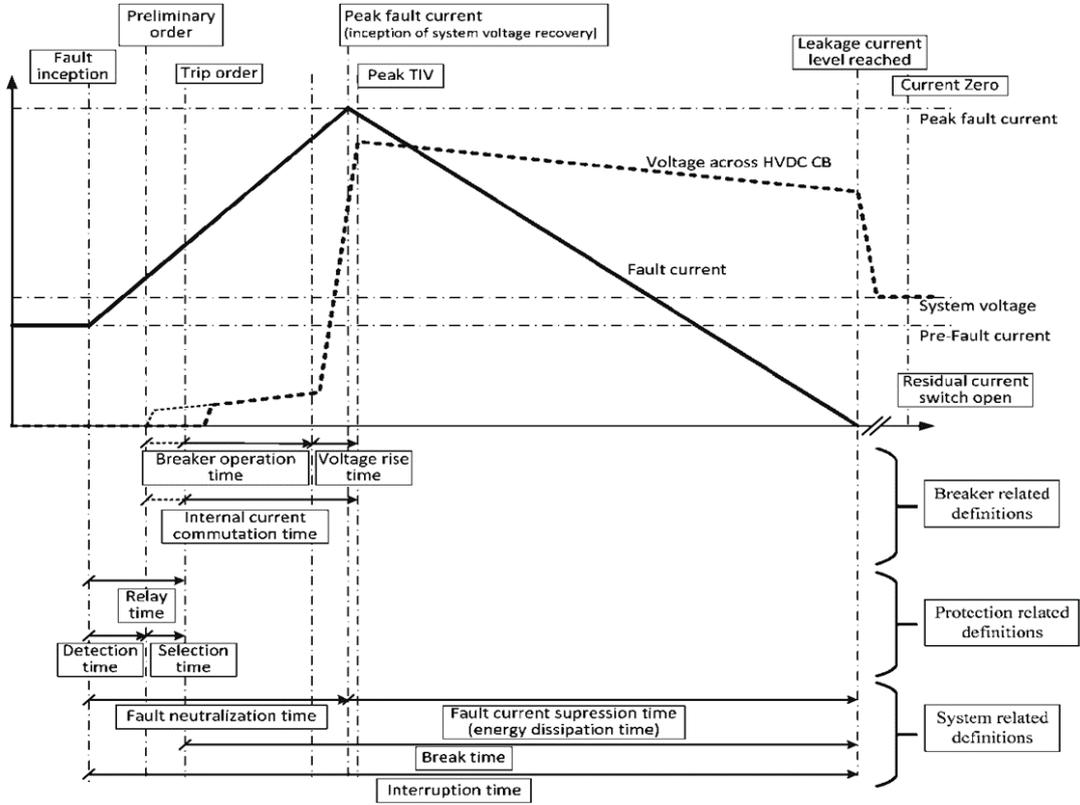


Figure 9 – DC fault current interruption timing definitions & terminology [source: JWG A3/B4-34]

In deliverable 5.4, as a base for the test requirements, service conditions for HVDC circuit breakers have been described. This is adopted from AC circuit breaker standards. The ratings related to HVDC circuit breaker which shall be specified in the name plate of the equipment have been described. The latter is also adopted from AC circuit breaker standards; however, by carefully selecting and adapting what is applicable to HVDC circuit breakers. These ratings are described in terms of the terms and definitions.

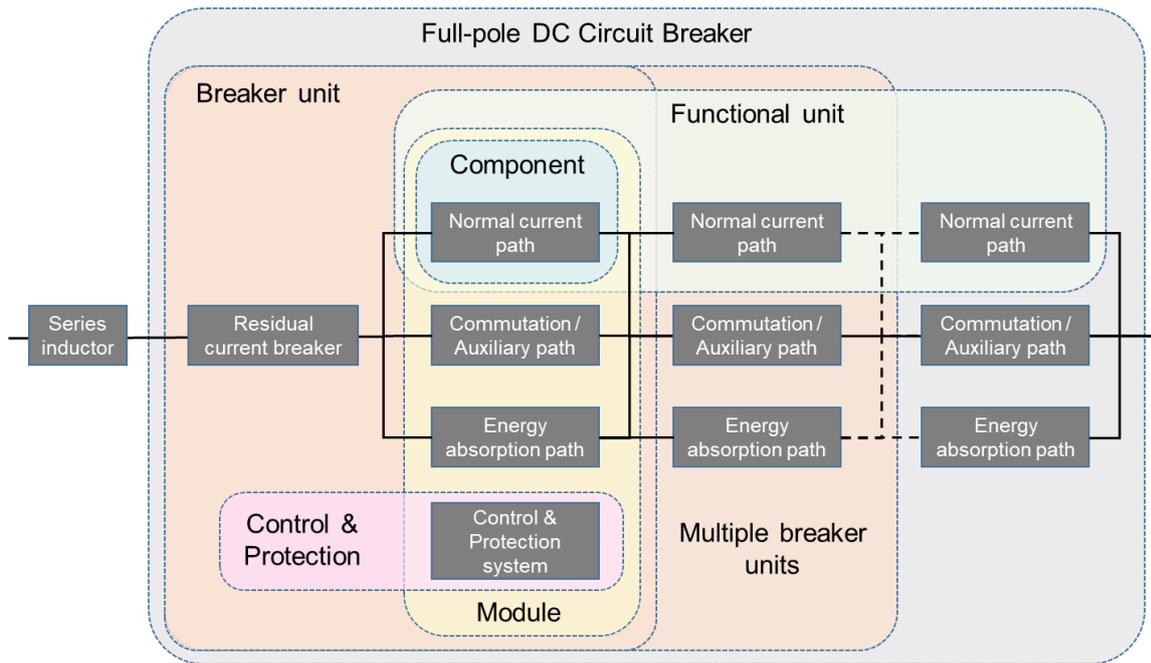


Figure 10 - Modular construction of HVDC circuit breakers - Terminology

Deliverable 5.4 also discusses design and construction of HVDC circuit breakers and the impact on testing. The terms related with internal components of HVDC circuit breaker, the physical construction as shown in Figure 11, as well as the build-up of HVDC circuit breaker for higher voltage rating as shown in Figure 10, have been discussed.

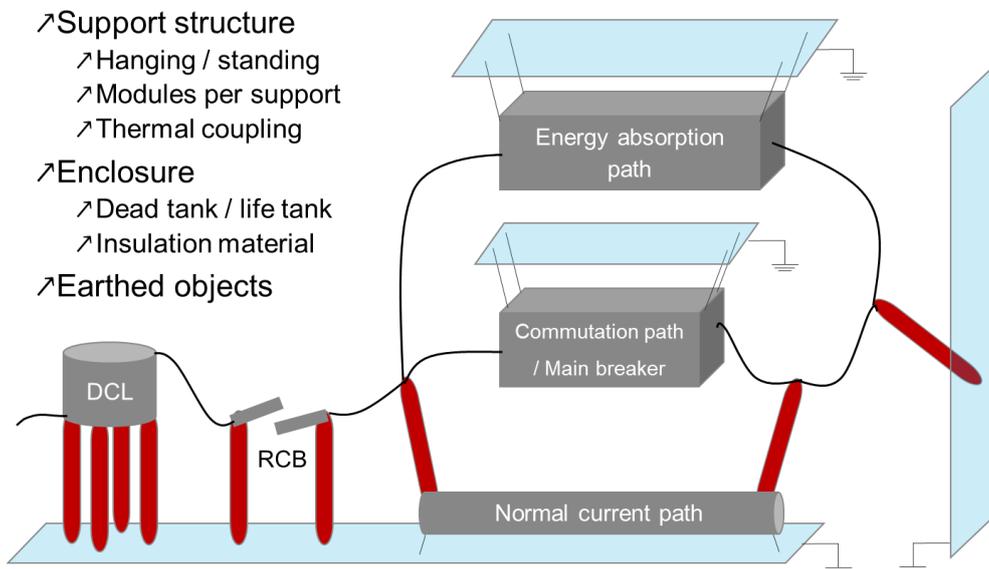


Figure 11 - HVDC circuit breaker physical construction design choices

The tests intended to verify the functionality and performance of HVDC circuit breaker in a type test program are discussed in deliverable 5.4. These tests are sub-divided into dielectric, operational, making and breaking tests as well as endurance tests as shown in Figure 12. However, it should be noted in PROMOTioN project the focus is on the demonstration of DC short-circuit current interruption performance of HVDC circuit breakers and this is carried out using the test circuits designed in task 5.7.

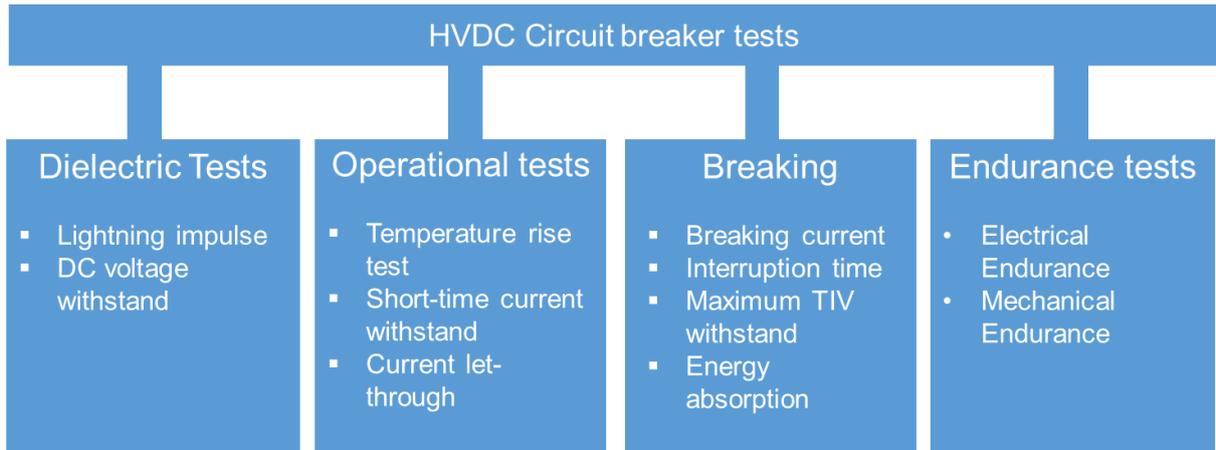


Figure 12 - HVDC circuit breaker test requirements

Test procedures described in IEC standards for AC switchgear (IEC 62271-1, IEC 62271-100, IEC 60060-1) as well as the IEC standards of DC switchgear for railway applications (IEC 61992-1, IEC 61992-2) have been used as guides in the development of this document. Also, the tests of HVDC circuit breakers conducted as part of TWENTIES project have been studied and some of the tests were adopted from the test reports thereby.

Deliverable 5.4 does not describe an exhaustive list of tests, but rather the main categories of tests that can be applied to HVDC circuit breakers. However, only a limited sub-set of the described tests fall within the scope of PROMOTioN – i.e. interruption tests. The exact scope and test procedure will be decided upon discussion between DNV GL KEMA laboratories and the manufacturer on a bilateral basis.

5 HVDC CIRCUIT BREAKER TEST CIRCUIT REQUIREMENTS

Based on the stresses which are exerted onto HVDC circuit breakers during DC fault current breaking operations, requirements for test circuits in which DC short-circuit current breaking capability is to be verified, have been developed in deliverable 5.6.

A test circuit for HVDC CB short-circuit current breaking testing should reproduce the stresses that are relevant for current breaking operations up to the rated values including a test factor where applicable. Furthermore, the test circuit must be able to withstand any stresses such as TIV which are produced and determined by the HVDC CB itself. For a test circuit to provide adequate stresses to HVDC CBs, it should fulfil the following requirements based on the characteristic of the four different periods discussed in the previous section:

1. Pre-condition the HVDC CB to mimic worst case normal service conditions, and ensure internal systems are powered up and charged
2. Produce a test current which rises somewhat linearly from anywhere up to the rated load (or short-time withstand current) to the intended test duty within the breaker operation time. It is shown in [7] that the most difficult interruption may not necessarily be the highest current. Thus, test circuits have to provide a wide range of quasi-DC currents, from the rated load current (or less) to the rated short circuit breaker current of an HVDC CB. The test circuit must be able to apply the test current bidirectionally.
3. Supply rated energy to the HVDC CB and withstand TIV
4. Supply rated dielectric stress immediately after current suppression
5. Avoid damage to the HVDC CB and test circuit in case of failure - if the prospective short-circuit current from a test circuit can exceed the HVDC CB's rated short-circuit breaking current, it is necessary to limit the damage to the HVDC CB as well as the test installation in case of a failure to clear. Methods to avoid potential damage to the test breaker as well as the test installation have been proposed
6. Be implementable / economical – the test circuit must be technically feasible, practical and economical

The above requirements should be fulfilled whilst respecting practical breaker operation times which are currently assumed to be in the range of 2 – 8 ms.

These stresses do not have to be supplied by the same source, in which case it is referred to as a synthetic test. The modular construction of HVDC CBs may under certain conditions allow the verification of functionality and/or ratings by testing a reduced number of modules, which is referred to as modular testing. Furthermore, in some cases, different functionalities of an HVDC CB can be tested in separate tests with different test circuits, in which it is referred to as multi-part testing.

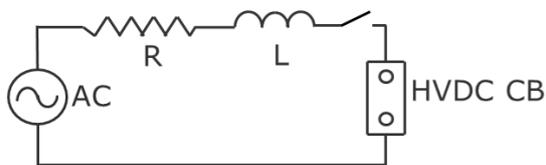
Four hypothetical test circuits based on a controlled rectifier, a charged capacitor, a charged inductor, and an AC short-circuit generator operated at reduced frequency, have been qualitatively discussed and compared to the test circuit requirements, as shown in Table 1.

Table 1 - Summary of test methods and their applications

Test circuit requirement	Rectifier	Charged capacitor	Charged reactor	AC short circuit generator
Pre-condition HVDC CB	Current profiles and stresses can be accurately controlled to follow a target waveform.	Separate circuit required	Separate circuit and/or source required	Separate circuit or source required
Produce test current	Current profiles and stresses can be accurately controlled to follow a target waveform.	Very high di/dt can be achieved	Difficult to control di/dt. Quasi DC current can be obtained in case very fast switching cannot be achieved. Hence the method may not be suitable for testing HVDC CBs with power electronics in the normal current path.	The existence of minimum inductance in the circuit due to generator and transformer reactance put maximum limit on di/dt
Supply rated energy to the HVDC CB and withstand TIV	Current, voltage and energy profiles and stresses can be accurately controlled to follow a target waveform. However, large required power supply may be prohibitively expensive to realize	Requires large capacitance, with associated volume and cost.	Requires large reactance with very high quality factor, with associated impact on charging circuit, volume and cost.	Very high voltage (full-pole voltage) may exceed the insulation coordination of test installation or multi-part, multi-unit tests to be applied.
Supply rated dielectric stress	Voltage stresses can be accurately controlled to follow a target waveform	Some DC charge remaining after suppression. Very large capacitance required to make this sufficient for testing	Must be realised by separate source/circuit.	After suppression, AC voltage stress is applied by the generator. Controlled DC stress must be realised by separate source/circuit
Avoid damage to the HVDC CB and test circuit	Must be realised by additional circuit provisions	Must be realised by additional circuit provisions	The peak current is the same as rated interruption current	Must be realised by additional circuit provisions
Be implementable / economical	High investment cost and complex control	Can utilise existing test facilities in some cases	Accurate switching of charging circuit is required; High quality factor reactor is required; Challenging to	Utilises existing test facilities, with minimal additional investment cost required. Within a reasonable

			achieve high currents	range, can provide full testing to prototype-level HVDC CB
Test extra functionality such as reclosing, soft-closing, etc.	Current, voltage and energy profiles and stresses can be accurately controlled to follow a target waveform	Separate circuit and/or source required	Separate circuit and/or source required	Separate circuit and/or source required
Application	Low to medium voltage testing	Interruption-only tests very low energy	Low-medium current and energy	Full current, high energy testing.

It was concluded that only a controlled rectifier circuit could directly synthesize all necessary stresses but is likely to be prohibitively expensive and complex at the required power ratings and functionality. Depending on the charging circuit, the charged reactor method may prove to be unsuitable for testing hybrid HVDC circuit breakers. Both the charged capacitor and AC short-circuit generators are capable of producing a suitable DC short-circuit test current. However, AC short-circuit generators running at a reduced frequency, as shown in Figure 13, offer the possibility to deliver high energy stresses, which may be unpractical to achieve using a charged capacitor circuit, due to the large required capacitance. The latter is especially relevant for testing HVDC circuit breakers with long breaker operation times.



↗ Test circuit parameters

- ↗ Generator frequency
- ↗ Circuit inductance
- ↗ Magnitude of source voltage
- ↗ Making angle

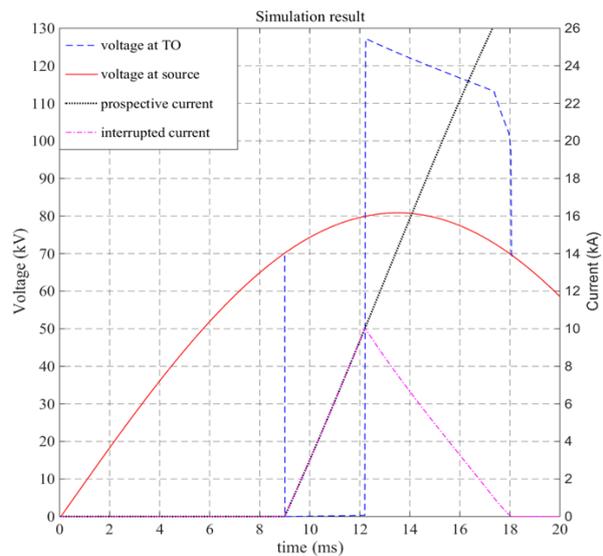


Figure 13 – Principle of AC short circuit generator based test circuit

It is shown that AC short-circuit generators operated at reduced frequency offer flexible control of the rate of rise of test current, as shown in Figure 14, and the amount of energy delivered to the HVDC circuit breaker by carefully choosing the generator frequency, the test circuit impedance, the generator source voltage magnitude, and the making angle.

The AC characteristic implies that an inherent limitation exists on testing HVDC circuit breakers with long breaker operation times, as the entire fault neutralisation time must be less than the longest possible half wave period of the applied test current.

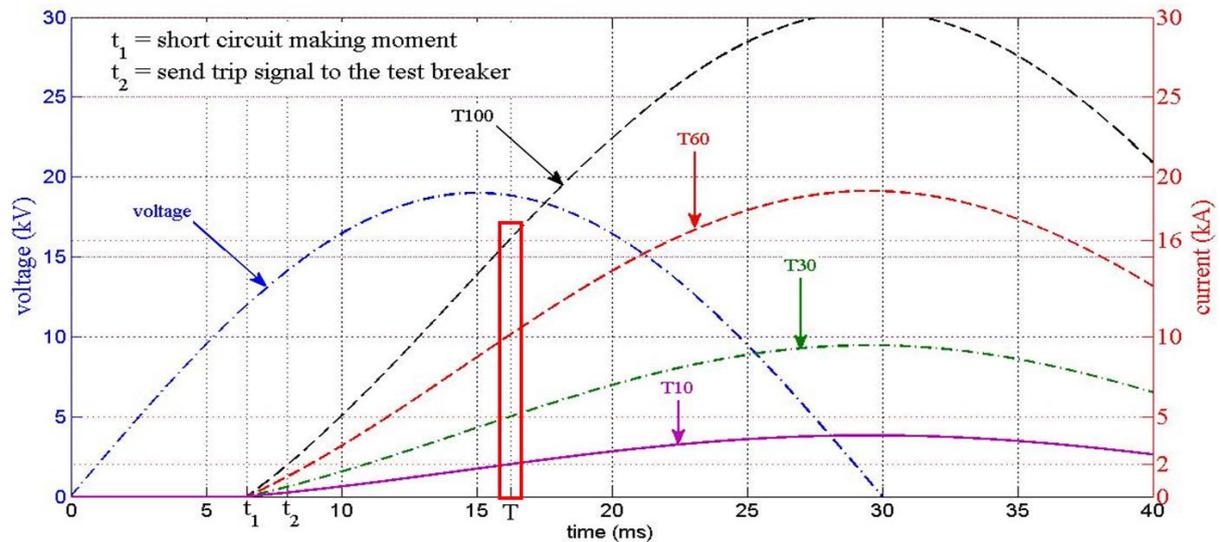


Figure 14 – Realizing different testing duties with AC short-circuit generators

A method to protect the test object and the test circuit from damage in case the HVDC circuit breaker fails to operate correctly, has been presented. A high-speed level-detector triggered spark-gap, combined with an auxiliary breaker can by-pass the prospective test current and isolate the test object from the test source.

Apart from the controlled rectifier circuit, none of the discussed test sources is capable of supplying DC voltage stress after interruption without additional measures. In case of AC short circuit generators, it is shown that for HVDC circuit breakers with active current injection, it is possible to achieve DC voltage stress by trapping charge in the injection capacitor, or otherwise by injecting a DC voltage stress from an external DC voltage source.

Finally, it was recognized that no practical test circuit can supply the required stresses to directly test EHV full-pole HVDC circuit breakers. Some suggestions for verifying performance of a modular part of a breaker i.e. unit testing, or separately verifying different functionalities i.e. multi-part testing and realising different stresses from different test sources i.e. synthetic testing are discussed in deliverable 5.6.

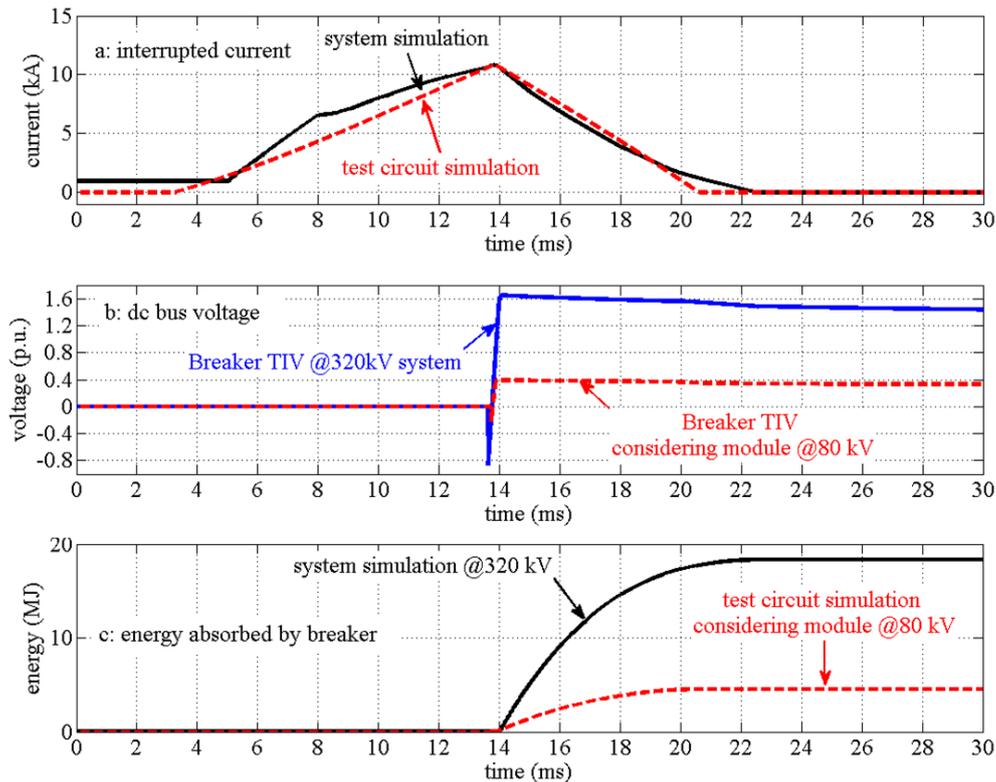


Figure 15 – Prorating of test requirements for modular testing

As shown in figure 15, the module ratings can be derived from full-pole HVDC circuit breaker ratings can be done in the following way:

Current sharing

- In series connected modules current, is not divided

Voltage grading

- Divided by number of series connected modules
- Determined by surge arrestors
- Full-pole components need to be dielectrically tested separately

Energy grading

- Divided by number of series connected modules
- Margin required determined by small differences in timing

In deliverable 5.7, the realisation of the reduced frequency AC short-circuit generators based test circuit at KEMA Laboratories, shown in Figure 17, was described. A method for tuning the test circuit's variables to achieve the required current and energy test stresses was presented. The implementation of overvoltage and overcurrent protection methods was explained, as well as methods to realize dielectric stress after current suppression. The resulting final test circuit is shown in Figure 16. A test program aimed at validating the test circuit's ability to meet the requirements was provided. Test results of prospective current tests, overcurrent and overvoltage protection tests, and of dielectric stress application tests were provided. Simulation results of HVDC circuit breaker models were superimposed onto the experimental results to illustrate the ability of the test circuit to synthesize realistic stresses, as shown in Figure 18.

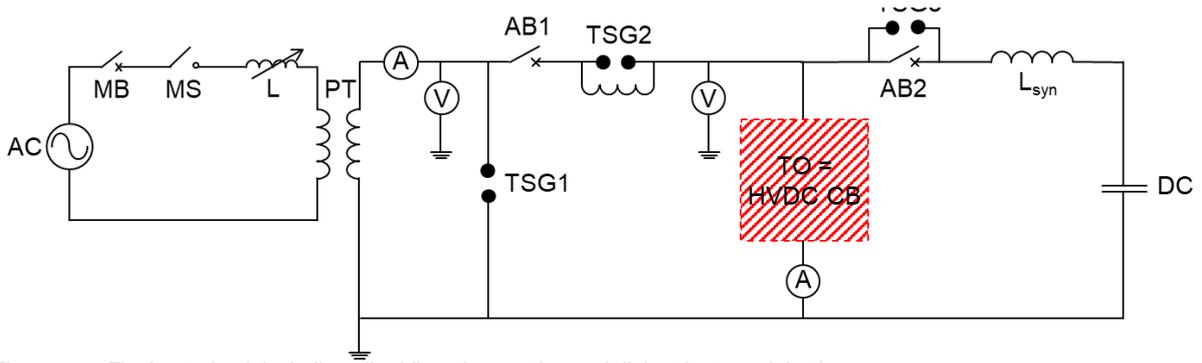


Figure 16 – Final test circuit including all additional protection and dielectric stress injection measures

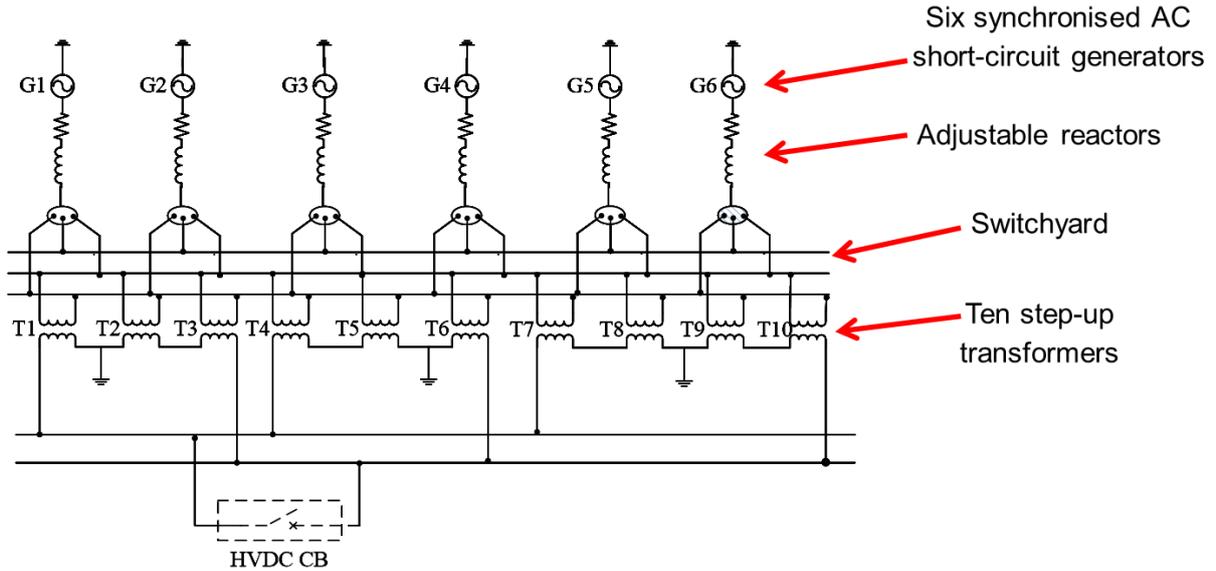


Figure 17 – KEMA Laboratories High Power Lab schematic

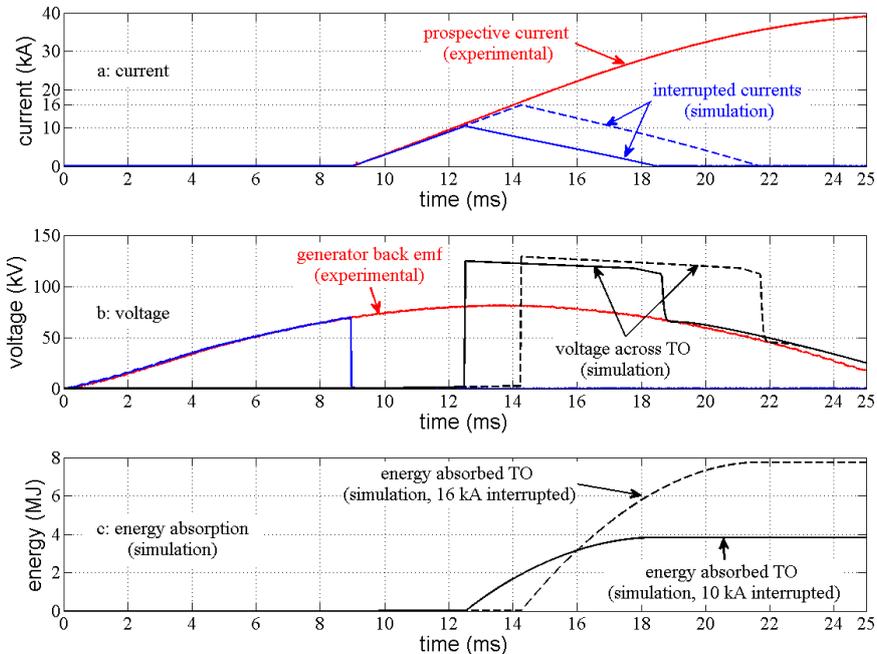


Figure 18 – Simulation results of fault current interruption superimposed onto experimental prospective current test result