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CIGRÉ A3/B4 - 009

CIGRÉ Winnipeg 2017 Colloquium
Study Committees A3, B4 & D1
Winnipeg, Canada
September 30 – October 6, 2017

Stress Analysis of HVDC Circuit Breakers for Defining Test Requirements and its Implementation

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SUMMARY

Testing of HVDC circuit breakers (CBs) is fundamentally different from that of AC CBs as both voltage across and current through the HVDC CB exist at the same time, leading to an energy absorption requirement. Meaningful validation of HVDC CB technology is achieved when the applied tests accurately reflect realistic fault conditions encountered in practical operation. Because of the absence of standards for testing HVDC CBs, it is necessary to first define generic test requirements and a test programme based on fault analysis of multi-terminal HVDC grids.

Therefore, the paper first provides detailed analysis of fault currents in a multi-terminal HVDC grid composed of bipolar converter configuration. The phenomena following the occurrence of a fault and the critical parameters contributing to the fault current are investigated. Then, the fault current interruption process by various concepts of HVDC CBs and the important stresses associated with these different technologies are identified. These stresses are translated into generic current interruption test requirements that are adequate representatives of practical operational conditions.

It is found that AC short-circuit generators running at low power frequency and having sufficient short-circuit power can supply the necessary electrical stresses needed for testing different technologies of HVDC CB. Experimental test results demonstrating a test circuit based on AC short-circuit generators at 16.67 Hz power frequency are presented. These results are compared with simulation results obtained from system studies. Some practical challenges of using AC short-circuit generators for testing HVDC CBs in a high-power laboratory are addressed via experimental validation.

KEYWORDS

HVDC circuit breaker testing, Faults in HVDC grid, test requirements, test circuits.

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1. INTRODUCTION

HVDC CBs are expected to play an important role in the protection of the future multi-terminal meshed HVDC grids. Several prototypes of HVDC CBs have been developed. Mainly two technologies– the hybrid power electronic and the active current injection HVDC CBs, have been described as promising [1]–[5]. However, the claimed performances of these prototypes have not yet been validated outside the manufacturer's laboratories.

To date, most of the VSC HVDC projects in operation are point-to-point interconnections apart from two projects commissioned in China [6], [7]. A few technical, regulatory and financial challenges need to be addressed before meshed HVDC networks are realized. To tackle the challenges that hamper the implementation of a meshed offshore HVDC grid, PROMOTioN (Progress on Meshed Offshore HVDC Transmission Networks), an EU funded research project, has been set up by a consortium consisting of 35 key European stakeholders [8]. One of the goals of the project is to demonstrate full-power testing of HVDC CBs. The performances of three different technologies of HVDC CBs are expected to be demonstrated in the project. This paper evaluates and presents the stresses that need to be replicated during the tests of HVDC CBs. The paper also discusses practical implementation of a test circuit based on AC short-circuit generators and presents experimental demonstration of this test circuit for HVDC CB having operation time of 8-10 ms.

The paper starts with system studies including models of HVDC CBs to study HVDC fault current interruption. This is to gain insight of the stresses imposed by the system on the breaker. To monitor the adequate performance of the HVDC CB prototype, these stresses need to be replicated by a test circuit. The impacts of various system parameters such as current limiting reactors, the strength of the neighboring AC grids, the distance of a fault location from a converter, etc. are discussed.

For testing HVDC CBs, a test circuit based on a high-power DC source such as rectifier circuits with tunable parameters would be the ideal solution. However, to build this circuit at a high-power laboratory requires unsurmountable investment cost. An alternative test circuit using AC short-circuit generators running at low power frequency is presented in [9]. AC short-circuit generators are already in use for AC equipment testing; therefore, without significant investment, these can readily be used for testing HVDC CBs. Two major issues of using AC short-circuit generators, namely, the application of dielectric stress after successful current interruption and a method to avoid overcurrent in the test breaker in the case of failure to clear the current, are experimentally demonstrated in the author's high-power laboratory.

The remaining part of the paper is organized as follows. Section 2 discusses faults in HVDC network. A simulation system used in the paper is described in this section. In Section 3, the stresses on HVDC CB during fault current interruption are discussed. These stresses are translated into qualitative current interruption test requirements in Section 4. Implementation of a test circuit based on low frequency AC short-circuit generators is presented in Section 5. Section 6 presents conclusion based on the discussion in the paper.

2. HVDC NETWORK FAULT ANALYSIS

2.1. Simulation System Description

For the purpose of studying faults in multi-terminal HVDC grids, a hypothetical five-terminal meshed HVDC grid shown in Figure 1 is used as a benchmark network. All converters are bipole converters with low impedance earthing at each converter. The system data for this network is adopted and modified from the DC test network developed in [10]. Three of the five terminals namely, C2, D1 and D2 are assumed to be located offshore and are interconnected via submarine cables with radial arrangement. The remaining converters, namely, A1 and B1 are located onshore and receive power from the offshore network via three DC cables as shown in the Figure 1. All converters are of the

modular multi-level (MMC) type with half bridge submodules. Simulation is performed in EMTDC/PSCAD using the detailed equivalent model of MMC developed in [11]. The simulation parameters of each converter are shown in Table 1.

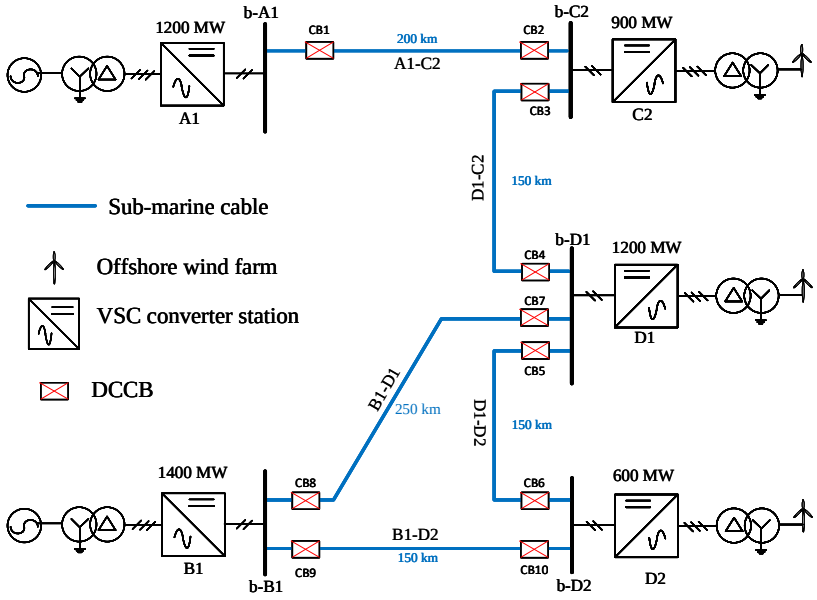

Figure 1: Five terminal bipolar HVDC grid

Table 1: Converter parameters

Parameter	A1	B1	C2	D1	D2
DC Voltage (kV)	±320	±320	±320	±320	±320
Rated power (MVA per pole)	800	800	600	800	400
AC short-circuit power (GVA at PCC)	30	30	3.8	3.8	3.8
Transformer primary voltage (kV)	380	380	145	145	145
Transformer secondary voltage (kV)	220	220	220	220	220
Transformer leakage reactance	18%	18%	18%	18%	18%
Transformer series resistance	0.6%	0.6%	0.6%	0.6%	0.6%
Conduction losses in arm reactor and converter valves	0.3%	0.3%	0.3%	0.3%	0.3%
Arm reactance	15 %	15 %	15 %	15 %	15 %
Number of SMs per arm	160	160	160	160	160

2.2. HVDC Network Fault Analysis

First, the prospective fault currents in a multi-terminal HVDC network under different fault conditions are investigated. In order to bridge the gap between the magnitude of the prospective fault currents in HVDC networks and the speed and the maximum current breaking capabilities of state-of-the-art HVDC CBs, DC current limiting reactors are used [3], [12]. These reactors reduce the rate-of-rise of fault currents, thus providing more time for HVDC CBs to act before the fault current exceeds the maximum limit. Unless otherwise specified, 100 mH current limiting reactors are placed at the end of each cable in series with HVDC CBs. HVDC CBs are put on the line side of the current limiting reactors.

Figure 2 shows simulation results when a pole-to-ground fault is applied at 10 km from converter D1 on a cable connecting to converter B1. The graph in Figure 2a shows the current measured at the CB on a faulted cable (CB7) and the main fault current contributors, namely, converter D1 and the two adjacent feeder cables. The graph in Figure 2b shows the voltages measured at each converter's dc

bus. The sudden voltage drops on the traces in this graph show the moment the corresponding converter blocks. The converters are set to block if the currents measured in any one of the arms exceed 3.5 kA and/or if the converter dc voltage falls below 0.75 p.u. It can be seen from this figure that except the converter D1 which blocks due to the overcurrent threshold, all other converters block due to the under-voltage threshold. The time at which a given converter blocks is proportional to the distance of the fault location from a converter, which means a fast protection system together with HVDC CBs can clear the fault before some of these converters block.

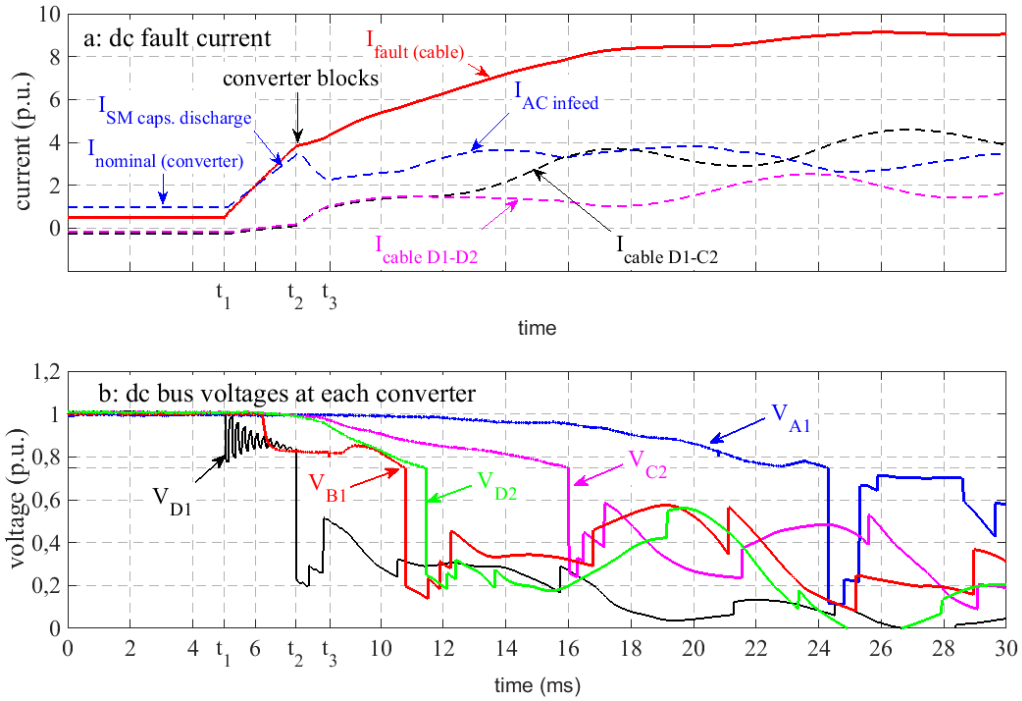

Figure 2: Impact of a fault in HVDC network. a: fault current and its contributors b: dc bus voltages at different converters

Considering Figure 2a, the sequence of events following the occurrence of a fault are divided into three distinct time periods and discussed below [13],

i. Submodule discharge period

This period is from the moment the travelling wave arrives at a converter till the converter blocks (t_1-t_2 in Figure 2a). During this period, the fault current starts to rise at a rate determined by the system voltage, the magnitude of the arm reactors of the converter and the DC current limiting reactor on the faulted cable. The larger the value of the DC current limiting reactor, the lower the rate-of-rise of fault current. It can be seen from Figure 2a that, during this interval, the fault current is dominated by the discharge of the converter's submodule capacitors.

ii. Arm current decay period

This is the time from t_2-t_3 in Figure 2a. Just before the converter blocks, the submodule capacitors of both lower and upper arms of each phase leg are discharging into the fault through the arm reactors. The moment a converter blocks, the currents through the arm reactors continue to flow via the freewheeling diodes or other bypass circuitry although there is no further discharge from the submodule capacitors. Basically, the AC and DC sides of the converter are momentarily decoupled during this period. The DC voltage collapses during this period, as can be seen in Figure 2b. The current coming from the converter decays at a rate determined by the time constant of the DC side

circuit up to the fault location (see dashed blue curve in Figure 2a). During this period, the contributions from the adjacent cables increases due to the voltage collapse.

iii. AC in-feed period

During the period from t_2-t_3, the current through some of the arms decays to zero depending on the resistance in the current path. From t_3 onwards (in Figure 2a), the fault current contributed by the converter D1 is coming from the AC side through the freewheeling diodes. The magnitude of the fault current due to AC in-feed depends on the strength of the AC grid, the impedances of the converter transformer, arm reactors and the DC side impedance up to the fault location. During this period the current contribution from adjacent cables also continues to increase because of the contribution from the converters at the remote ends of these cables.

3. STRESSES ON THE HVDC CIRCUIT BREAKER DURING FAULT CURRENT INTERRUPTION

Models of HVDC CBs based on the proposed concepts are inserted into the benchmark network to study the fault stresses seen by CBs during DC current interruption. Later, these stresses are used to define the requirements for the test circuits to be realized in a high-power laboratory where the actual HVDC CBs are expected to be tested.

Figure 3a (dashed curves) show the fault currents' magnitudes through a CB for faults occurring at distances of 10 km, 100 km and 240 km from the converter D1. The propagation delays of the travelling waves from the fault locations up to the converter D1 are removed in the figure for easy comparison. As the distance of the fault location increases, the magnitude of the fault current decreases.

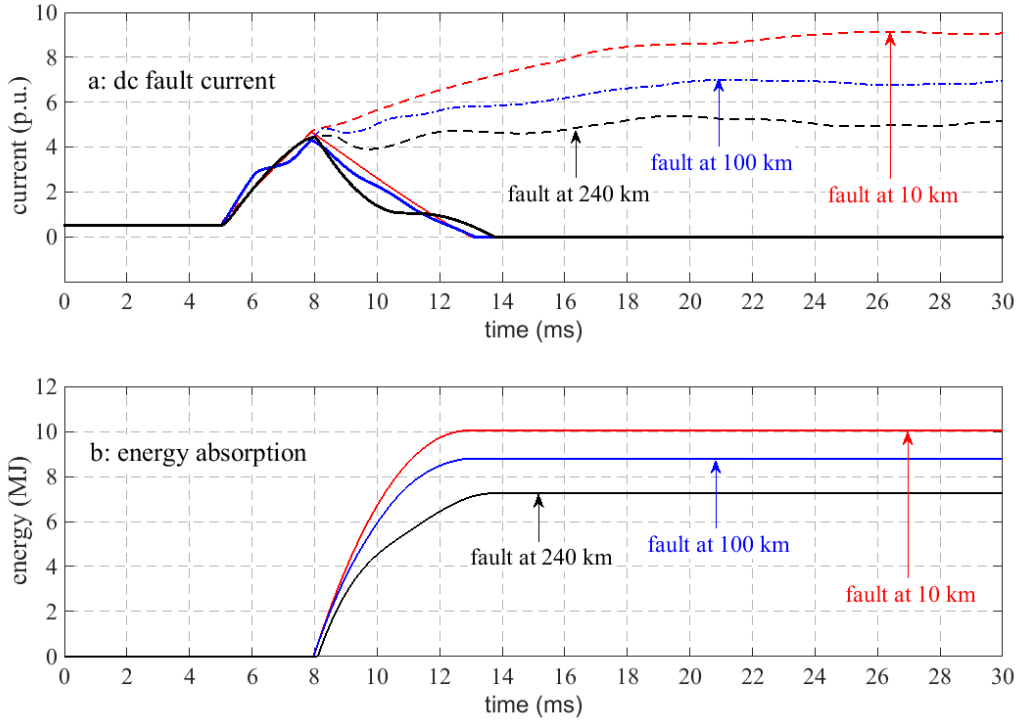

Figure 3: a: Fault currents at different distances on a cable. Dashed lines are prospective fault currents, solid lines interrupted current by HVDC CB. b: Energy absorbed by a HVDC CB when interrupting fault currents at different distances along a cable

Before discussion of fault current interruption, a few important timing definitions related with the operation of HVDC CB as presented in [5] are provided. **Fault neutralization time**– the time interval between fault inception and the instant when the fault current starts to decrease, **breaker operation**

time– time interval between the reception of the trip order and the beginning of the rise of the transient interruption voltage (TIV) and **fault current suppression time**– time interval between the peak fault current and the instant when the current has been lowered to leakage current level.

Figure 3 shows the fault current interrupted by a model of a hybrid HVDC CB for faults occurring at locations specified above. A breaker operation time of 2 ms is assumed and a trip signal is sent to the breaker when the fault current reaches 2 p.u. The HVDC CB is made to interrupt the fault current before the converter blocks. During fault current interruption, a HVDC CB needs to absorb inductive energy in the system. Figure 3b shows the energy absorbed when interrupting currents for faults occurring at different distances from a converter. It can be seen from this figure that the energy absorbed by the HVDC CB decreases with increasing distance. The difference is caused by the impact of the travelling waves, which superimpose on the transient interruption voltage created by the HVDC CB, on the rate at which the fault current is suppressed. The rate at which the fault current is suppressed depends on the difference between the superposition of the travelling wave and the TIV on one hand and the converter DC bus voltage on the other hand [9]. The higher the difference, the higher the negative di/dt. Depending on point on wave at which the HVDC CB generates the TIV, the superposition of TIV and the traveling waves can be (theoretically) as high as 2.5 p.u. Thus, the di/dt becomes higher when the travelling voltage wave and the TIV superpose in positive way. This in turn affects the amount of electrical energy absorbed from the system.

Figure 4 shows simulation results of fault current interruption by the active current injection HVDC CB. In this case a 150 mH current limiting reactor is used at the ends of each cable to reduce the rate-of-rise of current to within the breaking capability of the prototype HVDC CB assuming a fault neutralization time of 9 ms. Only a fault at 10 km from converter D1 on a line towards converter B1 is simulated. Under normal conditions 1 kA of load current is flowing through the breaker. The breaker receives a trip order when 2 kA current is detected. Figure 4a shows the interrupted current. About 11 kA current is interrupted by the HVDC CB.

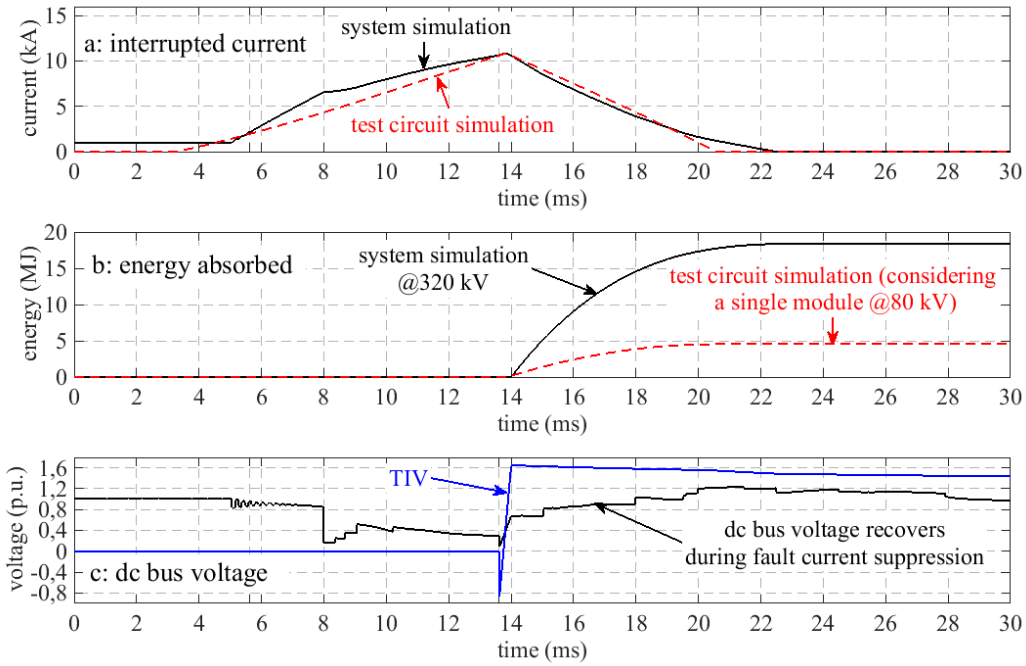

Figure 4: Comparison of DC fault current interruption by active current injection HVDC CB. Solid lines system simulation, dashed lines test circuit simulation a: interrupted current, b: energy absorbed, c: transient interruption voltage (TIV) and dc bus voltage

Figure 4b shows the energy absorbed by the HVDC CB during fault current interruption. In this case about 18.4 MJ energy is absorbed by the HVDC CB. The TIV generated by the HVDC CB and the converter dc bus voltage are shown in Figure 4c. The important point worth noting from this graph is

that the converter dc bus voltage starts to recover the moment the HVDC CB generates the TIV. Although the HVDC CB does not see the system voltage during a fault current suppression period, it has a significant implication on the amount of energy stress on the breaker [9], [13]. The part of the TIV after current interruption is due to the trapped charge remaining in the injection capacitor. This remaining charge can be used during current interruption tests for synthesizing dielectric stress across the main interrupter, which is discussed in the next section.

4. TRANSLATION OF STRESSES INTO TEST REQUIREMENTS OF HVDC CIRCUIT BREAKERS

The important aspects of HVDC CBs that need to be tested are current interruption capability within breaker operation time, the energy absorption capability and the voltage withstand capability (both during and post current interruption). Within the breaker operation time, a test needs to supply current up to the maximum breaking capability of the HVDC CB. It is expected that several breaker units (modules) are put in series for full pole voltage. So far the prototyped HVDC CB technologies have breaker operation time ranging between 2–10 ms with a module voltage rating in the range of 40–120 kV [1]–[4], [14]. Each breaker module interrupts the same current magnitude whereas the energy absorption and the TIV is shared among the series connected modules. With this assumption, simulation results of a test circuit for a single breaker module of 80 kV active injection HVDC CB are superimposed in Figure 4 (the dashed curves in part a and b). A test circuit designed based on low frequency AC short-circuit generator (running at 16.67 Hz) is used in this case. The peak value of the interrupted current is 11 kA in both system simulation and test circuit simulation.

The other important aspect that needs to be tested is the energy absorption capability of the breaker. From system simulation (in Section 3), it is observed that the HVDC CB needs to absorb several MJs of energy. The HVDC CB has the duty to absorb the magnetic energy stored in the current limiting reactor as well as the electric energy injected from the rest of the system during fault current suppression period. Figure 4b shows the energy absorbed by a single module of 80 kV, HVDC CB in a test circuit simulation. The single module of a breaker absorbs about a quarter (4.5 MJ) of the total energy absorbed in a system simulation.

HVDC CBs generate TIV which is higher than the system voltage to suppress the fault current to the residual current value. Hence, the maximum voltage stress depends on the protection level of the surge arresters installed as part of the breaker. The rate of rise of the TIV is dependent on the type of HVDC CB technology under consideration. It is determined by the size of the capacitor in the injection circuit in an active current injection HVDC CB, and the snubber circuits of the power electronic elements in a hybrid HVDC CB. Therefore, the rate of rise of TIV (du/dt) and its maximum value are dependent on the CB parameters. Nevertheless, the generation of the TIV by a HVDC CB must be verified during a test. In addition, a complete test requires post interruption voltage withstand capability. Thus, it is necessary to ensure the application of dielectric stress after current interruption.

5. IMPLEMENTATION OF A TEST CIRCUIT BASED ON LOW FREQUENCY AC SHORT-CIRCUIT GENERATORS

In Section 3, the system simulation results are replicated by a simulation of a test circuit based on low frequency AC short-circuit generators. Given a breaker operation time, the magnitude of the driving voltage, the making angle, circuit inductance and the frequency of the generator become the design parameters for sufficient d*i*/d*t* as well as for sufficient energy supply [9]. However, since the driving voltage is supplied by the AC generator, it cannot provide DC dielectric stress after successful current interruption. The dielectric stress after current interruption can be supplied by a separate DC voltage source but practically this poses several challenges. However, some HVDC CBs, for example, the active current injection HVDC CB have capacitors as part of the CB which is charged during the current interruption process. This capacitor remains charged during the entire energy absorption period

to a value equal to the TIV of the breaker. This can be deployed to provide dielectric stress after interruption.

An equivalent circuit diagram of the test circuit with a 'virtual' test object (TO, the HVDC CB) is shown in Figure 5. The actual implementation of the test circuit in the high-power laboratory (in the absence of HVDC CB) is shown in Figure 6. Three short-circuit generators at 16.67 Hz and three step-up transformers with a ratio of 1:7.7 are used. The master breakers (MB) have to switch off a primary generator-side current of 200 kA (peak) within a single loop. The making switch (MS) needs to be set precisely to switching in the fault current in order to create 'DC like' conditions during the fault suppression time of DC CBs having an operation time up to 10 ms. Two additional elements; namely AC CB (AB1) and the triggered make gap, are added to the circuit for galvanic isolation of the supply circuit from later to be added DC source and over current protection respectively, as described later.

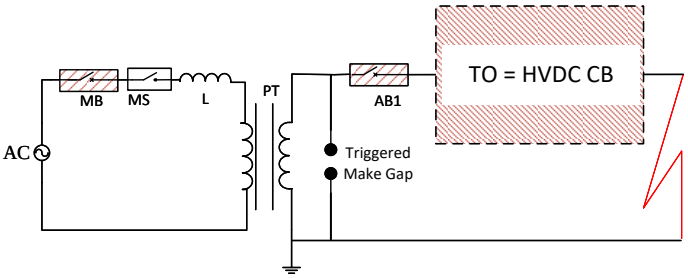

Figure 5: Test circuit based on low frequency AC short circuit generators

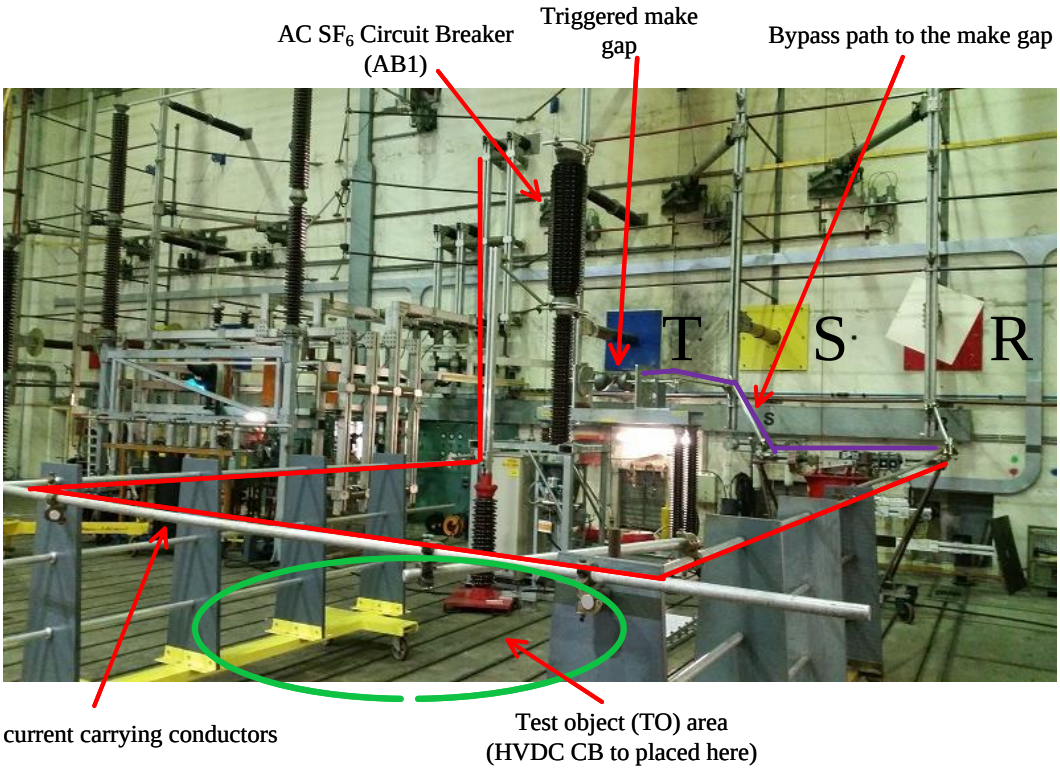

Figure 6: Actual HVDC CB test set-up in the high-power laboratory (Generators and transformers behind the wall). A test object to be connected between two phases, R and T.

A preparation test in the absence of a HVDC CB has been conducted. The results of the test are shown in Figure 7. The graph in Figure 7a shows the prospective current from the actual test result (see the red trace). The prospective current increases to a peak value of 26.5 kA which is higher than the

breaking current of the HVDC CB. The voltage measurements are shown in Figure 7b. The generator voltage after transformation, at the terminals of the HVDC CB at the test has a peak value of 46.5 kV.

To get insight into the phenomena occurring during test, current interruption by a (simulation) model of an active current injection HVDC CB in a test circuit having the same circuit parameters as the practical installation at a test facility is simulated and plotted (blue and black curves) on top of the experimental results (red curves) in Figure 7. The breaker receives a trip order when the current reaches 3 kA. A breaker operation time of 8 ms is assumed in the simulation. It can be seen from Figure 7a that about 16 kA current is interrupted by the HVDC CB. Figure 7b depicts the expected TIV of the breaker. Figure 7c shows the energy that would be absorbed by the test breaker when interrupting the current at 16 kA. About 5 MJ of energy is absorbed by the breaker and this is related to the energy stored in circuit inductance (27.5 mH) as well as the part supplied by the generators. If increased energy stress is needed, the generator voltage can be increased. In order to keep the breaking current the same, the circuit inductance must then be proportionally increased. The dashed trace in Figure 7c shows the energy absorbed by the HVDC CB when the generator voltage is increased from 46.5 kV peak to 70 kV peak. The same current is interrupted in both cases, however, about 9.2 MJ energy needs to be absorbed in the latter case.

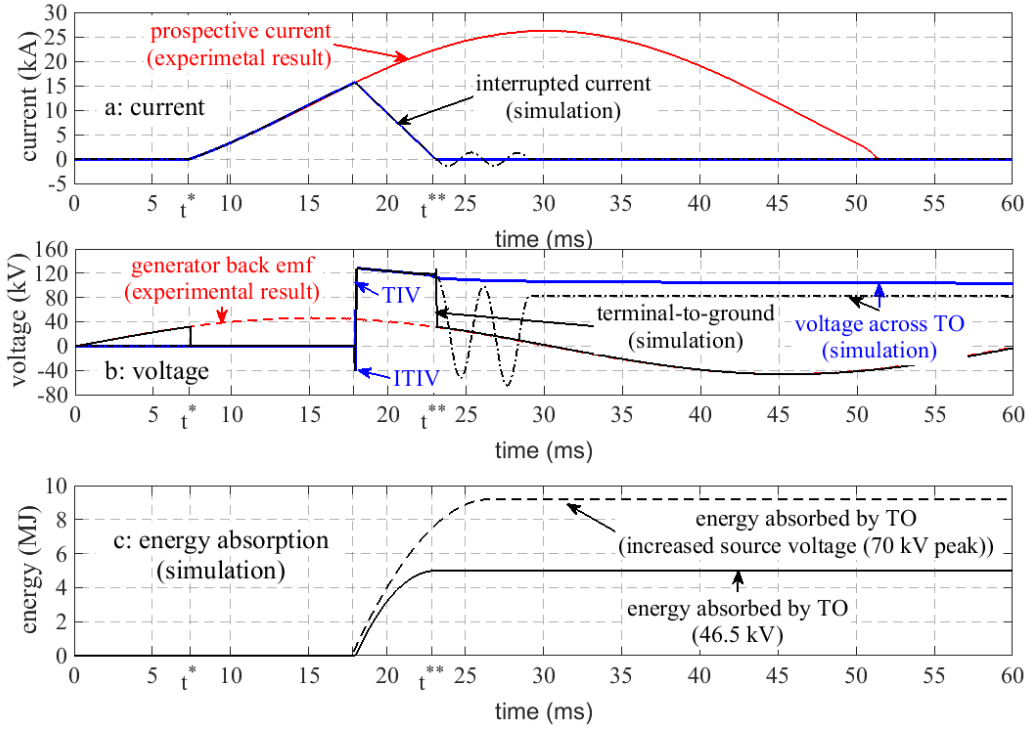

Figure 7: Simulation results of current interruption by active current injection HVDC CB in low frequency AC short-circuit generator test circuit

After current is suppressed to (nearly) zero by the test breaker, there will be a damped oscillation between the charged injection capacitor of the breaker and the circuit inductance (see the dash-dotted curve in Figure 7a and b). The magnitude of the oscillating current is determined by the difference between the voltage of the charged capacitor and the instantaneous voltage of the generator the moment current is suppressed to zero and the frequency is determined by the capacitance and the total inductance in the circuit including the inductance in the injection branch of the breaker. Now, if the auxiliary AC breaker (AB1 in Figure 5) interrupts to disconnect the source side from the test breaker the moment the short-circuit current is suppressed to zero, the remaining charge on the capacitor of the HVDC CB can be used to provide dielectric stress to its main interrupter. This can be seen by blue traces in Figure 7a and b. The voltage across the capacitor is slightly decaying since it is discharging through the surge arrester. In order to interrupt current the moment it reaches zero, AB1 has to start arcing before current is interrupted by the HVDC circuit breaker.

A major challenge of using AC short-circuit generators for testing HVDC CBs is the fact that a large prospective current will flow in case the test breaker fails to clear. This will result in two undesirable conditions. First, the test breaker may not be able to withstand the large current and could subsequently be damaged if proper protection against such a situation is not prepared. Second, it may damage the AB1 especially because of the long arc duration due to the low frequency. The former issue becomes critical when HVDC CBs having power electronic components are tested. Such breakers have a short breaker operation time leading to a requirement of high di/dt to reach the maximum breaking current within the breaker operation time. If such a breaker fails to clear the current, much larger current flows than these components can handle. The experimental result having di/dt of 3.5 kA/ms is demonstrated in reference [9]. The test result in that reference showed the peak prospective current of 40 kA.

Therefore, to avoid damage to both the test breaker and the auxiliary breaker, a parallel path provided by a triggered make (spark) gap as shown in Figure 5 (see its implementation Figure 6) is proposed. The make gap is triggered only if a predefined current threshold beyond which the test breaker cannot clear is reached. The proposed technique is experimentally verified and the test result is shown in Figure 8 where current commutates from the TO path to the triggered make gap bypass path. Sufficient voltage is needed in the test object path for ignition of the make gap. This is provided by the arcing voltage (several hundreds of Volt) of the AC auxiliary breaker (AB1). This was sufficient to commutate the current fully into the triggered make gap path.

The impact of the gap length was also investigated. Increasing the gap length slightly increased the commutation time. Moreover, the use of triggered make gap can serve a double purpose. The gap length can also be set for overvoltage protection to protect the test installation. During the actual test of the HVDC CB, the gap length must be set for overvoltage higher than the TIV of the test breaker with sufficient margin so that it does not interfere during the normal interruption process. The gap length was set to 15 cm for the test shown in Figure 8 and this is sufficient to withstand voltage up to 275 kV.

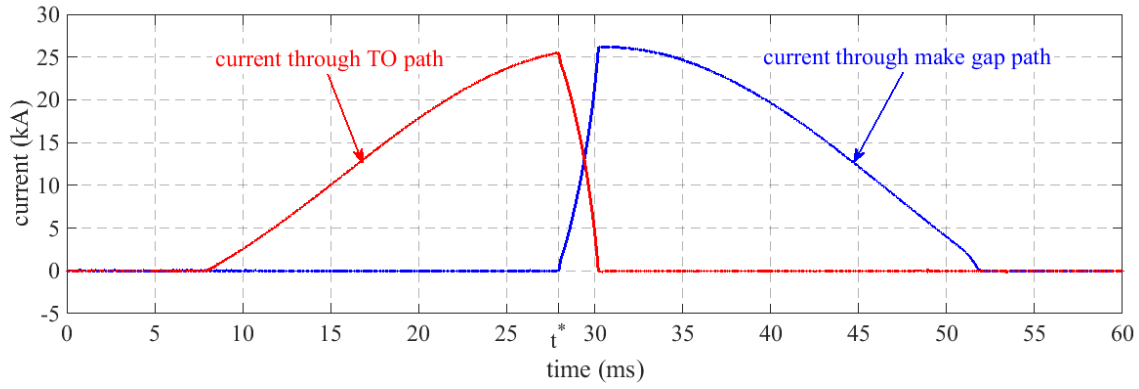

Figure 8: The test result showing current commutation from test object (TO) path to triggered make gap path

6. CONCLUSION

This paper analyzes fault currents in a multi-terminal HVDC grid through simulation. Three distinct time periods following the occurrence of fault, distinguished by the different fault current contributions during each period, are identified; submodule discharge, arm current decay and AC in-feed periods. HVDC circuit breakers are expected to operate on the rising edge of the fault current. Current limiting reactors are used to reduce the rate-of-rise of fault current (di/dt), in order to match it to the combination of breaker operation time and maximum current interruption capability. HVDC CBs need to absorb the energy stored in the reactors and the energy supplied by the HVDC grid during current interruption.

Fault current interruption by models of HVDC CBs is also investigated with the purpose of studying the stresses on the breaker. A test circuit based of low frequency AC short-circuit generator is designed to replicate the stresses obtained from system simulation. It is shown that by controlling the making angle and source voltage magnitude, the AC short circuit generator based test circuit can supply the necessary current and energy stresses to HVDC CBs. Experimental demonstration of prospective test current and voltage is performed to validate the method in a high-power laboratory. Techniques to address two major issues related to the use of AC source: dielectric stress after current interruption and overcurrent protection in case a test breaker fails, are introduced. The latter issue is experimentally validated.

7. ACKNOWLEDGEMENT

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 691714.

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