

D10.9: Reporting on HVDC circuit breaker testing

PROMOTiON – Progress on Meshed HVDC Offshore Transmission Networks
Mail info@promotion-offshore.net
Web www.promotion-offshore.net

This result is part of a project that has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

Publicity reflects the author's view and the EU is not liable of any use made of the information in this report.

CONTACT
rene.smeets@kema.com

DOCUMENT INFO SHEET

Document Name: Reporting on HVDC circuit breaker testing
Responsible partner: KEMA Labs
Work Package: WP10
Work Package leader: René Smeets
Task: 10.9
Task lead: René Smeets

DISTRIBUTION LIST

APPROVALS

	Name	Company
Validated by:	Nadew Belda	KEMA Labs
	Cornelis Plet	DNV GL
Task leader:	René Smeets	KEMA Labs
WP Leader:	René Smeets	KEMA Labs

DOCUMENT HISTORY

Version	Date	Main modification	Author
1.0	20200615	Original	René Smeets
2.0	20200630	Commented	Nadew Belda
3.0	20200708	Modified	René Smeets
4.0	20200907	Modified after review	René Smeets

WP Number	WP Title	Person months	Start month	End month
10	Circuit Breaker Performance Demonstration		25	57

Deliverable Number	Deliverable Title	Type	Dissemination level	Due Date
10.9	Reporting on HVDC circuit breaker testing		Public	Sep. 30 2020

LIST OF CONTRIBUTORS

Work Package and deliverable involve a large number of partners and contributors. The names of the partners, who contributed to the present deliverable, are presented in the following table.

PARTNER	NAME
KEMA Labs	René Smeets, Nadew Belda
MEU	Hiroki Ito, Takashi Inagaki
SciBreak	Simon Nee
ABB	Semere Mebrahtu-Melake
DNV GL	Cornelis Plet

CONTENT

- Document info sheet..... i**
 - Distribution listi
 - Approvalsi
 - Document historyi
- List of Contributors ii**
- Executive Summary 5**
- 1 Introduction..... 7**
 - 1.1 Purpose 7
 - 1.2 Motivation 7
 - 1.3 Document structure 7
- 2 Motivation of the activities 8**
- 3 HVDC circuit breakers in Chinese grids..... 11**
- 4 HVDC network fault analysis..... 12**
- 5 Simulation of HVDC circuit breaker operation 15**
- 6 HVDC circuit breaker test requirements 19**
 - 6.1 Introduction 19
 - 6.2 General requirements 19
 - 6.3 Fault current interruption requirements 21
 - 6.4 Contribution to standardization 24
- 7 Component stresses 25**
 - 7.1 Introduction 25
 - 7.2 Mechanical switching devices in HVDC circuit breakers 25
 - 7.3 Experimental observations on vacuum Interrupters 26
 - 7.4 Energy absorbing systemS in HVDC circuit breakers 27
 - 7.5 Experimental observations on MOSA absorbers 28
- 8 HVDC circuit breaker test circuit requirements..... 30**
 - 8.1 Generic test-circuit requirements 30
 - 8.2 Test circuit selection 31
 - 8.3 Modular Testing of HVDC circuit breakers 33
 - 8.4 Realisation of test circuit..... 34
 - 8.5 Validation of test circuit..... 36

- 9 Demonstration of HVDC circuit breakers 38**
 - 9.1 VSC Assisted resonant Current Injection DC breaker demonstration 38
 - 9.2 Active current injection HVDC circuit breaker demonstration 38
 - 9.3 Hybrid HVDC breaker demonstration 39
 - 9.4 Summary overview 39

- 10 External output and dissemination..... 41**
 - 10.1 Demonstrations 41
 - 10.2 Peer reviewed journal articles 41
 - 10.3 Conference contributions..... 41
 - 10.4 Public tutorials and workshops 42
 - 10.5 Award 43

- 11 References 44**

EXECUTIVE SUMMARY

This document reports on the complete research and development track leading to the public demonstration of HVDC circuit breaker technology. Thus, it can be assumed that the Technology Readiness Level of this technology has been raised to level 8: System complete and qualified.

Since HVDC grids are almost completely non-existent, models of conceptual HVDC grids are used to study the impact of faults on such grids, especially in terms of fault current levels, voltage collapse as well as impact on converter operations. HVDC grids require ultra-rapid fault detection and location protection strategy consisting of relays and circuit breakers that need to act within milliseconds to isolate the faulted section(s). Through system studies, understanding is gained on the mitigating measures that can reduce voltage collapse, such as series reactors that can delay voltage collapse.

Such studies are also used, and presented in project deliverables, to quantify the electrical transients that the circuit breaker has to deal with. As a result, quantities like rate-of-rise of fault current, energy to be dissipated are evaluated. Combined with a study of AC circuit breaker standards, this has led to a general high-level set of standards for HVDC circuit breakers, including all its functionalities.

An experimental HVDC circuit breaker is set up in the high-power laboratory to study the impact of current interruption on two key components that are common in most HVDC technologies: vacuum interrupter and metal oxide surge arrester for energy absorption. Limits of performance of these components are researched and quantified.

As a next step, a detailed set of test requirements is set up, consisting of clearly defined test-duties, to be followed in order to qualify the breaker for its main task: fault current interruption under full power condition. These test requirements are agreed among the manufacturers of three varieties of HVDC circuit breakers:

- Active current injection technology (without power electronics and arc interruption with a high-speed mechanical circuit breaker);
- Hybrid technology (interruption with power electronics and insulation with high-speed switch) and
- VSC assisted resonant current injection technology (with power electronics and arc interruption with a high-speed mechanical circuit breaker)

Then, a study evaluating practical aspects as well as comparing performance possible test circuits singled out the test circuit based on low-frequency AC short-circuit generators as technically the best option to replicate the stresses as in service, quantified by a number of essential phases in the interruption process. The suitability of this circuit is demonstrated with an 80 kV industrial HVDC circuit breaker module interrupting 16 kA of fault current.

As the last step, all three technologies, up to rated voltage 350 kV and fault current 20 kA were demonstrated regarding their fault interruption capability, using the defined test-requirements. The demonstrations were performed in the presence different stakeholders such as transmission system operators, project developers and many possible users of HVDC circuit breakers witnessing the live test.

In all cases, this was the first time a complete breaker (prototype) was submitted to a full-power test.

1 INTRODUCTION

1.1 PURPOSE

The purpose of this document is to summarize the steps in research and development that led to demonstration of the fault current interruption capability of HVDC circuit breakers, a key component of future meshed HVDC grids. Being 'terra incognita' since such grids do not yet exist, the work covers the entire line of development, from fault simulation studies in conceptual grids up to and including full-power laboratory testing in newly developed test circuits.

1.2 MOTIVATION

The motivation of this document is to report an overview of the activities in PROMOTioN WP5 and WP10 aimed at demonstration of a significant technology readiness level of three technologies of HVDC circuit breakers by full-power testing in an independent (not manufacturer's) related test-laboratory.

1.3 DOCUMENT STRUCTURE

This document consists of the following parts:

- Explanation of the rationale of having a technology available to actively protect HVDC grids by selective elimination of faulted sections and thus guaranteeing the integrity of the complete grid.
- A short overview of the status of HVDC circuit breaker application in existing (pilot) HVDC grids and a commercial 500 kV grid under construction in China.
- Simulation study in order to identify the response of a simplified model of HVDC grid to a fault.
- Electrical stresses resulting from interruption of such a fault that impacts a (modelled) HVDC circuit breakers as seen from outside.
- A set of general test requirements that follows from system simulation studies and from a study of AC equipment standards.
- Contribution to emerging international standards of DC circuit breakers and switchgear.
- Analysis of the stresses on subcomponents of HVDC breakers, based on experimental laboratory studies of an experimental HVDC circuit breaker.
- Identification of critical phases in the fault interruption process and definition of verification tests, as agreed upon by all work package partners.
- Evaluation of possible test circuits with respect to performance, availability, etc., leading to the choice of a test circuit powered by low-frequency AC generators as the best compromise to cover all critical phases in the interruption process.
- Demonstration of the capability of this circuit with a full-scale HVDC breaker module.
- Demonstration of three technologies of HVDC circuit breakers regarding their capability to fulfil the fault current interruption requirements as defined within the project.
- Dissemination activities outside the project.

2 MOTIVATION OF THE ACTIVITIES

Switching has been the prime technology to control the safe flow of power. In traditional AC systems, a large number of switchgear can be identified for a myriad of different functions. The most critical switching device is the circuit breaker; a device that can make (switch on) and break (interrupt) fault currents during a short-circuit in a system [1, 2]. Its function is to isolate faulted sections of the power system in a short time (< 100 ms) so that power flow in the healthy parts of the system remains unaffected. In a traditional point-to-point HVDC transmission systems, however, there is no need for such a dedicated fault current interruption device. Normally, a fault in such a system automatically leads to a total loss of power in the affected pole line. Fault current in such systems can be cleared by converter control actions at either end or by AC circuit breakers at the AC side.

Almost all of the HVDC systems in operation in the world are point-to-point systems: a single HVDC link connecting two HVDC stations nearby large-scale generation, e.g. a large hydro power plant and a large load centre. With the need of connecting huge amounts of large sized generators (commonly renewable sources) spread across a large surface, meshed HVDC grids or multi-terminal HVDC systems [3] are being realized in small scale and conceived in a large scale, aimed to harvest hundreds of gigawatts in a few decades from now [4]. The meshed or multi-terminal topology greatly enhances reliability, system stability and electricity trade. Topological solutions are studied intensively [5, 6].

A key requirement of such meshed HVDC grids is the possibility to de-energize faulted parts and/or branches of the grid (submarine cables in an offshore grid) without endangering the integrity of the system as a whole.

Faults are inevitable. In submarine cable links they occur at a frequency in the order of 3 faults per 1000 km/year in HVAC applications [7] and 0.2 – 2.0 per 1000 km/year in HVDC projects [8]. During system restoration, there is no or limited energy flow. Especially in systems having submarine connections, repair times can be very long; a survey among European TSOs reports an average repair time of 60 days [9].

The HVDC circuit breaker [10, 11] is a good candidate to interrupt any possible fault current and isolate the faulted section from the grid in a very short time in order to maintain system integrity.

Other options of HVDC grid protection include the use of converters having fault-blocking capability (full-bridge topology). In this case, the grid de-energizes shortly and fault current is reduced to levels allowing separation of the faulted section under near-zero voltage and current conditions [12, 13]. This requires fast mechanical disconnectors to be installed at the ends of each DC line. The DC side circuit must completely de-energize before these fast disconnecting switches are operated.

Anyhow, costs of protection will be rather high: the investments for system protection (including HVDC circuit breakers) for HVDC grids are estimated up to 9% of the total project costs [6].

Compared to AC fault current interruption DC fault current interruption is challenging because of the following reasons [14]:

1. There is no natural current zero in DC systems unlike in AC systems [1, 2]. This implies that there is no moment when the inherent magnetic energy ($\frac{1}{2}LI^2$) in the system is zero. For AC current interruption, current zero provides the opportunity to interrupt at the moment when there is no magnetic energy in the system. Thus, the AC circuit breaker does not need to absorb magnetic energy in the system whereas the DC circuit breaker must have a provision to absorb several Megajoules of the energy in the (faulted part of the) system. As an example, the magnetic energy stored in a 100 km faulted line carrying 15 kA of current is around 11 MJ. Converted into mechanical terms, this is equivalent to the kinetic energy of a 30 ton truck running at 100 km/h, that has to be stopped in a matter of a few milliseconds. Whereas a buffer would be designed to bring the truck to a standstill, a sustained counter voltage generated by the DC circuit breaker has to counteract the DC fault current and must bring fault current, to a “standstill”.

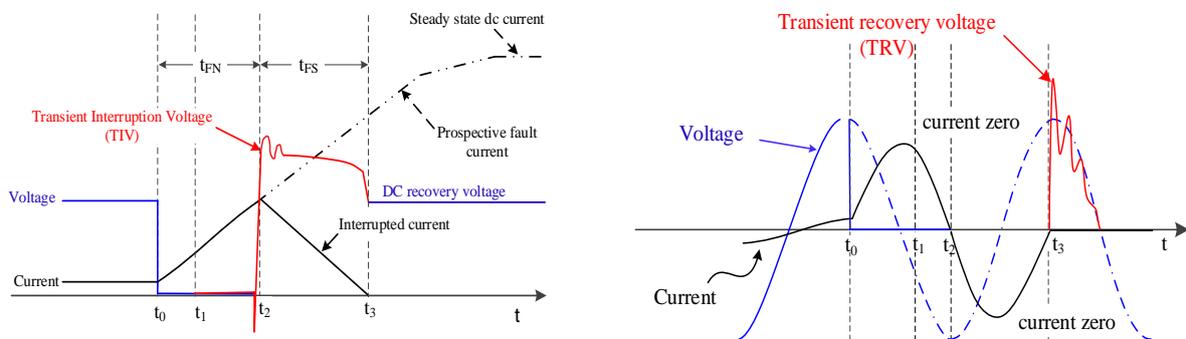


Figure 1: Schematic of DC (left) and AC (right) fault current interruption

2. The peak value of fault current in DC systems is limited only by the resistance (R) in the current path, whereas in AC systems it is the inductance (L) of the conductors that limits the fault current. In power systems, $R \ll \omega L$ (standardized value of $\omega L/R = 14 - 17$). This implies that, provided the DC source is strong enough, very high prospective DC fault currents can emerge, see Figure 1. Therefore, HVDC breakers need to act fast, around ten times faster than AC breakers to clear a fault current on its rising edge before reaching its peak value. With rate-of-rise of fault current (di/dt) in the range of a few to several kA/ms [15], breaker operation time may not exceed 8 - 10 ms in order to handle technically feasible values of peak fault current (I_{pk}). Though this current is much lower than the rated short-circuit breaking current of AC breakers (63 - 80 kA), the challenge in DC current interruption is in realizing a short breaker operation time in order to limit undesirable consequences for system and converter. In addition, rapid response also calls for the need of very fast DC fault protection. Values in the range of 1 - 3 ms of relay time (t_{RY}) are reported as feasible [16].

3. To interrupt fault current, HVDC circuit breakers need to quickly generate and sustain counter voltage exceeding the system voltage. This voltage is henceforth termed as Transient Interruption Voltage (TIV) – see Figure 1 whereas there is no such need for an AC current interruption. Rather an AC circuit breaker needs to sustain a system imposed transient recovery voltage (TRV) imposed by the system.

The different challenges of both type of circuit breakers has its impact on testing. Testing of HVDC circuit breakers is fundamentally different from that of AC circuit breakers as both voltage across and current through the circuit breaker exist at the same time during the energy absorption phase, leading to an energy absorption

requirement.

One of the goals of PROMOTioN is to demonstrate the performances of the proposed HVDC circuit breaker technologies with full power testing at an independent short-circuit laboratory.

Before commissioning HVDC circuit breakers in practical applications, adequate verification of its ratings and functionality through testing is crucial. Meaningful demonstration of HVDC circuit breaker technology is achieved when the applied tests accurately reflect realistic fault conditions, e.g. in multi-terminal HVDC networks. Hence, to accelerate the realization of the envisaged MTDC networks, test facilities sufficiently representing a practical DC system under various conditions are designed and developed.

In standardization, so far there are no internationally accepted specified and quantified test requirements of HVDC circuit breakers let alone a standardized method to test these devices.

In the project, a test program is agreed among the participating manufacturers on a test program covering the main duty of HVDC circuit breakers: breaking of current up to its rated peak fault current.

3 HVDC CIRCUIT BREAKERS IN CHINESE GRIDS

At the time of writing, HVDC circuit breakers are in service in two projects in China. One is in the ± 160 kV three-terminal Nan'ao project (2013) [17], operated by China Southern Power Grid, where active current injection HVDC circuit breakers are installed [18], see Figure 2. In another project, hybrid HVDC breakers were installed in the ± 200 kV Zhoushan five-terminal island link (2014) [19, 20] from State Grid Corporation of China, see Figure 3.

The realization of the Zhangbei meshed ± 500 kV HVDC onshore grid [21, 22] also a project in China, will initially include 16 HVDC breakers of five different Chinese suppliers offering three designs of hybrid type [23, 24], current injection [25] and coupled negative voltage technology [26], see Figure 4, Figure 5 and Figure 6 (Courtesy of State Grid Corporation of China). These circuit breakers are installed 2019-2020.



Figure 2: 160 kV active current injection HVDC circuit breaker [17]



Figure 3: Two 200 kV HVDC hybrid circuit breakers [24]



Figure 4: 500 kV hybrid HVDC circuit breaker



Figure 5: 500 kV HVDC active current injection circuit breaker



Figure 6: 500 kV HVDC coupled negative voltage circuit breaker

4 HVDC NETWORK FAULT ANALYSIS

Identifying the factors determining the fault currents in meshed multi-terminal HVDC networks was the goal of task 5.1 [27]. Existing technical literature on HVDC network fault behaviour and analytical fault analysis techniques were reviewed and simulation studies on a benchmark study network [28] shown in Figure 7 were carried out. Fault analysis has been carried out by means of PSCAD/EMTDC simulation software on a multi-terminal bipolar ± 320 kV HVDC benchmark study network fed by half-bridge (HB) modular multi-level converters (MMC) in a voltage source converter system (VSC) to study the various fault current contributions and their characteristics. The effects of network topology, series reactors, fault location, converter blocking logic, AC network strength and line type on the rate of rise and the magnitude of the fault current have been analysed qualitatively.

Simulation results can be summarized as follows [29]:

1. A fault occurs by a breakdown of the insulation system, which results in a voltage transient which travels along the cable, line away from the fault location and invokes, first, the discharge of any charged capacitances resulting in a current limited only by any series impedance of the cable. These discharges result in the first transients that last only for few milliseconds. Then, the AC sources start feeding the short circuit current limited by AC side impedance and DC side resistance.
2. At impedance boundaries, a part of the negative voltage wave is transmitted and the rest is reflected. At HB MMC VSC terminals, the voltage transient triggers the discharge of the submodule capacitors leading to a (near linear) rise in current limited only by the converter arm reactor.
3. In order to protect the internal circuitry, an HB MMC VSC converter blocks, as shown in Figure 8 governed by a protection algorithm combining arm and output overcurrent and DC under-voltage information. This turns the converter essentially into an uncontrolled diode rectifier. Prior to blocking, the increasing DC output current of the converter has little impact on the AC current, so all energy is supplied by the submodule capacitors.

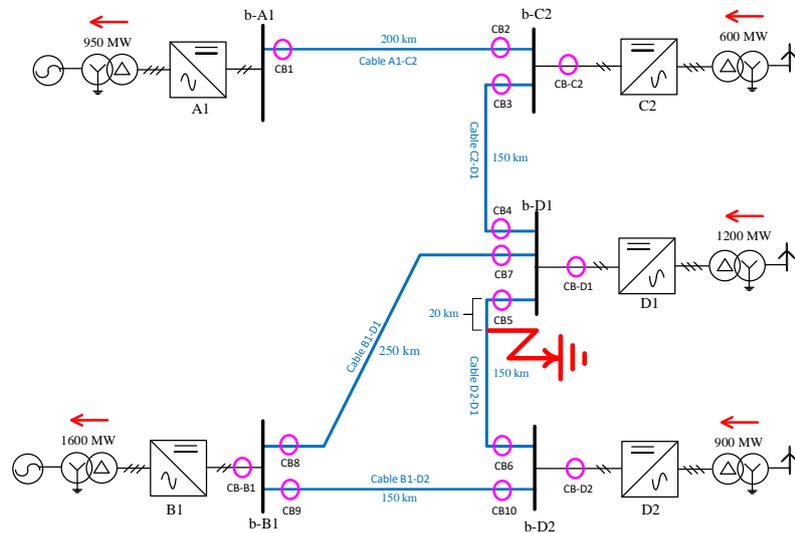


Figure 7: Five terminal meshed HVDC benchmark network based on CIGRE WG B4-57

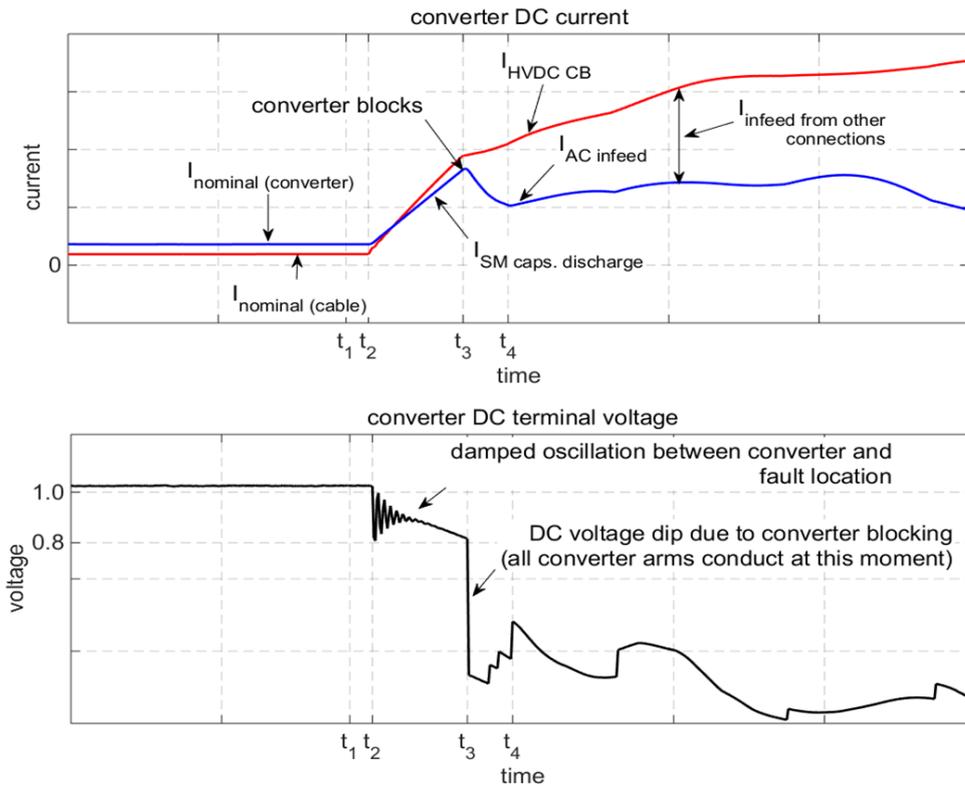


Figure 8 – Fault response of converter and fault current at location of HVDC circuit breaker

4. Because of the different travelling times of the voltage transients to various locations in the network, converters at different distances from the fault block at different times as shown in Figure 9

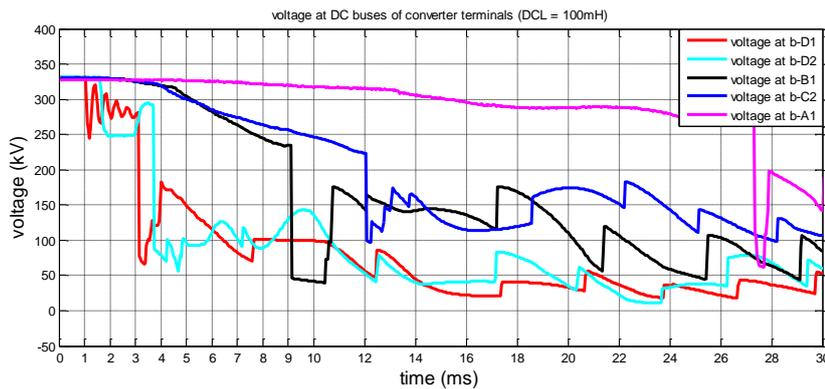


Figure 9 - Converter terminal voltages after occurrence of a fault (series inductor = 100 mH)

5. After blocking, the prospective output current of the converter is determined by the resistance between the fault, the converter resistance, the converter transformer impedance and the AC network strength.

6. Series reactors at the ends of cables reduces/limits the rate-of-rise of fault currents. The higher the inductance of the reactor, the lower the rate-of-rise of fault current. This spreads out the arrival times of the voltage transients.
7. Because of the series reactors, the time until converter blocking is increased and the converters are enabled to regulate their terminal voltage. The higher the inductance of the reactor, the smaller the voltage drop at the converter terminal before it blocks.
8. As long as a converter can regulate its output voltage (in the presence of series reactors), the discharge of adjacent feeders is very limited.
9. The moment a converter blocks, the terminal voltage collapses inducing discharge of adjacent cables.
10. Rate-of-rise of current in adjacent cables is suppressed in the presence of multiple series reactors in the fault current path.
11. The rate-of-rise of fault current through a HVDC circuit breaker increases with increasing numbers of adjacent cables (or converter stations) connected to its bus.
12. The reflecting waves cause periodic voltage swings at the cable ends of both positive and negative polarity.
13. Depending on the length of the cable and the location of the fault, the reflection of a positive voltage transient may increase the average voltage at the cable end and reduce the rate-of-rise of fault current.
14. Because of the reactive nature of overhead lines, their presence in a DC network has a similar mitigating effect to that of a series reactor and decreases the rate-of-rise of fault current.

These qualitative descriptions may be used to predict the worst case of fault condition in a given HVDC network. The worst case conditions are always network specific and must under all circumstances be less severe than the maximum ratings of a HVDC circuit breaker. From the analysis it follows that the inductance of series reactors may be adjusted in order to change the stresses or demands placed on converter stations and/or HVDC circuit breakers. A detailed description of these fault current contributions is given in deliverable 5.1 [27].

5 SIMULATION OF HVDC CIRCUIT BREAKER OPERATION

In order to study the stresses on HVDC circuit breakers during DC fault current interruption, the detailed operation principle of various technologies of HVDC circuit breakers has been analysed:

- An active current injection HVDC circuit breaker with current injection based on pre-charged capacitor discharge, shown in Figure 1010;
- VSC assisted resonant current injection (VARC) type of HVDC circuit breaker, an active injection type of circuit breaker with an electronic current injection circuit. Modelling of this type of breaker is described in work package 6;
- two types of hybrid power electronic HVDC circuit breakers, an IGBT-based version of which is shown in Figure 11 was modelled in PSCAD [30].

The models are available in deliverable 5.2. The models of these circuit breakers are inserted in the benchmark study grid which was defined in deliverable 5.1 [27] and simulation results were analysed and reported in deliverable 5.3 [29].

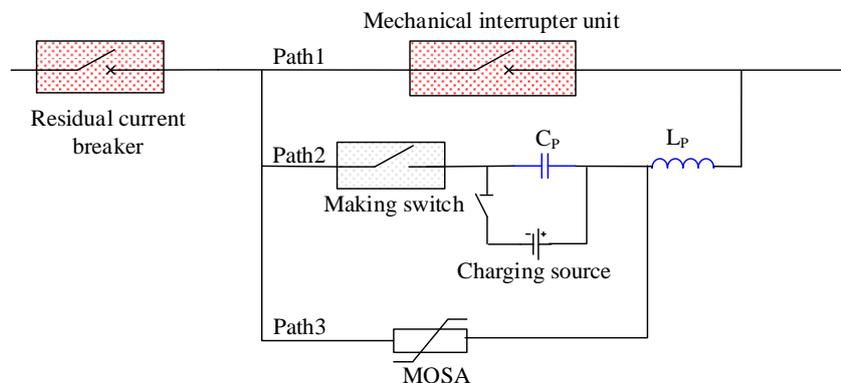


Figure 10 – Model of mechanical HVDC circuit breaker with active current injection

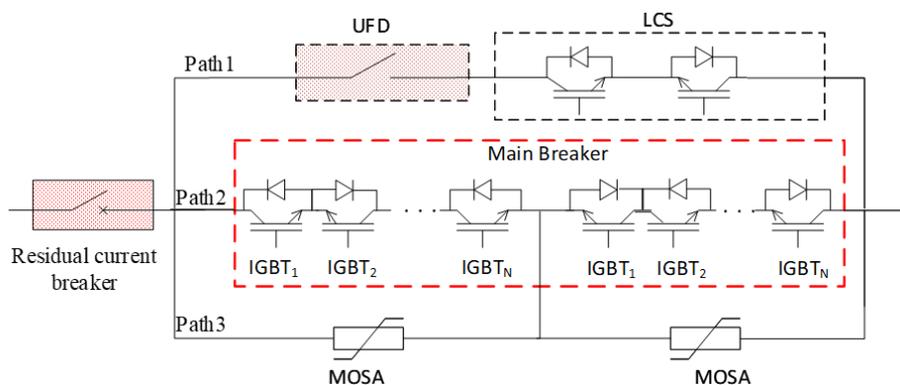


Figure 11 – Model of hybrid HVDC circuit breaker

For all the considered HVDC circuit breakers, it is necessary to have a series DC current limiting reactor in series with the HVDC circuit breaker. Assuming fast enough protection the inductance of the reactor along with each circuit breaker technology depends mainly on the breaker operation time (the time from trip order until the circuit breaker can withstand the maximum transient interruption voltage (TIV)) of the circuit breaker. In general, the DC current limiting reactor is chosen to:

- Limit the magnitude of the fault current occurring in the protection zone of the circuit breaker to within the interruption capability of the circuit breaker during fault current neutralization time.
- Ensure continued controlled operation of the healthy part of the system by avoiding the voltage collapse of the entire DC grid during the fault neutralization time. In doing so the series DC current limiting reactor also provides more time for the protection system to detect and locate the fault.

In the simulations, a 150 mH reactor is used in series with the active current injection HVDC circuit breaker and a breaker operation time of 8 ms is assumed. A peak current of about 12 kA is interrupted and an amount of energy of about 25 MJ is absorbed by the breaker. In this case the converters at the ends of the faulted cable block as either of these converters cannot continue its controlled operation during the relatively long fault neutralization time. It must be noted that the maximum interrupted current and the corresponding energy absorbed by a circuit breaker highly depend on the system architecture and associated parameters.

For the hybrid HVDC circuit breakers, a breaker operation time of 2 ms is assumed. Due to the shorter internal operation time, a 100 mH DC current limiting reactor is used in series with the hybrid HVDC circuit breakers. Hence, in the simulation a peak current of about 8.5 kA is interrupted and an amount of energy of circa 10 MJ is absorbed by the hybrid circuit breaker. With the assumed relay time, the fault can be cleared before any of the converters in the system block.

For all studied HVDC circuit breakers the DC short-circuit current breaking process can be split into four distinct states, as illustrated in Figure 12. The stresses, as seen from outside the HVDC circuit breaker, in each state are as follows:

- ❶ Normal closed position ($t < t_2$) - Before the tripping of the HVDC circuit breaker. The HVDC circuit breaker experiences:
 - Dielectric stress due to the rated voltage U_s on the support structure – terminal to ground dielectric stress
 - Thermal stress due to heating by nominal continuous current I_{con} passing through the normal current branch
 - Thermal stress due to heating by rated short-time withstand current passing through the normal current branch, or by initial rise of fault current before tripping
- ❷ Fault current commutation ($t_2 < t_3$) – From tripping of the HVDC circuit breaker until start of conduction of energy dissipation branch. The HVDC circuit breaker experiences:

- Rising short-circuit current which needs to be commutated from the continuous current branch, through the commutation/ current injection branch, into the energy dissipation branch. The short-circuit current can be bidirectional and have various rates of rise with maximum rated di/dt , and a peak current of I_{pk}
- Low positive voltage across the terminals, based on impedance/voltage drop in the commutation branch
- Residual voltage transient across terminals is experienced by mechanical HVDC circuit breakers with active current injection at the end of this period. The potential peak voltage of the transient is inversely proportional to the interrupted current with a maximum equal to the injection capacitor charging voltage
- Fault current suppression ($t_3 < t_4$) – From the start of conduction of energy dissipation branch until short-circuit current is suppressed to zero. The HVDC circuit breaker experiences:
 - Thermal stresses in the energy dissipation branch up to the rated energy absorption E_{rated}
 - Dielectric stress due to the Transient Interruption Voltage V_{MOSA} with a maximum duration up to the rated fault current suppression time ΔT_{fs}
 - Dielectric stress between terminal and ground (across support structure) which can be in the range between 1.5 – 2.5 p.u.
- ④ Normal open position ($t > t_4$)
 - Dielectric stress across terminals and on support structure equal to the rated line voltage U_s . The duration is from the moment of current suppression (end of conduction of energy dissipation branch) until the operation of the residual current breaker.

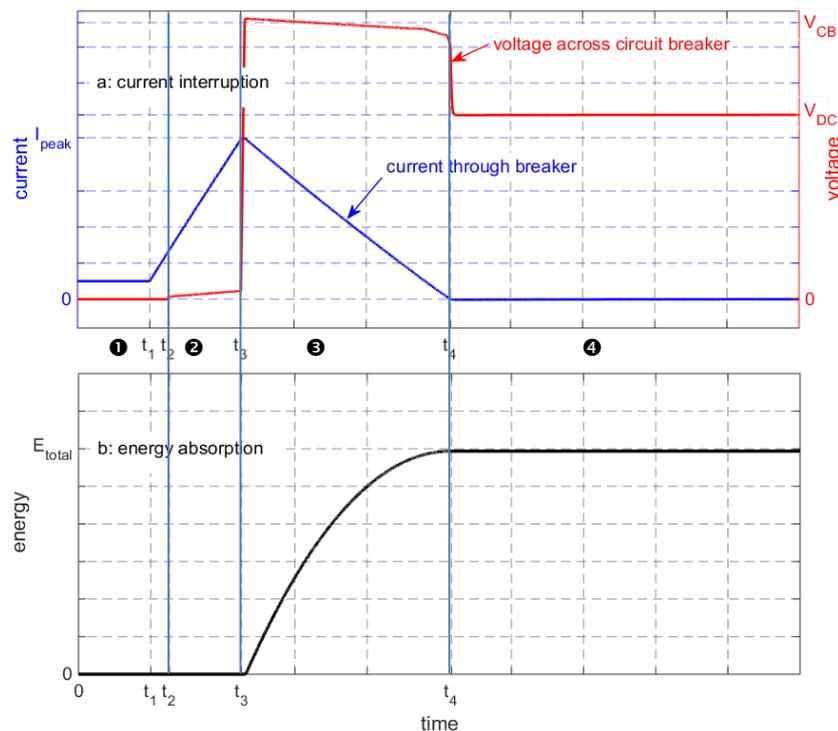


Figure 12 – Typical electrical stresses on an HVDC circuit breaker during DC short-circuit current breaking

For all the circuit breakers, it is observed that the system voltage starts to recover even before the fault current is completely cleared. Thus, from the system perspective, the most important phase of the current interruption process is, therefore, the fault neutralization time.

6 HVDC CIRCUIT BREAKER TEST REQUIREMENTS

6.1 INTRODUCTION

In general, to stress the HVDC circuit breakers as in service, a test circuit should provide sufficient current, voltage and energy. The specific details are mainly dependent on the system under consideration. The key functionality of any HVDC circuit breaker system is to suppress the fault current to a very small value. In order to realize this, the following requirements of an HVDC circuit breaker, regarding fault current interruption capability must be verified:

1. Capability to create a local (inside the breaker system) current zero without restrike/breakdown of mechanical switches/interrupters or thermal overload of power electronic components at rated DC fault current;
2. Generation of sufficient counter voltage to initiate fault current suppression;
3. Capability of energy absorption components to absorb energy during fault current suppression as in service. Depending on the rated test sequence, this capability must be demonstrated several times within a defined sequence;
4. Capability to interrupt low-current and continuous current;
5. Capability to withstand the rated DC voltage after the current interruption process;
6. The breaker operation time: the minimum time at which the circuit breaker reaches the TIV withstand level after trip order;
7. The maximum current interruption: The maximum current the breaker can interrupt within the breaker operation time;
8. The number and frequency of operation: the number of interruption operations that the circuit breaker can perform before thermal run away occurs in its surge arresters. The interruption interval needs to be defined, e.g. like auto reclosure in AC circuit breakers;

6.2 GENERAL REQUIREMENTS

To date, there is no international standard describing the requirements, applicable tests and test procedures of HVDC circuit breakers. Initially within the project, a general guideline for lists of tests that shall be applied to HVDC circuit breakers for its operation and performance verification has been developed and reported in deliverable 5.4 [31].

Test procedures described in IEC standards for AC switchgear (IEC 62271-1, IEC 62271-100, IEC 60060-1) as well as the IEC standards of DC switchgear for railway applications (IEC 61992-1, IEC 61992-2), operating at voltages in the distribution range, have been used as guides in the development of this document.

Also, the tests of HVDC circuit breakers conducted as part of TWENTIES project have been studied and some of the tests were adopted from the test reports thereby. The tests intended to verify the functionality and performance of HVDC circuit breaker in a type test program are discussed in deliverable 5.4 [31].

These tests are sub-divided into dielectric, operational, making and breaking tests as well as endurance tests as shown in Figure 13. However, in PROMOTioN project the focus is on the demonstration of DC short-circuit current interruption performance of HVDC circuit breakers and this is carried out using the test circuits designed in task 5.7 [32].

In international standardization, work proceeded during the project, with active participation from project partners. As a result of recent multi-terminal project proposals, wide spread research activities, CIGRE [33] and IEC inventories [34], IEC Technical Committee 17/17A, C has set up six working groups by early 2020 covering requirements and tests of all DC switchgear (>1.5 kV). IEC WG64, starting 2020 has the task to compile a technical specification (TS) of HVDC circuit breakers.

IEC Technical Committee 115 issued a standard on DC side equipment for LCC systems [35]. This document includes basic requirements for DC disconnectors and certain types of specialized DC switching devices (such as MRTS), but it excludes any type of DC circuit breaker designed to interrupt fault currents.

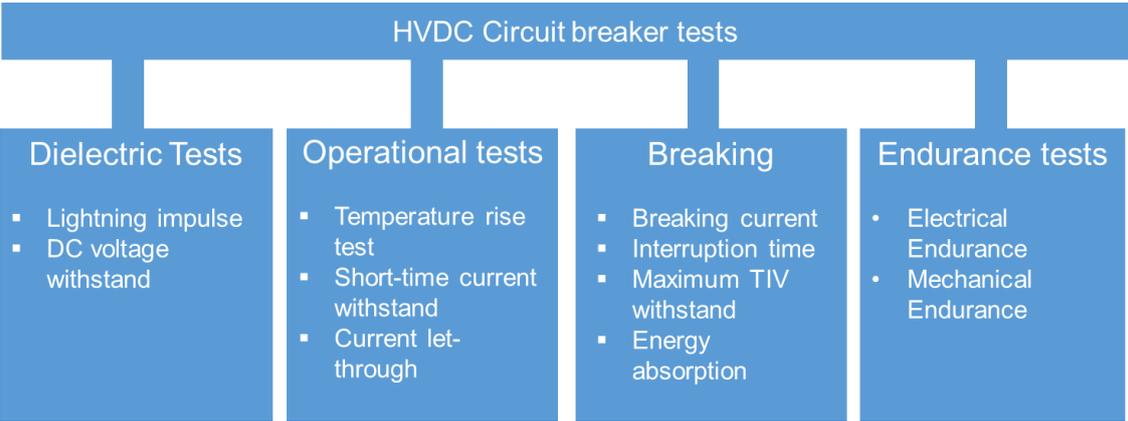


Figure 13 - HVDC circuit breaker test requirements

In deliverable 5.4 [31], as a base for the test requirements, service conditions for HVDC circuit breakers have been described. This is adopted from AC circuit breaker standards.

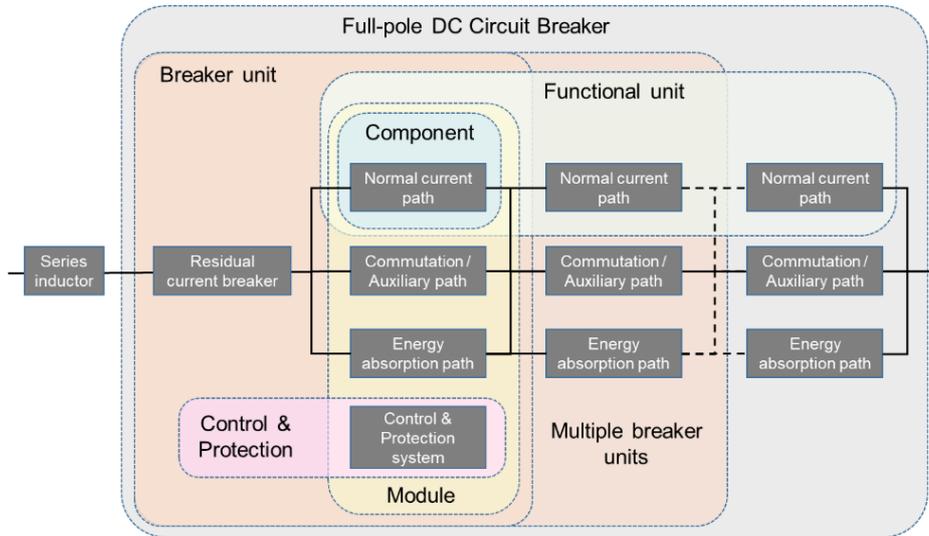


Figure 14 - Modular construction of HVDC circuit breakers - Terminology

Deliverable 5.4 [31] also discusses design and construction of HVDC circuit breakers and the impact on testing. The terms related with internal components of HVDC circuit breaker, have been discussed.

6.3 FAULT CURRENT INTERRUPTION REQUIREMENTS

In later stage of the project, after experiments with experimental DC circuit breaker exploring the stresses on subcomponents of HVDC circuit breakers, as reported in [36, 37] and discussed in chapter 7 more specific test requirements have been defined.

Before designing any test circuit, the critical stages of current interruption process and the actual stresses that need to be reproduced (for complete stress) must be identified. To this aim, six critical stages of DC fault interruption are defined. These are illustrated in Figure 15, in a schematic overview of fault current interruption characteristics:

1. Rise of fault current (proper di/dt) → breaker needs to act very fast;
2. Local current interruption in continuous current branch;
3. Internal commutation → initiation of counter voltage generation (du/dt);
4. Limitation and maintenance of TIV → fault current suppression;
5. Energy absorption;
6. System recovery voltage withstand.

In table 1, these stages are schematically outlined, and the critical parameters are identified.

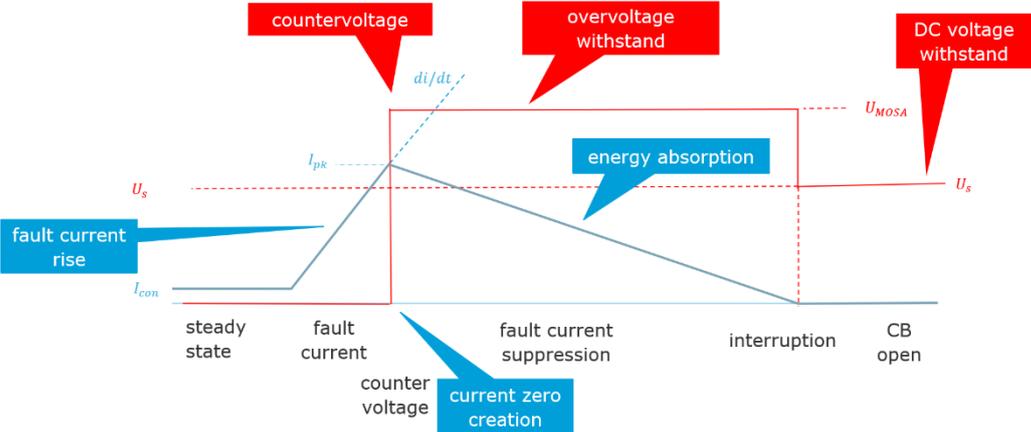


Figure 15: Critical stages of fault current interruption

Table 1: Stages of interruption and critical parameters

Stage of interruption		Breaker action	Components mainly stressed	Critical parameter
1	Rise of fault current	activates and trips very fast	mechanical actuators continuous current branch	t_{ic} di/dt
2	Local current interruption	blocks the continuous current branch	interrupting device (vacuum interrupter, load commutation switch)	I_{pk}
3	Internal commutation	generates counter voltage disconnecter insulates	active current injection circuit load current switch main breaker	U_{MOSA}
4	Limitation and maintenance of TIV	withstands short duration overvoltage (≈ 1.5 p.u.) fault current suppression	mechanical switching gap breaker in commutation branch	U_{MOSA} t_{FS}
5	Energy absorption	absorbs energy	MOSA	E
6	System voltage recovery	withstands long duration dielectric stress	mechanical switching gap (residual current switch)	U_s

The main motivation of including also the stages 4-6 in interruption tests is the following:

- Mechanical switches are key and novel components of all HVDC circuit breakers. In some applications they switch high current, in some they isolate high voltage, or both. Short-time dynamic (stage 4) overvoltage withstand and long duration static dielectric withstand (stage 6) shall be an essential part of a verification program.
- Surge arresters in HVDC circuit breakers are used in a different application than for overvoltage protection (the usual application). The unusual amount of energy to be absorbed requires a large number of parallel arrester columns and an equal current sharing between the non-linear ZnO elements.

In order to harmonize the stresses to which HVDC circuit breakers are exposed to during a fault current interruption tests, within the PROMOTioN project, agreement among participating manufacturers (Mitsubishi Electric, ABB, SciBreak) and the test-authority (KEMA Labs) was reached on a set of test-duties to which their breakers are exposed. Table 2 shows these test-requirements.

In many cases, especially for testing extra-high voltage (EHV) DC circuit breaker, it may not be possible to apply full-rated energy stress due to either a limitation of a test laboratory or for some practical reasons the test breaker is supplied with reduced energy capability. In such a case an alternative test duty which can replicate the magnitude and duration of TIV is defined. The test-duty TDT in Table 2 is introduced to fill this gap. This duty is intended to demonstrate the TIV withstand capability of the circuit breaker during the full duration of TIV that would occur under full rated energy (e.g. as specified in a specific project). Details are described in [38].

The test program of table 2 is taken as a guideline in the testing of three HVDC circuit breakers rated 80 kV 16 kA (VSC assisted resonant current type), 160 - 200 kV 16 kA (active current injection type) and 350 kV 20 kA (hybrid type).

Table 2: Agreed test-requirements of HVDC circuit breakers

Name	Current	Breaking test	#
TC10+	10% of rated continuous current	2 tests in positive current direction	2
TC10-	10% of rated continuous current	2 tests in negative current direction	2
TC100+	100% of rated continuous current	2 tests in positive current direction	2
TC100-	100% of rated continuous current	2 tests in negative current direction	2
TF100+	100% of peak fault current	2 test at specified energy absorption*, positive current direction	2
TF100-	100% of peak fault current	2 test at specified energy absorption*, negative current direction	2
TDT+	TBD	2 test at rated fault current suppression time**, positive current direction	2
TDT-	TBD	2 test at rated fault current suppression time**, negative current direction	2
*: Specified energy absorption based on specified value of energy absorption (MJ) of the test-object delivered			
**: Rated fault current suppression time based on U_s , U_{MOSA} , t_{IC} , I_{pk} , as would be present in service condition			
All tests are single opening operations			
In all tests, U_s (considering 10-15 % overvoltage) will be supplied during 300 ms after main current interruption			

6.4 CONTRIBUTION TO STANDARDIZATION

Lessons learnt regarding stresses to the HVDC circuit breaker as a black-box device and regarding stresses to its key components by actual laboratory testing are reported in deliverable D10.8 [38]. These experiences have been shared with international (pre)standardization committees who are drafting standards for HVDC circuit breakers.

As a result of recent multi-terminal project proposals, wide spread research activities, CIGRE [33] and IEC inventories [39], IEC Technical Committee 17/17A, C has set up six working groups by early 2020 covering requirements and tests of all DC switchgear (>1.5 kV). IEC WG64, starting 2020 has the task to compile a technical specification (TS) of HVDC circuit breakers. This document is based on a (draft) Chinese standard on common specifications of DC circuit breakers [40], to be followed by separate national standards for 'mechanical' (active current injection) and hybrid types.

Active input from WP10 herein is provided through membership and participation in international meetings. These activities have been in close connection with PROMOTioN WP11 ("Harmonization towards standardization"), that issued a "harmonization catalogue" [41] and organized various harmonization workshops with WP10 presentations.

In CIGRE, Joint Working Group (WG) B4/A3.80 is presently studying HVDC circuit breakers and its test requirements, whereas WG A3.40 is focusing on MVDC circuit breakers and systems. CIGRE WG A3.39 is addressing the application of metal-oxide surge arresters (MOSA) in HVDC circuit breakers, among others.

All three working groups have active participation/membership and input from WP10.

7 COMPONENT STRESSES

7.1 INTRODUCTION

All designs of HVDC circuit breakers have components applied in a non-conventional way, or they include new types of components. In order to reduce the risk of failures of these subcomponents in the application of HVDC circuit breakers, standardization committees need to analyse the new stresses, typical for HVDC circuit breakers, that these components face.

To define and refine justified test requirements, a thorough understanding of the interactions between the internal components of the HVDC circuit breaker and the stresses on these components under real DC fault current interruption condition is necessary. To this aim, an experimental active current injection DC circuit breaker is set up in KEMA's high-power laboratory to investigate the stresses of the main components; namely, the vacuum interrupter (VI) and the metal oxide surge arrester (MOSA).

The performances of three different designs VIs are investigated and it is found out that each of the VIs behave completely different regarding the interruption of high-frequency injection current. The key parameters having impact on current interruption performance of the VIs are identified and analysed.

The performance of a MOSA, designed for HVDC circuit breaker application, is also investigated by applying energy per volume ranging between 70 - 220 J/cm³ at temperatures as high as 250 degC. In order to find out the performance limit of the MOSA for this application, successive high-energy tests are performed until electro-mechanical failures occur in the MO varistors. Various failure modes such as fracturing and puncture are observed. Results are published in [42] and reported in deliverable D10.2, 10.3 [43,44].

7.2 MECHANICAL SWITCHING DEVICES IN HVDC CIRCUIT BREAKERS

Every practical HVDC circuit breaker is equipped with a mechanical switching device. Its function is to enable low losses in continuous operation and to alleviate (when in open state) dielectric stresses on the power electronic components. In HVDC circuit breakers, every mechanical switching device has to achieve contact separation very fast, which is achieved by electromagnetic repulsion drives. Such drives are electronically controlled, which implies a certain susceptibility to EM interference from transients of the primary sources (arcing, re-ignition, fast switching, high di/dt -current, high du/dt etc.).

In most designs a (considerable) number of mechanical switching devices is put in series. This implies that power to the individual drives cannot be supplied through galvanic connections. Usually, transformers that have sufficient insulation capability are used. For example, several isolation transformers are stacked in series to achieve sufficient insulation from earth for 500 kV HVDC circuit breakers. High-speed drives and their isolated power supply are not used in such a way before in power equipment and service experience is very limited or non-existent. Due attention needs to be paid to the verification of the mechanical endurance of the total kinematic chain.

In addition, the proper functioning of a stack of a larger number of smaller interrupters needs a well synchronized contact separation as well as a built-in redundancy to overcome the functional loss of one or more individual interrupters.

Vacuum is a very good “medium” regarding interruption of HF current and very fast recovery of the gap against steep rising recovery voltage. Nevertheless, the application of vacuum interruption in active current injection type of HVDC circuit breakers may approach performance limits.

Mechanical gaps (vacuum/SF₆) breakdown electrically when they are not able to withstand voltage. Most critical is the fault current suppression phase, where the overvoltage is around 1.5 p.u. whereas at the same time the gaps are recovering from interruption and/or switching. After fault current suppression, there is a much longer exposure to the recovering system voltage and its (slow) transients, until the residual current switch takes over that voltage stress.

In HVDC circuit breakers, high-speed disconnectors need to open with very low current and with very low voltage in order to avoid arcing. Once current (at contact separation) exceeds a certain threshold, the arc will persist during a time, depending on the voltage across the commutation branch.

Therefore, the design of (ultra-)fast disconnectors is very critical. Opening of the disconnector needs to be synchronized carefully, after current transients in the continuous current branch decay sufficiently.

Once the main breaker has interrupted the fault current, soon the full TIV appears across the switching gap which must have been sufficiently open to isolate. Breakdown of this gap would lead to dielectric overload of the load commutation switch and a free burning arc in the SF₆ disconnector. Therefore, dielectric coordination of this disconnector allows only a very small variation in its opening time over service life. Requirements for mechanical stability are more severe than for controlled (capacitor bank) SF₆ circuit breakers for HVAC applications [45].

In the active current injection schemes using capacitor discharge as the counter current source, an ultra-fast switching device must be used to start the discharge. This may be a mechanical switch (vacuum making switch, triggered spark gap) or a semiconductor stack (IGCTs, thyristors). In both applications, the very large di/dt and peak current need to be evaluated as a non-standard stress. In the case of vacuum making switch, provisions must be made to avoid contact welding. For EHV applications several of these switches need to be connected in series. Synchronous operation of these making switches is essential to avoid premature current injection as a result of pre-strike. In case of semiconductor making switches, di/dt and short-time thermal and dynamic stresses can be extreme and far from standard. In addition, during normal operation the making devices in open position are subjected to continuous DC voltage stress.

7.3 EXPERIMENTAL OBSERVATIONS ON VACUUM INTERRUPTERS

An experimental set up was created, using up to three 36/38 kV commercially available vacuum interrupters in series, showing the details of local current zero in vacuum interrupters. A typical representative oscillogram and impression of the experiments is shown in Figure 16

The main observations are as follows:

- Commercially available medium voltage vacuum interrupters differ greatly in the way they deal with interruption of high-frequency (HF) current;
- It cannot be expected that vacuum interrupters can interrupt the HF current at the first current zero crossing, especially when the main current is small. In most cases, a later current zero crossing comes with interruption;
- Breakdown (restrike) of a vacuum gap can occur relatively long after interruption (during the fault current suppression phase) but in most cases leads to recovery of insulation. This leads to the conclusion that during testing, it is essential to maintain the TIV for a time that corresponds to the service condition (this is the motivation for the TDT test-duty).

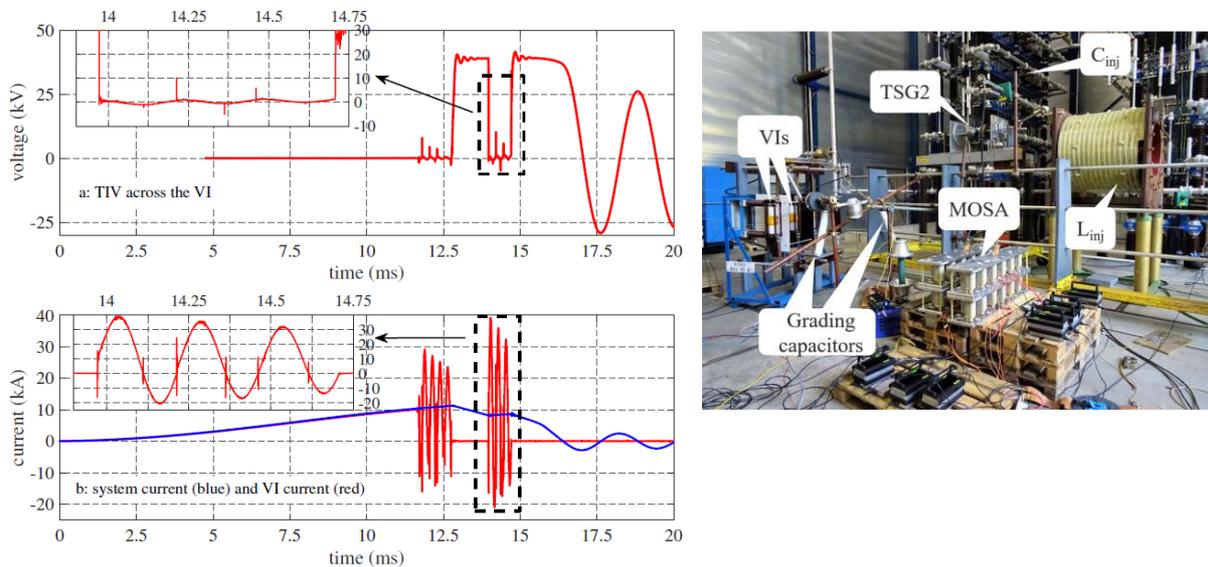


Figure 16: Local current zero creation in experimental DC circuit breaker.

Left: Oscillogram of injection current (red) showing several zero crossings before interruption and TIV rise at 14.7 ms. After TIV creation, the gap cannot withstand the voltage and breaks down at 13.5 ms but spontaneously recovers insulation 1 ms later.

Right: Laboratory set-up including vacuum circuit breaker (VIs), making switch to initiate injection (TSG2) and injection circuit capacitors (C_{inj}) and reactor (L_{inj}).

7.4 ENERGY ABSORBING SYSTEMS IN HVDC CIRCUIT BREAKERS

A large volume of MOSA is needed for absorbing the energy from the faulted system and maintaining the counter voltage. Many columns are needed in parallel to cope with large energy absorption. This means the individual zinc-oxide (ZnO) varistor discs composing each column need to be carefully selected to have an equal current flowing through the column. Given the high non-linearity of the U-I characteristic, a small mismatch in conduction voltage would lead to a large current difference. This, in turn, would heat the columns unequally and change its characteristic unfavourably [46, 47]. Therefore, careful matching of the columns is essential. A state-of-the-art selection and matching procedure is described in [43].

The total mass of ZnO material in HVDC circuit breakers can be over one thousand kilograms, which implies that cooling down (after interruption of a significant fault current) is very time consuming. In testing, it is recommended to have cooling times in the order of several hours after rated fault current interruption. The consequence of this is that when a reclosure and re-open function is required, the design should be able to absorb at least double the energy that is associated with a single interruption (and proportionally more counter voltage creation etc. when more than two reclosures are expected). Moreover, the other functions of the breaker (local current zero creation, should be accommodated for quickly repeated operation).

Multi-reclosure of HVDC breakers is required in overhead line (OHL) systems. OHL arcing faults most often disappear after a reclosure and a subsequent opening (O-CO sequence) of the breaker. HVDC circuit breakers for the Zhangbei (OHL) project in China have been specified to deal with total energy absorption exceeding 150 MJ [48]. When the actual short-circuit, carrying the large fault current is removed, in many cases a low-current secondary arc to earth persists, which is fed through the stray impedances of the transmission system. Reclosure should then be delayed until the secondary arc ceases, mostly by natural reasons, like wind or by thermal elongation. Further study needs to reveal the persistence of secondary arcs in HVDC OHL systems. In cable systems, reclosure does not seem to be a suitable action, since faults in cable systems are normally destructive and need repair.

7.5 EXPERIMENTAL OBSERVATIONS ON MOSA ABSORBERS

In this part of the experimental study, attention was paid to the thermal stress experienced by the energy absorption system. In HVDC circuit breakers, a large number of ZnO discs are used in series and parallel to absorb the energy from the system. A critical design parameter is the sharing of the current during the current suppression phase by a multitude of parallel columns.

This was investigated in a specially state-of-the-art designed MOSA bank [46], consisting of 12 columns of 4 ZnO discs each, see Figure 17.



Figure 17: Left: Experimental 2 MJ MOSA bank, with 8 columns equipped with thermal high-speed monitoring and separate current measurement. Right: Static IR recording of thermal status of this equipment after current loading.

Due to the highly non-linear nature of the ZnO material, a small mismatch in individual characteristics of the separate columns can lead to an increase of current in one of them, causing potential thermal overload.

This effect is illustrated by the test-results in Figure 18.

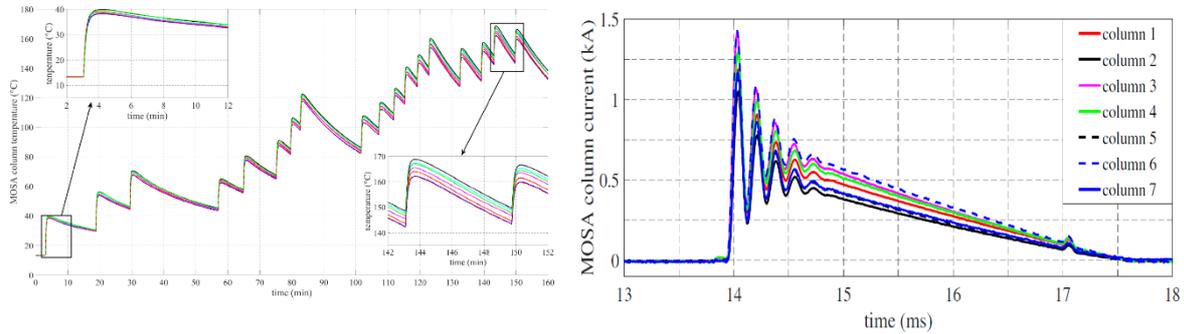


Figure 18: Measured differences in stresses in parallel columns of a 2 MJ surge absorber. Left: Difference in temperature between 8 eight columns after a large number of successive fault current interruptions. Right: Difference in current through 8 individual columns during a single fault current interruption

For the sake of understanding failure modes of MOSA, high-energy tests are executed on a 6 MJ bank (three stages in series of the structure shown in Figure 17) to cause the bank to fail on purpose. An impression of this exercise can be obtained from Figure 19.

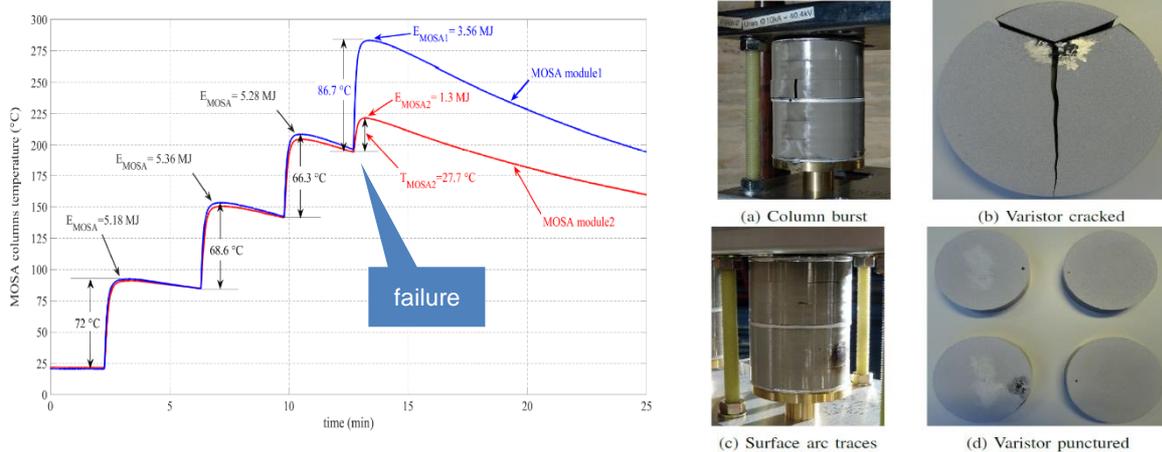


Figure 19: High-energy input to MOSA bank. Left: Temperature track of four consecutive fault current interruptions, each inserting around 5.2 MJ of energy in the absorber during 13 minutes. Right: Various failure modes as a result of excessive energy input

The main observations are as follows:

- Design of multi-paralleled columnar MOSA absorbers is critical because the electrical stresses need to be distributed evenly across the columns. Since MOSA normally is applied for overvoltage protection, the application in HVDC circuit breakers as energy absorption is a non-standard one;
- a properly designed MOSA module performs well when the temperature is below 200 degC and the energy injection per volume is limited to less than 200 J/cm³. Energy absorption at temperatures more than 200 degC may result in damage of MO varistor(s);
- Upon fault current interruption, temperature rises very fast but cooling down is much slower than a possible second opening, as in case of re-opening. Therefore, HVDC breakers that are specified in overhead lines, need an amount of ZnO material proportional to the number of required re-opening operations.

8 HVDC CIRCUIT BREAKER TEST CIRCUIT REQUIREMENTS

8.1 GENERIC TEST-CIRCUIT REQUIREMENTS

Based on the stresses which are exerted onto HVDC circuit breakers during DC fault current breaking operations, requirements for test circuits in which DC short-circuit current breaking capability is to be verified, have been developed in deliverable 5.6 [49].

A test circuit for HVDC CB short-circuit current breaking testing should reproduce the stresses that are relevant for current breaking operations up to the rated values including a test factor where applicable. Furthermore, the test circuit must be able to withstand any stresses such as TIV which are produced and determined by the HVDC CB itself. For a test circuit to provide adequate stresses to HVDC CBs, it should fulfil the following requirements based on the characteristic of the different periods during current interruption discussed in chapter 6 and illustrated in Figure 15 :

1. Pre-condition the HVDC CB to mimic worst case normal service conditions, and ensure internal systems are powered up and charged.
2. Produce a test current which rises somewhat linearly from anywhere up to the rated load (or short-time withstand current) to the intended test duty within the breaker operation time. It is shown in [1] that the most difficult interruption may not necessarily be the highest current. Thus, test circuits have to provide a wide range of currents, from the rated load current (or less) to the rated short circuit breaker current of an HVDC CB. The test circuit must be able to apply the test current bidirectionally.
3. Supply TIV of adequate duration and magnitude immediately after the mechanical switching operation.
4. Supply an adequate amount of energy (to be agreed upon between manufacturer and project developer; in case of the largest HVDC breaker, test-labs cannot provide the project-required energy)
5. Supply rated dielectric stress immediately after current suppression
6. Avoid damage to the HVDC CB and test circuit in case of failure - if the prospective short-circuit current from a test circuit can exceed the HVDC CB's rated short-circuit breaking current, it is necessary to limit the damage to the HVDC CB as well as the test installation in case of a failure to clear. Methods to avoid potential damage to the test breaker as well as the test installation have been proposed
7. Be implementable / economical – the test circuit must be technically feasible, practical and economical

The above requirements should be fulfilled whilst respecting practical breaker operation times which are currently assumed to be in the range of 2 – 8 ms.

These stresses do not have to be supplied by the same source, in which case it is referred to as a synthetic test. The modular construction of HVDC CBs may under certain conditions allow the verification of functionality

and/or ratings by testing a reduced number of modules, which is referred to as modular testing. Furthermore, in some cases, different functionalities of an HVDC CB can be tested in separate tests with different test circuits, in which it is referred to as multi-part testing.

8.2 TEST CIRCUIT SELECTION

Four hypothetical (ideal) test circuits based on a controlled rectifier, a charged capacitor, a charged reactor, and an AC short-circuit generator operated at reduced frequency, have been qualitatively discussed and compared to the test circuit requirements, as shown in Table 2.

It is concluded that only a controlled rectifier circuit could

directly synthesize all necessary stresses but is likely to be prohibitively expensive and complex at the required power ratings and functionality.

The pre-charged capacitor circuit is able to provide sufficient di/dt and sufficient supply voltage in order to verify the current zero creation, commutation and the counter voltage (TIV) generation. Apart from capacitor circuits which include excessively large capacitors, the duration of supply voltage falls short to provide adequate duration of TIV and thus energy. This also applies for the pre-charged reactor circuit.

AC short-circuit generators running at a reduced frequency offer the possibility to deliver high energy stresses, which may be unpractical to achieve using a charged capacitor circuit. The latter is especially relevant for testing HVDC circuit breakers with longer breaker operation times.

A comparison is outlined in Figure 20. In this

case, an 80 kV breaker module is considered that interrupts a peak fault current of 9 kA in four different circuits. In the capacitor circuit a capacitor of 506 μF (charged to 80 kV) is considered. In all cases the reactor's

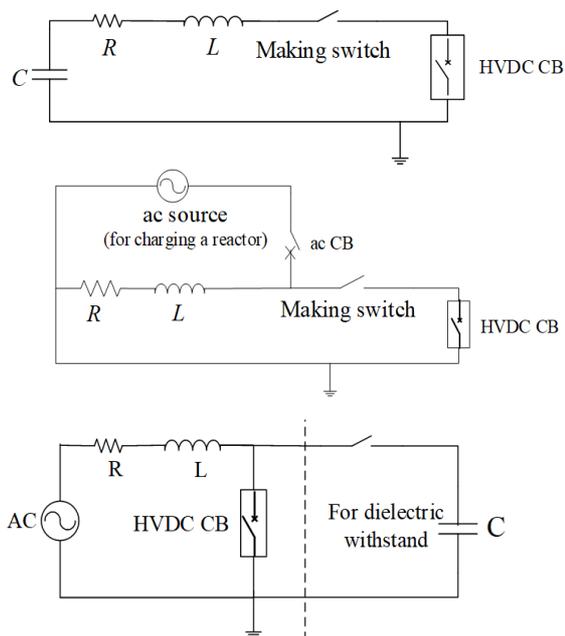


Figure 21: Circuits studied for feasibility for HVDC circuit breaker testing. Upper: Energy supplied from a pre-charged capacitor bank; middle: Energy supplied by a pre-charged reactor bank; lower: Energy supplied by an AC generator

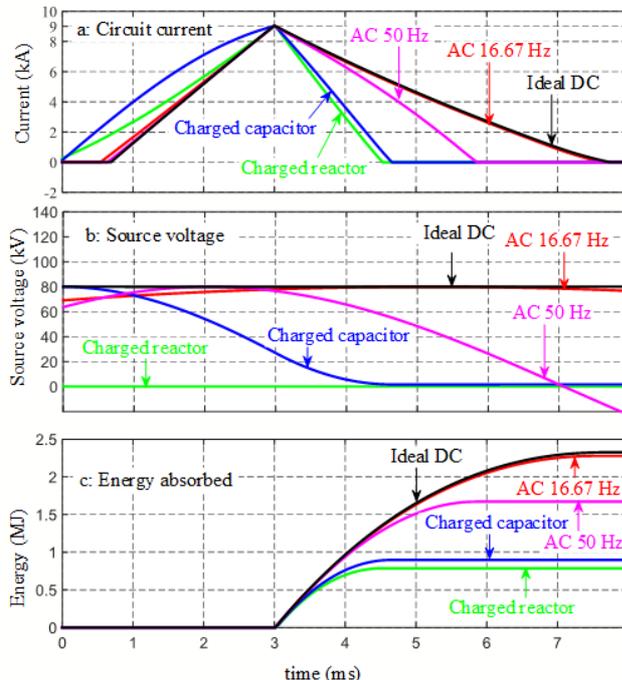


Figure 20: Comparison of current suppression and energy supply of four idealized test-circuits.

Table 3 - Summary of test circuits and their possibilities/limitations

Test circuit requirement	Rectifier	Charged capacitor	Charged reactor	AC short circuit generator
Pre-condition HVDC CB	Current profiles and stresses can be accurately controlled to follow a target waveform.	Separate circuit required	Separate circuit and/or source required	Separate circuit or source required
Produce test current	Current profiles and stresses can be accurately controlled to follow a target waveform.	Very high di/dt can be achieved	Difficult to control di/dt. Quasi DC current can be obtained in case very fast switching cannot be achieved. Hence the method may not be suitable for testing HVDC CBs with power electronics in the normal current path.	The existence of minimum inductance in the circuit due to generator and transformer reactance put maximum limit on di/dt
Supply rated energy to the HVDC CB and withstand TIV	Current, voltage and energy profiles and stresses can be accurately controlled to follow a target waveform. However, large required power supply may be prohibitively expensive to realize	Requires large capacitance, with associated volume and cost.	Requires large reactance with very high quality factor, with associated impact on charging circuit, volume and cost.	Very high voltage (full-pole voltage) may exceed the insulation coordination of test installation or multi-part, multi-unit tests to be applied.
Supply rated dielectric stress	Voltage stresses can be accurately controlled to follow a target waveform	Some DC charge remaining after suppression. Very large capacitance required to make this sufficient for testing	Must be realised by separate source/circuit.	After suppression, AC voltage stress is applied by the generator. Controlled DC stress must be realised by separate source/circuit
Avoid damage to the HVDC CB and test circuit	Must be realised by additional circuit provisions	Must be realised by additional circuit provisions	The peak current is the same as rated interruption current	Must be realised by additional circuit provisions
Be implementable / economical	High investment cost and complex control	Can utilise existing test facilities in some cases	Accurate switching of charging circuit is required; High quality factor reactor is required; Challenging to achieve high currents	Utilises existing test facilities, with minimal additional investment cost required. Within a reasonable range, can provide full testing to prototype-level HVDC CB
Test extra functionality such as reclosing, soft-closing, etc.	Current, voltage and energy profiles and stresses can be accurately controlled to follow a target waveform	Separate circuit and/or source required	Separate circuit and/or source required	Separate circuit and/or source required
Application	Low to medium voltage testing	Interruption-only tests very low energy	Low-medium current and energy	Full current, high energy testing.

inductance is 20 mH. This implies that the capacitor circuit has a stored energy of 1.6 MJ and the reactor circuit stores 0.81 MJ. Generators, in their rotational energy, have much more stored energy. As can be seen in Figure 20, an AC generator running at 16 $\frac{2}{3}$ Hz gives almost identical stresses (regarding di/dt , voltage, current and energy) as the ideal DC source. AC short-circuit generators offer flexible control of the rate-of-rise of test current and the amount of energy delivered to the HVDC circuit breaker by carefully choosing the generator frequency, the test circuit impedance, the generator source voltage magnitude, and the making angle.

A method to protect the test object and the test circuit from damage in case the HVDC circuit breaker fails to operate correctly, has been presented, see chapter 8.4. A high-speed level-controlled triggered spark-gap, combined with an auxiliary breaker can by-pass the prospective test current and isolate the test object from the test source.

8.3 MODULAR TESTING OF HVDC CIRCUIT BREAKERS

Depending on the installed power of short-circuit generators, there is limit to which HVDC breakers can be tested as a single device. The AC characteristic implies that an inherent limitation exists on testing HVDC circuit breakers with long breaker operation times, as the entire fault neutralisation time must be less than the longest possible half period of the applied test current. For KEMA labs, which have 6 generators at 2500 MVA each available, the limits are outlined in Figure 22 [50].

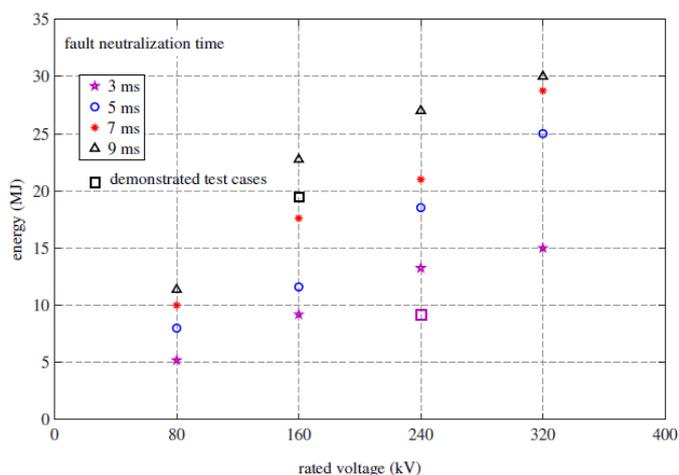


Figure 22: Maximum energy supply versus voltage ratings considering different technologies of HVDC CBs at KEMA laboratories. This is considering 16 kA peak fault current.

Finally, it is recognized that no practical test circuit can supply the required stresses to directly test

500 kV class full-pole HVDC circuit breakers. Some suggestions for verifying performance of a modular part of a breaker i.e. unit testing, or separately verifying different functionalities i.e. multi-part testing and realising different stresses from different test sources i.e. synthetic testing are discussed in deliverable 5.6 [49].

As shown in Figure 14, the modular test specifications, derived from full-pole HVDC circuit breaker ratings can be done in the following way:

Current sharing

- In series connected modules current is shared by every module

Voltage grading

- Divided by number of series connected modules
- Determined by surge arrestors
- Full-pole components need to be dielectrically tested separately

Energy grading

- Divided by number of series connected modules
- Margin required determined by small differences in timing

In Figure 23, a simulated example is shown of the characteristics of an 80 kV module of a 320 kV HVDC circuit breaker, compared to the latter's behaviour in a system.

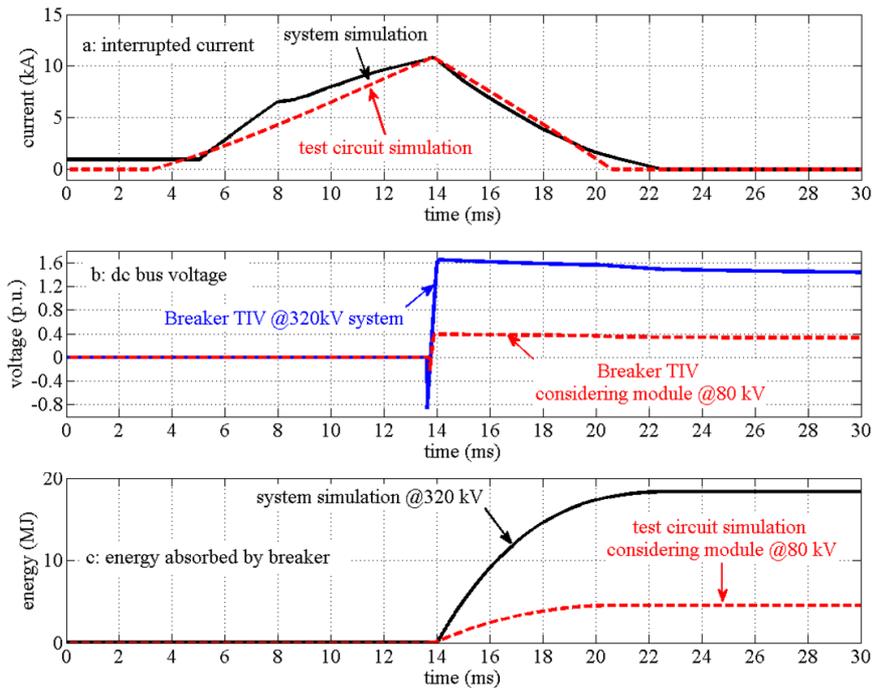


Figure 23 – Test wavetraces of a 80 kV module in a 320 kV HVDC circuit breaker

8.4 REALISATION OF TEST CIRCUIT

In deliverable 5.7 [51], the realisation of the reduced frequency AC short-circuit generators based test circuit at KEMA Laboratories, shown in Figure 24, is described. A method for tuning the test circuit's variables to achieve the required current and energy test stresses is defined.

The implementation of overvoltage and overcurrent protection methods was explained, as well as methods to realize dielectric stress after current suppression. The resulting final test circuit, with a focus to the generators and step-up transformers is shown in Figure 24. Generators, transformers and reactors can be adjusted to realise the proper combination for reaching a certain stress package as demonstrated in Figure 22.

A test program aimed at validating the test circuit's ability to meet the requirements is executed. Test results of prospective current tests, overcurrent and overvoltage protection tests, and of dielectric stress application tests were provided. Simulation results of HVDC circuit breaker models were superimposed onto the experimental results to illustrate the ability of the test circuit to synthesize realistic stresses, as shown in Figure 25.

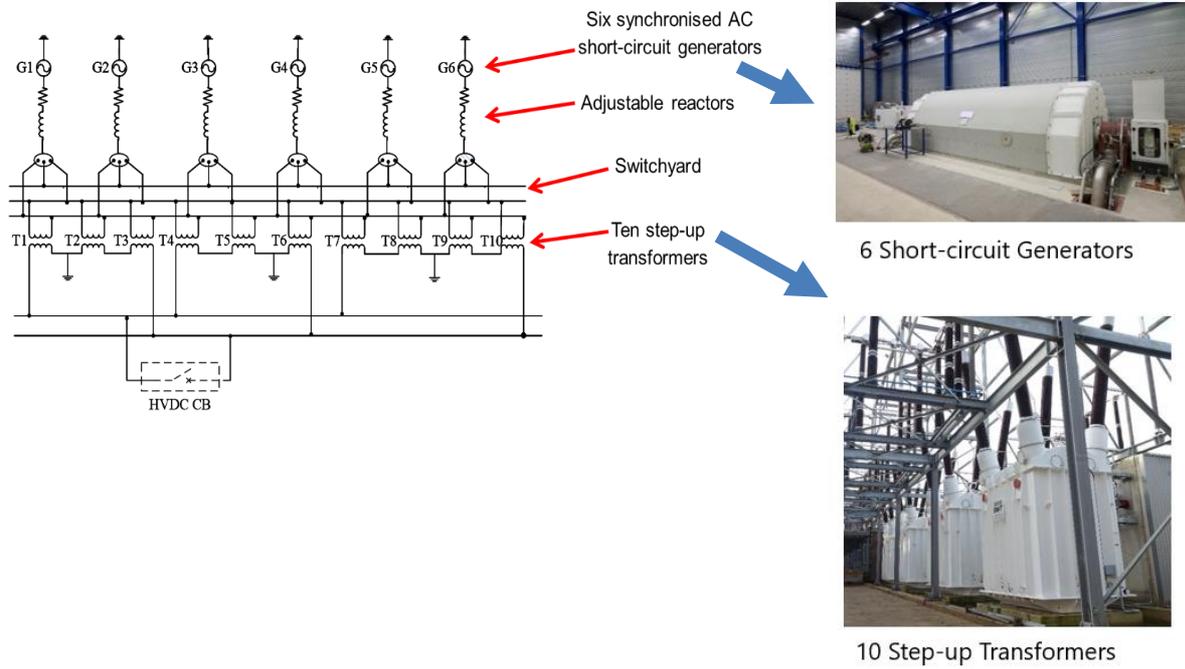


Figure 24 – KEMA Laboratories High Power Lab schematic HVDC circuit breaker test circuit outline

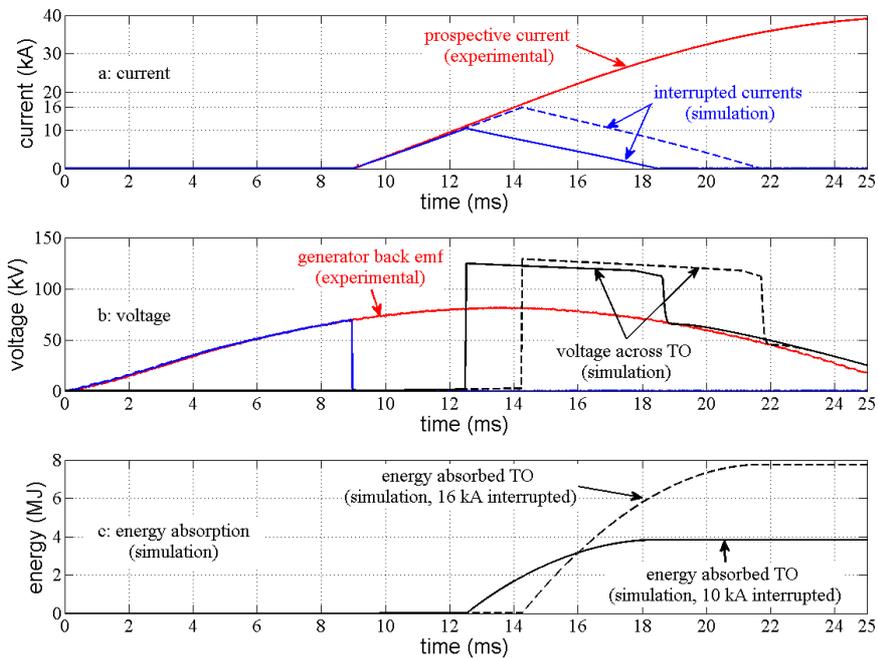


Figure 25 – Simulation results of fault current interruption superimposed on an experimental prospective current test result

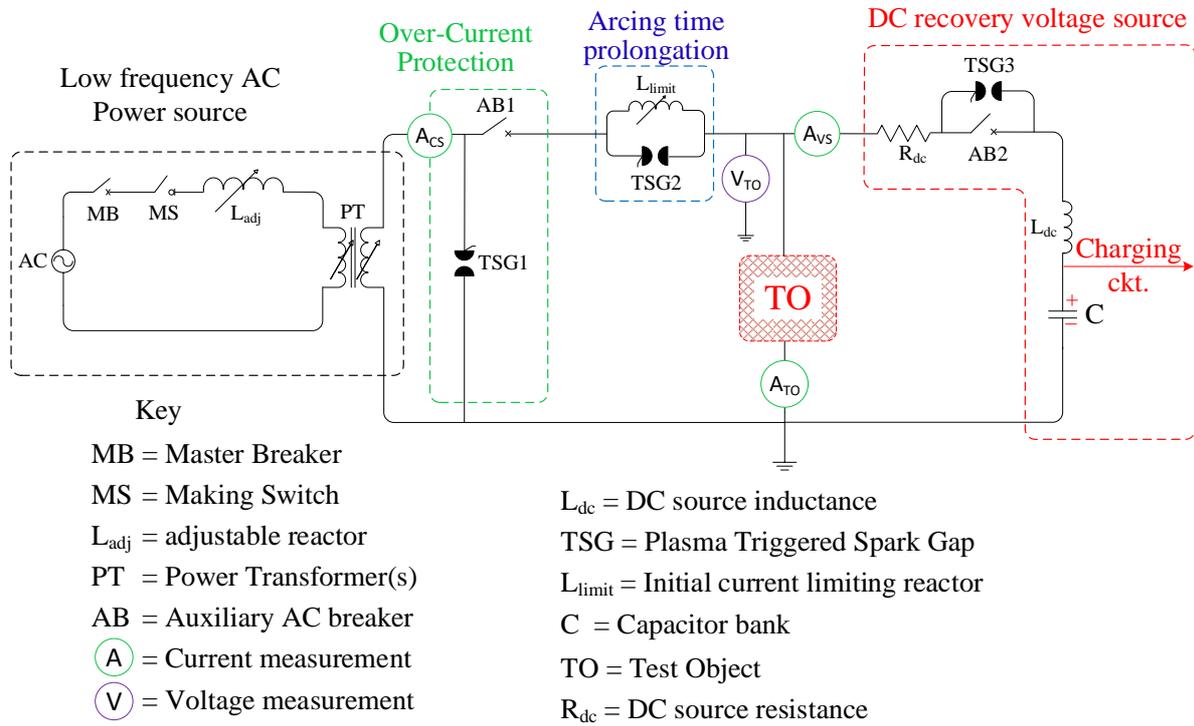


Figure 26: Complete Test Circuit for HVDC Circuit Breaker

8.5 VALIDATION OF TEST CIRCUIT

In order to actually demonstrate the capability of the test-circuits, its controls, protections, auxiliary circuitry etc., an 80 kV module of an active current injection HVDC circuit breaker, provided by Mitsubishi Electric, was installed at KEMA Labs. A photo of the test-laboratory with the breaker inside is shown in Figure 27. Validn of the test-circuit is described in deliverable 5.7 and 10.1 [52].

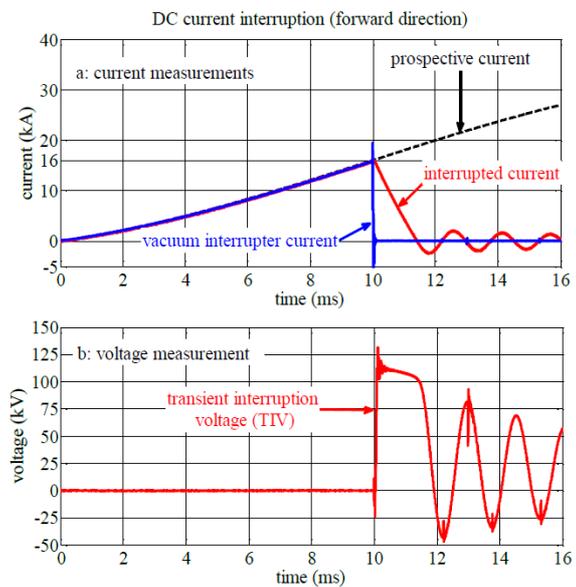
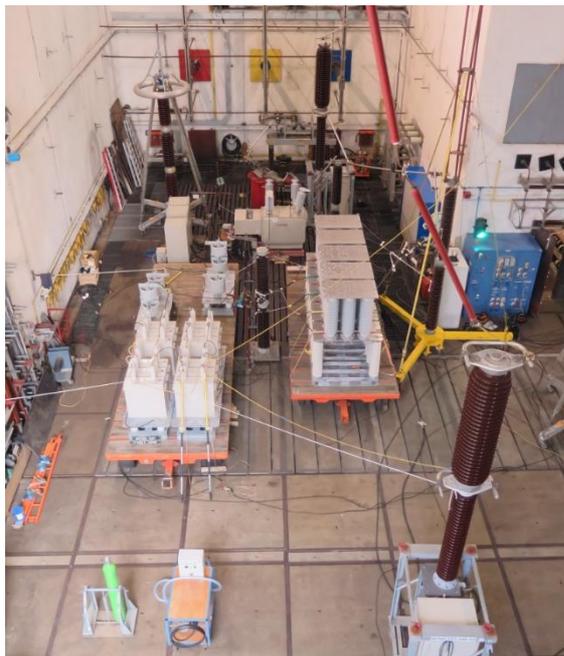


Figure 27: Test-circuit demonstration with an 80 kV 16 kA active current injection HVDC circuit breaker module. Left: set-up in the laboratory, right: oscillograms of currents (upper) and voltage (lower)

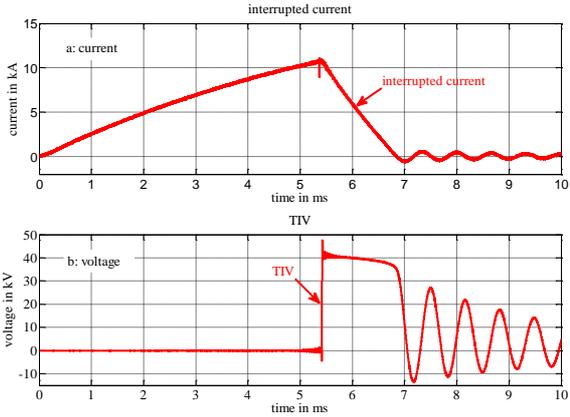


Figure 28: Testing of single module (27 kV, 10 kA) VSC assisted resonant DC Circuit breaker. Left: Test setup in the laboratory, right: oscillograms of currents (upper) and voltage (lower)

9 DEMONSTRATION OF HVDC CIRCUIT BREAKERS

9.1 VSC ASSISTED RESONANT CURRENT INJECTION DC BREAKER DEMONSTRATION

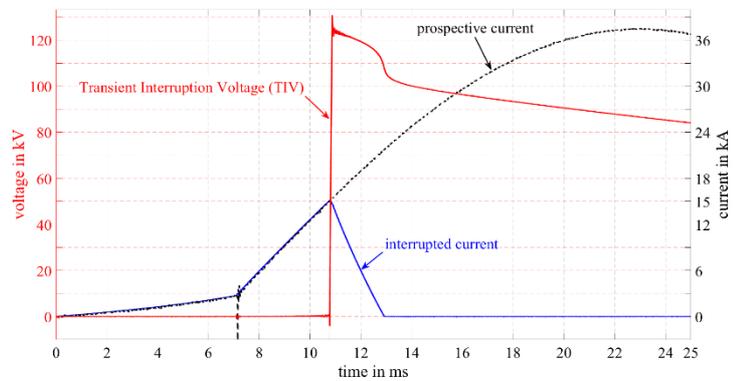


Figure 29: Demonstration of HVDC circuit breaker performance in the KEMA Labs' high-power laboratory. Laboratory set-up and oscillogram of a TF100+ (15 kA) test of a 80 kV VSC assisted resonant current (VARC) HVDC circuit breaker consisting of three . Red: Voltage across the circuit breaker; blue: current through the circuit breaker; grey: prospective low-frequency AC current.

9.2 ACTIVE CURRENT INJECTION HVDC CIRCUIT BREAKER DEMONSTRATION

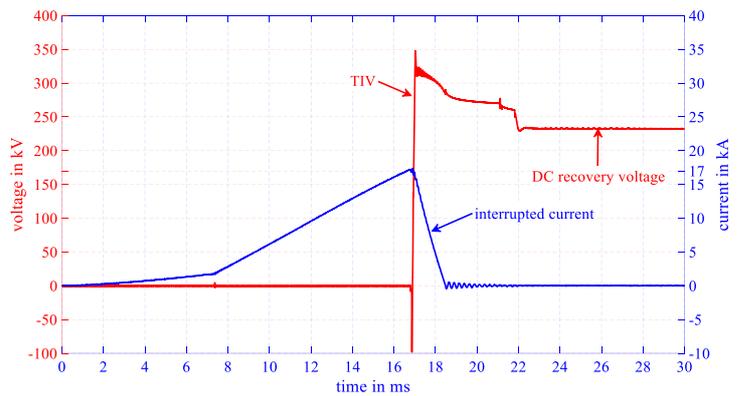


Figure 30: Demonstration of HVDC circuit breaker performance in the KEMA Labs' high-power laboratory. Laboratory set-up and oscillogram of a TF100+ (16 kA) test of a 200 kV active current injection HVDC circuit breaker; Red: Voltage across the circuit breaker; blue: current through the circuit breaker.

9.3 HYBRID HVDC BREAKER DEMONSTRATION

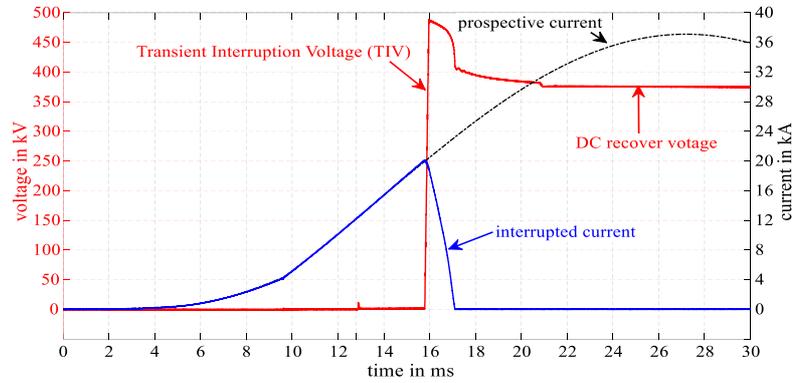


Figure 31: Demonstration of HVDC circuit breaker performance in the KEMA Labs' high-power laboratory. Laboratory set-up and oscillogram of a TF100+ (20 kA) test of a 320 kV hybrid HVDC circuit breaker;
 Red: Voltage across the circuit breaker; blue: current through the circuit breaker; grey: prospective low-frequency AC current.

9.4 SUMMARY OVERVIEW

In the table below, an overview is presented of the test-campaigns, dedicated to the technology verification of HVDC circuit breakers in various stages of development from proto-type to product.

Manuf.	Type	Rated voltage (kV)	Modules	Interrupted current (kA)	Energy (MJ)	Internal commutation time (ms)	Status
A	Active current injection	80	1	16	4	8	Tested
A	Active current injection	160	2	16	5	7	Tested
A	Active current injection	200	2	16	4	8	Tested
B	Hybrid	350	1	20	10.5	3	Tested
C	VSC assisted current inj.	27	1	10	0.6	3	Tested
C	VSC assisted current inj.	80	3	16	3	1.5 - 2	Tested

The test results of the three different technologies of HVDC CBs demonstrated within the PROMOTioN project framework. For each breaker technology, tests have been performed according to the commonly agreed test program. However, the actual test parameters and the breaker performance parameters are defined by the OEM of the specific technology.

First, the active current injection HVDC CB is demonstrated. This breaker has been tested for its bidirectional current interruption capability. The following tests have been performed:

- TF100 → 16 kA current interruption → bidirectional
- TC100 → 2000 A current interruption → bidirectional
- TC10 → 200 A current interruption → bidirectional
- TDT → 8.5 kA current interruption with TIV duration of 4.2 ms → bidirectional

The breaker operation time is 7 ms and the breaker system voltage is 160 kV. The maximum energy absorbed is 4.7 MJ. A test of 200 kV system voltage has also been performed successfully in which the breaker cleared 17 kA current in the forward direction within breaker operation time of 8 ms.

Second, the hybrid HVDC CB has been demonstrated. This is a unidirectional breaker rated for 350 kV system voltage. The following tests have been performed on the hybrid HVDC CB:

- TF100 → 20 kA current interruption → unidirectional
- TC100 → 3300 A current interruption → unidirectional
- TC10 → 330 A current interruption → unidirectional
- TDT → 4.6 kA current interruption in which TIV is maintained for 9.5 ms → unidirectional

The breaker operation time for the hybrid HVDC CB is 3 ms. The maximum of 10.5 MJ energy absorption has been demonstrated.

Finally, the VARC HVDC CB has been demonstrated. This breaker is rated for 80 kV system voltage and the following tests have been performed:

- TF100 → 12 kA current interruption → bidirectional
- TF100 → 15 kA current interruption → Once in each direction
- TC100 → 2000 A current interruption → bidirectional
- TC10 → 200 A current interruption → bidirectional
- TDT → 8.2 kA current interruption in which TIV is maintained for 5.6 ms → bidirectional

Two breaker operation times have been demonstrated for VARC HVDC CB. First, all the agreed test program has been fulfilled at the breaker operation time of 2 ms. Then, TF100 (12 kA) current interruption has been performed at breaker operation time of 1.5 ms. This was successfully demonstrated by performing current interruption twice in each direction.

10 EXTERNAL OUTPUT AND DISSEMINATION

10.1 HIGH-POWER LABORATORY DEMONSTRATIONS

- Mitsubishi Electric Europe active current injection circuit breaker 80 kV, 16 kA, September 28, 2017 (test circuit demonstration to selected TSO staff)
- Mitsubishi Electric Europe active current injection circuit breaker 160 – 200 kV, 16 kA, June 20, 2019 (see Figure 33), 30 participants + workshop
- ABB hybrid circuit breaker 320 kV, 20 kA, Feb. 27, 2020 (see Figure 32), 37 participants + workshop
- SciBreak VSC assisted resonant current injection circuit breaker, 80 kV, 15 kA, Aug. 19, 2020 (on-line)

10.2 PEER REVIEWED JOURNAL ARTICLES

- N.A. Belda, R.P.P. Smeets, “Test Circuits for HVDC Circuit Breakers”, IEEE Trans. Pow. Del., Vol. 32, pp. 285-293, 2017
- N.A. Belda, C.A. Plet, R.P.P. Smeets, "Analysis of Faults in Multiterminal HVDC Grid for Definition of Test Requirements of HVDC Circuit Breakers", IEEE Trans. on Pow. Del., vol. 33, no. 1, pp. 403 - 411, 2018
- N.A. Belda, C.A. Plet, R.P.P. Smeets, “Full-Power Test of HVDC Circuit-Breakers with AC Short-Circuit Generators Operated at Low Power Frequency”, IEEE Trans. Pow. Del., Vol. 54. Issue 5, pp.1843 – 1852, 2019
- N.A. Belda, R.P.P. Smeets, R.M. Nijman, “Experimental Investigation of Electrical Stresses on the Main Components of HVDC Circuit Breakers”, IEEE Trans. Pow. Del., early access , DOI 10.1109/TPWRD.2020.2979934, 2020
- R.P.P. Smeets, N.A. Belda, “HVDC Fault Current Interruption: A technology review”, High Voltage (in review)
- S. Liu, M. Popov, S. S. Mirhosseini, S. Nee, T. Modeer, L. Ängquist, N. A. Belda, K. Koreman, M. A. M. M. van der Meijden, “Modeling, Experimental Validation, and Application of VARC HVDC Circuit Breakers”, IEEE Transactions on Power Delivery, Vol. 35, Issue: 3, pp. 1515 - 1526 , 2020

10.3 CONFERENCE CONTRIBUTIONS

- N.A. Belda, R.P.P. Smeets, S. Tokoyoda, H. Ito, “Testing of HVDC Circuit Breakers”, CIGRE Conference, paper A3-109, 2016

- N.A. Belda, C.A. Plet, R.P.P. Smeets, R.M. Nijman, “Stress Analysis of HVDC Circuit Breakers for Defining Test Requirements and its Implementation”, CIGRE A3/B4/D1 Int. Coll. HVDC & HVAC Network Technologies for the Future, paper 009, Winnipeg, Sept. 30 – Oct. 6, 2017
- S. Tokoyoda, T. Inagaki, K. Tahata, et al., “DC current interruption tests with HV mechanical DC circuit breaker”, CIGRE Winnipeg 2017 Colloquium, paper A3/B4-124, 2017
- N. A. Belda, C. A. Plet, R. P. P. Smeets, R. Nijman, et al “Full Power Short-circuit Tests of HVDC Circuit Breakers using AC Generators Operated at Reduced Power Frequency”, CIGRE Conf. , paper A3/15, 2018
- P. Hock, N.A. Belda, V. Hinrichsen, R. Smeets, “ Investigations on Metal-Oxide Surge Arresters for HVDC Circuit Breaker Applications”, INMR World Conf., Tucson, USA, 2019
- 纳德夫. 阿迪苏.贝尔达, 科内利斯.阿里埃.普莱特, 雷内.比彼得.保罗.斯梅茨 (N.A. Belda, C.A. Plet, R.P.P.), Smeets): “高压直流多端电网故障分析确定高压直流断路器试验要求 (Analysis of Faults in Multiterminal HVDC Grid for Definition of Test Requirements of HVDC Circuit Breakers) 5th China Int. High Power Test and Measurement Technical Forum, Suzhou, 2019
- R. le Roux, S. Roche, N.A. Belda, “Utilization of Metal Oxide Surge Arresters in HVDC Circuit Breakers and Similar Application”, Int. Conf. on Cond. Mon., Diagn. and Maint., paper 4-8, Bucharest, 2019
- L. Änquist, S. Nee, T. Modeer, et al., “VARC DC Circuit Breaker – a Versatile Concept for Non-Zero Current Interruption”, CIGRE Conf., paper A3-103, 2020
- S. Tokoyoda, T. Inagaki, H. Sadakuni, et al. “Development and testing of EHV mechanical DC circuit breaker”, 5th Int. Conf. on Electr. Pow. Equipment – Switching Techn., paper E4-4, Kitakyushu, Japan 2019
- R.P.P. Smeets, N.A. Belda, ”HVDC Fault Current Interruption Technology”, invited lecture, 5th Int. Conf. on Electr. Pow. Equipment – Switching Techn., Kitakyushu, Japan 2019
- N. A. Belda, R. P. P. Smeets, R. M. Nijman, M. Poikilidis and C. A. Plet, “High-Frequency Current Interruption of Vacuum Interrupters in an Experimental DC Circuit Breaker”, paper E4-4, 5th Int. Conf. on Electr. Pow. Equipment – Switching Techn., Kitakyushu, Japan 2019
- L. Ängquist, S. Nee, T. Modeer, A. Baudoin, S. Norrga and N. A. Belda, "Design and test of VSC assisted resonant current (VARC) DC circuit breaker", *Proc. 15th IET Int. Conf. AC DC Power Trans.*, pp. 1-6, 2019.

10.4 PUBLIC TUTORIALS AND WORKSHOPS OUTSIDE PROMOTION

- R.P.P. Smeets, tutorial on HVDC Switchgear, 4th Int. Conf. on Electr. Pow. Equipment – Switching Techn., Xi’an, China 2017
- R.P.P. Smeets, J. Hu, CIGRE A3/B4 tutorial on HVDC Switchgear, IEEE Switchgear Committee meeting, Orlando, USA, 2018

- C. Plet, R.P.P. Smeets, CIGRE SC A3 panel session on HVDC circuit breakers, CIGRE Conference, Paris, 2018
- C.A. Plet, N.A. Belda, Tutorial, CIGRE-IEC 2019 Conf. on EHV and UHV (AC & DC) April 23-26, Hakodate, Japan, 2019
- N.A. Belda, Panel Session on HVDC circuit breakers, 5th Int. Conf. on Electr. Pow. Equipment – Switching Techn., Kitakyushu, Japan 2019
- R.P.P. Smeets, “HVDC Fault Current Interruption Technology”, workshop AC-DC Protection Essentials for the Future, Delft University, Feb. 19, 2020
- N.A. Belda, “Performance Demonstration of full-scale HVDC Circuit ”, Panel session on HVDC grid protection and protection equipment, IEEE PES General Meeting, online, 2020
- N.A. Belda, R.P.P. Smeets “HVDC Circuit Breaker Testing”, CIGRE Forum on HVDC grid technology, on-line, 2020

10.5 AWARD

- Wang Jimei Young Investigator Award to N.A. Belda for the paper: “High-Frequency Current Interruption of Vacuum Interrupters in an Experimental DC Circuit Breaker”, presented at 5th Int. Conf. on Electr. Pow. Equipment – Switching Techn., Kitakyushu, Japan 2019



Figure 33: Demonstration of SciBreak 80 kV HVDC VARC circuit breaker



Figure 32: Demonstration of Mitsubishi Electric 160-200 kV active current injection circuit breaker



Figure 34: Demonstration of ABB 320 kV hybrid circuit breaker

11 REFERENCES

-
- [1] Smeets, R.P.P, van der Sluis, L. , Kapetanovic, M., Peelo, D.F., Janssen, A.L.J., “Switching in Electrical Transmission and Distribution Systems”, John Wiley & Sons, ISBN 978-118-38135-9, 2015
Chinese edition: 输配电系统电力开关技术, John Wiley, China Machine Press, ISBN 978-7-62086-0, pp. 1 – 358, 2019
 - [2] Ito, H. (editor), “Switching Equipment”, CIGRE Green Book, Springer Int. Publ. Co., ISBN 978-3-319-72537-6, 2019
 - [3] van Hertem, D., Gomis-Bellmunt, O., Liang, J., "HVDC Grids for Offshore and Supergrid of the future", John Wiley & Sons, ISBN 978-1-118-85915-5, 2016
 - [4] The EU Horizons 2020 project PROMOTioN ("Progress on Meshed HVDC Offshore Transmission Networks") seeks to develop meshed offshore HVDC grids on the basis of cost-effective and reliable technological innovation, <https://www.promotion-offshore.net/>, 2016-2020
 - [5] Antoine, O., Henneux, P., Karoui, K. et al., "Towards a deployment plan for a future European offshore grid: Development of topologies", CIGRE Conf., paper B4-131, 2020
 - [6] Moore, J., van Uden, J., Antoine, O. et al., "Towards a deployment plan for a future European offshore grid: Cost-benefit analysis of topologies", CIGRE Conf., paper B4-123, 2020
 - [7] Warnock J. , McMillan, D., Pilgrim, J., Shenton, S., "Failure Rates of Offshore Wind Transmission Systems", *Energies*, 12, 2019
 - [8] Kurkowska, M., "Cable malfunctions", *Offshore Cabling*, 2018
 - [9] Lindblad, P., "Reliability of existing HVDC links feedback", *CIGRE Sci. & Eng.*, nr. 11, pp. 96-103, 2018
 - [10] Franck, C.M., "HVDC Circuit Breakers: A Review Identifying Future Research Needs", *IEEE Trans. on Pow. Del.*, Vol. 26, No. 2, pp. 998-1007, 2011
 - [11] Jovcic, D., Tang, G., Pang, H., "Adopting Circuit Breakers for High-Voltage dc Networks", *IEEE Pow. & Energy Mag.*, Vol. 17, issue 3, 2019
 - [12] Bertinato A., Gonzales, J.C. et al., "Development of a protection strategy for future DC networks based on low-speed DC circuit breakers", *CIGRE Conf.*, paper A3-111, 2018
 - [13] Jovcic, D., Lin, W., Nguefeu, S., Saad, H., "Low-energy protection System for DC grids Based on Full-Bridge MMC Converters", *IEEE Trans. on Pow. Del.*, vol. 33, no.4, pp. 1934-1943, 2018
 - [14] Pucher, W., "Fundamentals of HVDC interruption", *Electra*, No. 5, pp. 24-39, 1968
 - [15] Belda N.A., Plet, C.A., Smeets, R.P.P., "Analysis of Faults in Multiterminal HVDC Grid for Definition of Test Requirements of HVDC Circuit Breakers", *IEEE Trans. on Pow. Del.*, vol. 33, no. 1, pp. 403 - 411, 2018
 - [16] Leterme W., Jahn, I., Ruffing, P. et al., "Designing for High-Voltage dc Protection", *IEEE Pow. and Energy Magazine*, June 2019
 - [17] Li, X., Yuan, Z., Fu, J., Wang, Y., Liu, T., "Nanao multi-terminal VSC-HVDC project for integrating large-scale wind generation", *IEEE PES General meeting*, 2014
 - [18] Zhang, Z., Li, X., Chen, M. et al., “Research and Development of 160kV Ultra-Fast Mechanical HVDC Circuit Breaker”, *Pow. Syst. Techn.*, Vol. 42, No. 7, pp. 2331-2338, 2018
 - [19] Zhou, H., Li, H., Xie, R. et al., “Research of DC circuit breaker applied on Zhoushan multi-terminal VSC-HVDC project”, *IEEE Asia Pacific PES Conf.*, 2016
 - [20] Tang, G., Wei, X., Zhou, W. et al., “Research and Development of a Full-bridge Cascaded Hybrid HVDC Breaker for VSC-HVDC Applications”, *CIGRE Conf.*, paper A3-117, 2016
 - [21] Tang, G., Wang, G., He, Z. et al., “Research on Key Technology and Equipment for Zhangbei 500 kV DC Grid”, 2018 Int. Pow. Electronics Conf. (IPEC-Niigata 2018 -ECCE Asia), Niigata, Japan, pp 2343- 235, 2018
 - [22] Tang, G., He, Z., Pang, H. et al., “Characteristics of system and parameter design on key equipment for Zhangbei DC grid”, *CIGRE Conf.*, paper B4-121, 2018
 - [23] Yang, B., Cao, D., Shi, W. et al., “A novel commutation-based hybrid HVDC circuit breaker”, *CIGRE Winnipeg Colloquium*, paper A3-15, 2017
 - [24] Tang, G., "Development of 500kV Modular Cascaded Hybrid HVDC Breaker for DC Grid Application", *CIGRE Conf.*, paper A3-105, 2018
 - [25] Gu, W., Feng, D., Guo, Z., “Development of High-Speed Mechanical Switchgear with Vacuum Interruption Technology and Application in HVDC Circuit Breaker”, 3rd IEEE Int. Electr. And Energy Conv. Conf. (CIEEC), 2019
 - [26] Wen, W., Huang, Y., Li, B. et al., “Technical Assessment of Hybrid DCCB With Improved Current Commutation Drive Circuit”, *IEEE Trans. on Ind. Appl.*, Vol.54, No.5, pp. 5456-5464, 2018
 - [27] PROMOTioN deliverable 5.1: HVDC network fault analysis, 2016

-
- [28] Kristian Vrana, T., Yang, Y., Jovicic, D. et al., "The CIGRE B4 DC Grid Test System", *Electra* no. 270, pp. 1-19, 2015
- [29] PROMOTioN deliverable 5.3: Fault Stress Analysis of HVDC Circuit Breakers, 2017
- [30] PROMOTioN deliverable 5.2: PSCAD models of HVDC circuit breakers, 2016
- [31] PROMOTioN deliverable 5.4: Document on test requirements, 2017
- [32] PROMOTioN deliverable 5.7: Realization of Test Environment for HVDC Circuit Breakers, 2017
- [33] CIGRE Joint Working Group A3B4.34, "Technical requirements and specifications of state-of-the-art HVDC Switching Equipment", CIGRE Techn. Brochure 683, 2017
- [34] IEC TC17/17C: Ad Hoc Group 04: HVDC Switchgear; Document 17/1032/INF to investigate market relevance of DC switchgear and the need for standardisation, 2017
IEC TC17/17A: Ad Hoc Group 60: DC Switchgear: Document 17A/1200/INF to further investigate the need for standardization of DC switchgear, 2018
- [35] IEC TC115: IEC TS 63014-1, "High voltage direct current (HVDC) power transmission - System requirements for DC-side equipment - Part 1: Using line-commutated converters", 2018
- [36] PROMOTioN deliverable 10.3: Acquisition of input data for characterization of stress withstand of breaker sub-components, 2019
- [37] PROMOTioN deliverable 10.4: Document on Test Result Analysis, 2019
- [38] PROMOTioN deliverable 10.8: Initiation of standardization activities for HVDC circuit breaker design testing and application, 2020
- [39] IEC TC17/17C: Ad Hoc Group 04: HVDC Switchgear; Document 17/1032/INF to investigate market relevance of DC switchgear and the need for standardisation, 2017
IEC TC17/17A: Ad Hoc Group 60: DC Switchgear: Document 17A/1200/INF to further investigate the need for standardization of DC switchgear, 2018
- [40] Chinese draft standard GB/T 38328-2019, 柔性直流用高压直流断路器的共用技术要求 "Common specifications of high-voltage direct current circuit-breakers for high-voltage direct current transmission using voltage sourced converters", 2019
- [41] PROMOTioN deliverable D11.1: Harmonization catalogue, 2019
- [42] Belda, N.A., Smeets, R.P.P., Nijman, R.M., "Experimental Investigation of Electrical Stresses on the Main Components of HVDC Circuit Breakers", *IEEE Trans. Pow. Del.*, early access, DOI 10.1109/TPWRD.2020.2979934, 2020
- [43] PROMOTioN deliverable D10.2 Report Describing the Interaction of Test Objects with the Test Environment, 2019
- [44] PROMOTioN deliverable D10.3 Acquisition of input data for characterization of stress withstand of breaker subcomponents, 2019
- [45] IEC TR 62271-302: High-voltage switchgear and controlgear – Part 302: Alternating current circuit-breakers with intentionally non-simultaneous pole operation, 2010
- [46] Hock, P., Belda, N.A., Hinrichsen, V., Smeets, R.P.P., "Investigations on Metal-Oxide Surge Arresters for HVDC Circuit Breaker Applications", *INMR World Conf.*, Tucson, USA, 2019
- [47] le Roux, R., Roche, S., Belda, N.A., "Utilization of Metal Oxide Surge Arresters in HVDC Circuit Breakers and Similar Application", *Int. Conf. on Cond. Mon., Diagn. and Maint.*, paper 4-8, Bucharest, 2019
- [48] 张北柔性直流电网示范工程 500kV 机械式直流断路器试验方案 (Zhangbei Flexible DC Grid Demonstration Project, 500 kV mechanical DC circuit breaker test proposal, State Grid Economic and Technical Research Institute Co.), 2018
- [49] PROMOTioN deliverable D5.6: Software and analysis report on candidate test-circuits, 2018
- [50] N.A. Belda, C.A. Plet, R.P.P. Smeets, "Full-Power Test of HVDC Circuit-Breakers with AC Short-Circuit Generators Operated at Low Power Frequency", *IEEE Trans. Pow. Del.*, Vol. 54. Issue 5, pp.1843 – 1852, 2019
- [51] PROMOTioN deliverable D5.7: Realization of Test Environment for HVDC Circuit Breakers, 2018
- [52] PROMOTioN deliverable D10.1: Test Report Describing the Functioning of Test Circuits, 2019